Ceramic embedding of SiC-semiconductor using cofiring technology

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Abstract **-** The presented work demonstrates our current state in embedding of SiC power electronic dies using Ceramic Multilayer Technology. The novelty of the approach presented includes the cofiring of a semiconductor element with ceramic base material, which demands for a reduced sintering temperature of ceramics (using LTCC or ULTCC based ceramics) in combination with an increased temperature stability of the semiconductor**.**

Keywords—power electronics, embedding, SiC, LTCC, ULTCC, Multilayer Ceramics

I. Introduction

SiC-based semiconductors are currently used in the form of diodes and transistors. Within the application power electronics, the devices are used as field effect transistors (MOSFET) or Schottky-Diodes. Conventional assembly and connection technology involves soldering or metal sintering the semiconductor to a metalized ceramic substrate, with electrical contacting on the top using wire bonding technology. For encapsulation, the semiconductor can be injected with a plastic. More innovative approaches integrate the semiconductor into a polymer-based circuit board. Regardless of the type of semiconductor, the current assembly and connection technology (housing, potting compound and connection contacts) can only be operated up to temperatures of 200 °C for a short time and up to 150 °C for a long time. In addition, the housing materials currently used have poor corrosion resistance and mismatched thermal linear expansion. The proposed solution involves developing and establishing a high temperature-stable assembly without principal temperature limit and connection technology for SiC. For this purpose, the components are embedded in a multilayer ceramic package under ceramic-specific firing temperatures, sintered and at the same time electrically and thermally contacted.

II. State of the Art

A. Ceramic Multilayer Technology

Ceramic Multilayer Technology is an established method for the manufacturing of ceramic microcircuits [1]. The process (Fig. 1) uses ceramic green tapes, manufactured by tape casting, and functional pastes as semi-finished products. During a blanking step the ceramic tapes are cut into defined sizes (up to 8x8 sq inch) and geometrically structured by punching (creation of via holes) or lasing. The via holes will afterwards be filled by stencil printing of a metallization paste, followed by screen printing of a predefined conductor layout. The individually structured and functionalized tapes will be stacked, laminated and sintered. During the sintering process the laminated stack transforms into a highly robust monolithic ceramic body, while the functional structures can be buried into the ceramic. The process allows not only for the integration of conducting structures, but also for the embedding of other passive functionalities like resistors, capacitors or inductors.

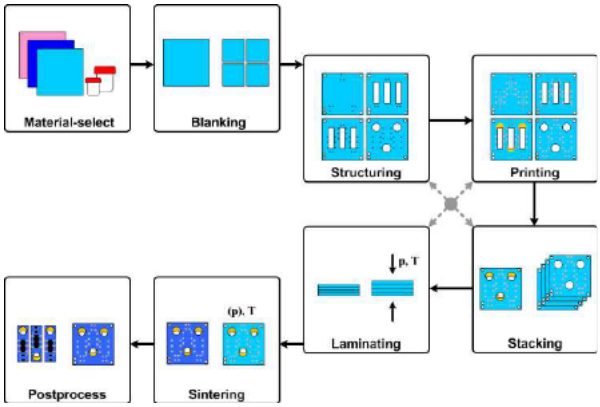


Fig. 1. Multilayer Ceramic Manufacturing Process

B. Semiconductor design and selection

SiC semiconductors are used in power electronics mainly for switching high electrical currents (up to several 100 A) and high voltages (up to several kV) in drives and energy converters. Because of its larger band gap, SiC has advantages compared to state of the art Si: higher junction temperatures (Tj $\geqslant$ 250 ° C, no practical temperature limit by intrinsic carrier density), higher power density and higher switching speed and switching frequency with lower switching losses. Due to the high thermal stability of the SiC, the power and power loss density can be increased during operation, resulting in significantly higher operating temperatures (T > 400 °C) of the chip. The SiC material can endure higher operation temperatures, the first limiting factor is the surface metallization of the SiC chip, which has to withstand these high temperatures. As part of the semiconductor development various metals or metal combinations were examined as

suitable high-temperature process-capable surface platings. SiC chips with selected layer stacks for the power metallization were chosen for the embedding investigations.

III. LTCC Embedding Technology

The initial approach of our work was the integration of a SiC semiconductor device in a pre-metallized and pre-structured LTCC green tape stack using commercially available LTCC tapes. After cofiring at the sintering temperature of the ceramic, a monolithic ceramic pre-package with embedded SiC device is generated (Fig. 2).

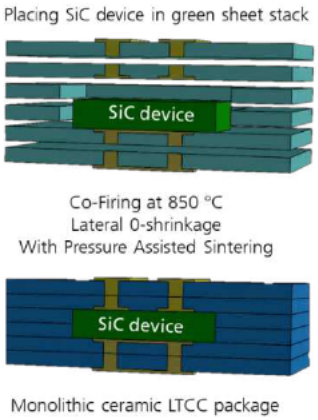
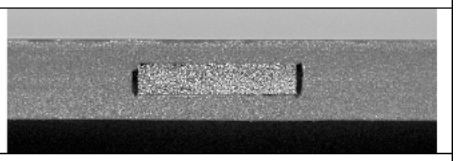


Fig. 2. Illustration of the approach: Embedding a SiC semiconductor device in a pre-metallized LTCC multilayer during cofiring using pressure assisted sintering

That approach requires a precise control of the shrinkage during cofiring. Especially, a lateral shrinkage of ≤ 1 % is important for a selective interconnection between the ceramic package and SiC device [2, 3]. Thus a pressure assisted sintering process [4,5] is applied to constrain the shrinkage in the x/y-direction.

The investigation [6] was performed with three commercial LTCC materials: GT 951 (DuPont©), L8 (Ferro©) and 9k7 (DuPont©). These materials have a recommended firing temperature of 850 °C. Further we selected two commercially available Ag via-fill pastes and two commercially available Ag conductor pastes for screen-printing. The embedding experiments were executed with SiC dummy dies with 2 and 5 mm edge length showing ohmic behavior. They were fabricated from a n-doped SiC wafer with a dopant concentration of ≥ 10^{18} cm^3. Top and bottom surface of the SiC dies were covered with a processed ohmic contact Ni_2Si layer and a power metallization layer. For the investigation of the embedding process we developed a 2 inch LTCC layout which enables the integration of four equal SiC chips in one process run. After laminating the green substrate with four integrated SiC chips they were co-fired in a box furnace (ATV PEO 603 - Sinterpresse, company ATV Technologie GmbH) under applied sinter pressure p_s. After the firing process the four segments of each substrate were separated by wafer dicing and in addition two segments were cut in the middle of the embedded chip within the same process to enable the documentation of the cross-section. A cross-section of SiC dummy chips with 2 mm edge length embedded in a 2 inch LTCC substrate at specified parameter combinations is illustrated and rated in Table I.

TABLE I. Embedding results for SiC dummy chips with 2 mm edge length at specified parameter combinations

material	**GT 951**
SiC chip size	2 mm square
parameter: *HR*; T_{max}; t_d; p_s	2 K/min; 850 °C; 60 min; 40 kPa
cross-section	
rating	feasible

For the mechanical/electrical embedding investigations we expanded the layout and the technology of the 2-inch LTCC sample preparation by the mechanical embedding of inner and outer contact pads as well as via structures to interconnect four SiC dies with 5 mm edge length inside the LTCC pre-package during sintering. For the embedding process we chose the material 9K7 and we reduced the firing temperature to 750°C at a heating rate of 5 K/min, a sintering pressure of 40 kPa and a dwell time of 2h to treat the SiC device with care. Adapted conductor paths connected the vias with the inner contact pads of the SiC device. We fabricated pre-packages with electrical interconnects between top and bottom side (Fig. 3) without any obvious defects.

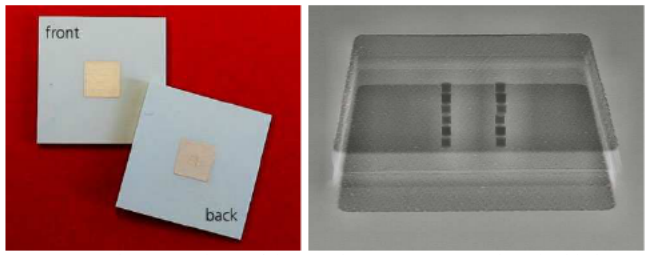


Fig. 3. Single pre-packages fabricated in LTCC 9K7 with embedded SiC dummy chips having 5mm edge length (component left, X-Ray image right)

Additionally, we evaluated the electrical interconnections of LTCC pre-packages with integrated SiC chips of different power metallizations (Table II) by measuring the resistance between top and bottom side of the package [7], [8]. For best package performance the resistance should be similar to the resistance of the ohmic dummy SiC dies (< 1 Ω).

TABLE II. *Characteristics of the fabricated LTCC Pre-packages*

	Fabricated pre-packages		
	Batch 1	***Batch 2***	***Batch 3***
Die generation	Power metallization A)	Power metallization B)	Power metallization B)
Resistance R (Ω), Package + SiC die	3.3 to 8.3	1.0 to 1.8	1.7 to 2.6

In-situ measurements of the resistance during heating exhibit the onset of a degradation at 600 °C for the investigated

power metallizations. At all, these effects are less distinctive at power metallization (B) than at (A) due to the implementation of an extra diffusion barrier.
Besides further optimization of the power metallization regarding higher temperature stabilities new materials with lower sintering temperatures had to be developed und qualified for the embedding process.

IV. ULTCC Embedding Technology

ULTCC (Ultra Low Temperature Cofired Ceramics) are a new class of multilayer ceramic materials made of glass-ceramic composites. They can be sintered at very low temperatures (400 °C to 700 °C), making their manufacturing process very energy efficient. These materials seem to be an elegant choice to reduce the temperature load of the semiconductor chips, while maintaining the design freedom of the Multilayer Ceramic manufacturing process.

For ULTCC development, appropriate materials and mixing approaches were derived. The approach concentrated on glass-ceramic composites. These are characterized by a mixture of inert ceramic powders (for example Al_2O_3 or SiO_2) and powder of a low-melting glass. The glass-ceramic composites are densified by non-reactive liquid phase sintering, whereby the glass melts, partially wets the ceramic particles and causes particle rearrangement and pore closure. This is majorly attributed to capillary forces and/or viscous flow. Corresponding material compositions were in a first step analyzed in the form of compacts with focus on density, sintering temperature and microstructure. Table III lists the relevant ULTCC compositions studied and compares the calculated density and the calculated coefficient of thermal expansion (TEC) corresponding to the blend ratios set.

TABLE III. ULTCC compositions under investigation

Description	Volume ratio filler [%]	Volume ratio glass [%]	Calc. Density [g/cm³]	Calc. TEC [ppm/K]
ULTCC65	65 %	35 %	3,7	3,1
ULTCC60	60 %	40 %	3,9	3,4
ULTCC55	55 %	45 %	4,0	3,7
ULTCC40	40 %	60 %	4,6	4,5

For the analysis of the sintering temperatures and the microstructure, compacts (Ø10 mm x approx. 2 mm) were produced from these powder mixtures with a pressure of 25 MPa and fired at 20 K/min at temperatures from 500 °C to 900 °C (holding time 30 min each). Subsequently, the density of the sintered bodies and the microstructure was analyzed. The plot of the relative density as a function of the firing temperature (Fig. 4) shows, that the temperature of maximum densification increases with increasing ceramic filler content. With a relative density of 92 % at 550 °C firing temperature, the composition ULTCC40 showed high potential for low temperature sintering while adjusting a microstructure without open porosity.

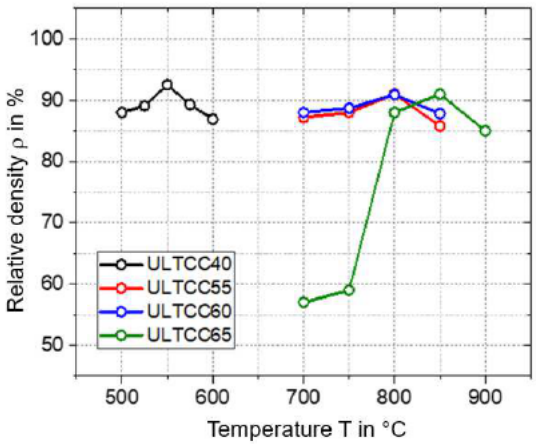


Fig. 4. Determination of the sintering temperature of ULTCC compositions with varying glass fractions

Based on an adapted composition named mULTCC40, the tape casting process for the ULTCC material was developed. For this purpose, a castable slurry was prepared by adding solvents, binders and plasticizers. In addition to setting the viscosity for the slurry, the challenge in this step was to select binder materials which can already be completely thermally extracted (debinding) below the sintering start of the ULTCC material. Subsequently, the slurry was deposited on a carrier film using a film casting system, dried and qualified. In a total of five iterative development stages, the slurry composition and film casting parameters were varied for realizing satisfactory film qualities. Fig. 5. visualizes important process steps during this development.

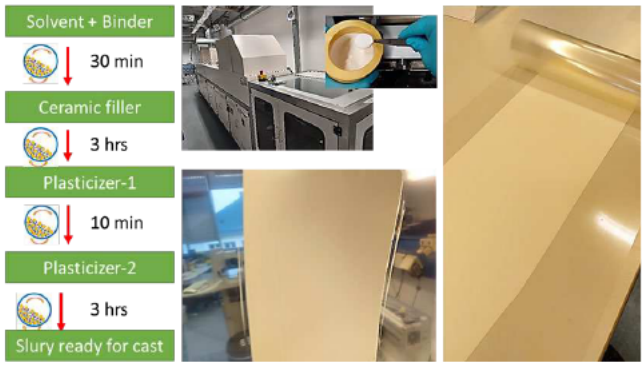


Fig. 5. Process steps in the development of tape casting for ULTCC materials

For testing the substrate manufacturing the green tapes were cut, punched, laminated and subsequently fired. Fig. 6 shows a laminate consisting of 4 layers with integrated 0,2 mm punched alignment marks for shrinkage evaluation.

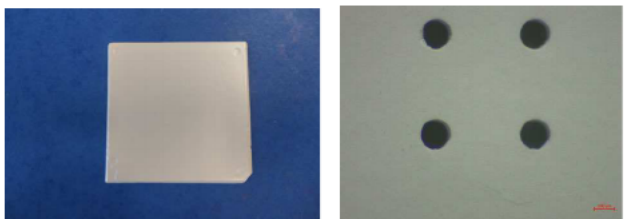


Fig. 6. ULTCC-based laminate (2"x2" size) with alignment marks for shrinkage measurement (left); punched 0,2 mm via holes (right)

Subsequently the material was sintered in an unconstrained sintering process (without pressure assistance). Table IV shows the determined density, calculated porosity and the measured water absorption of the material sintered at 480 °C/30min.

TABLE IV. Characterization of mULTCC40 after unconstrained sintering

Sample	Sintering profile	Density in g/cm³	Porosity in %	Water absorption in %
mULTCC40	480°C/ 30 min	5,18	< 1%	0,02

In Fig. 7 the microstructure of the sintered material is presented. The low magnification represents the entire substrate with the magnified pictures are focusing on the center and the top region of the substrate. The results show that the sample is well compacted in agreement with the density and water absorption measurements. The residual glass phase in combination with the filler materials can be clearly identified. Besides the initial filler materials (Al_2O_3 and SiO_2) additional secondary phases have formed. They improve the mechanical stability of the ceramic and provide stability during further firing steps.

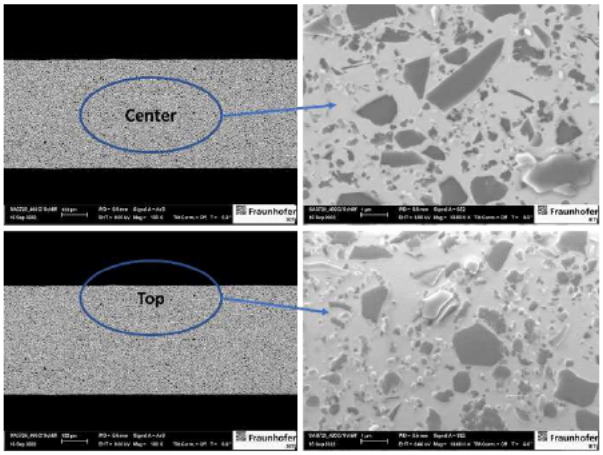


Fig. 7. Microstructure of mULTCC40 sintered at 480°C/30 min

Due to the need for a precise shrinkage control in the chip embedding step (lateral shrinkage of ≤ 1 %) the ULTCC material must be fired in a pressure sintering process (compare to section III). Thus, an additional shrinkage investigation of mULTCC40 material was performed by a thermal mechanical analysis using the vertical dilatometer TMA 402 F1/F3 Hyperion (Netzsch-Gerätebau GmbH). Cylindrical samples (Ø5 mm x approx. 2 mm) were laser cut out of a ULTCC laminate. During the experiments a uniaxial pressure of 40 kPa was applied to the samples, while the axial shrinkage (ε_z), which corresponds directly to the measured strain, was determined. Fig. 8 shows the results of the TMA measurement.

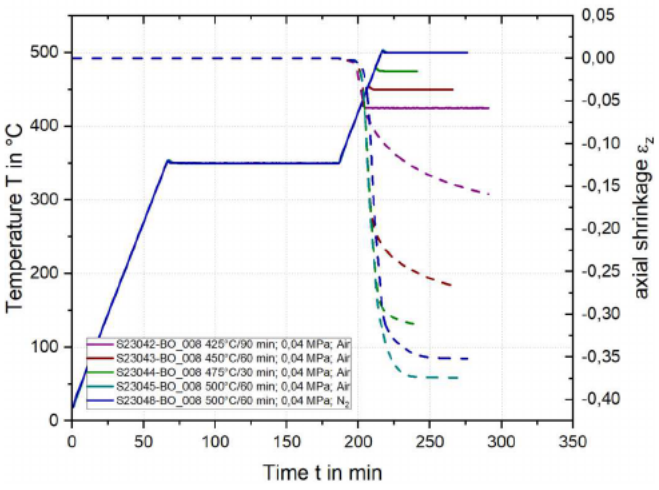


Fig. 8. TMA analysis of mULTCC40 with variation of sintering profile and atmosphere

After a debinding phase at 350°C the ceramic starts to shrink at 400°C until the sintering ends at approx. 500°C. For a dense sintered state an axial shrinkage of about 35% was determined, which must be considered in the design of the future package. The shrinkage behavior under nitrogen atmosphere is comparable to the measurement in air, which is favorable for the stability of the SiC chip power metallization.

Based on these results first mechanical integration experiments for embedding SiC dummy chips in ULTCC material were conducted. SiC dies were embedded in 5 Layer ULTCC laminates, isostatically laminated at 5 MPa and sintered in air (Fig. 9).

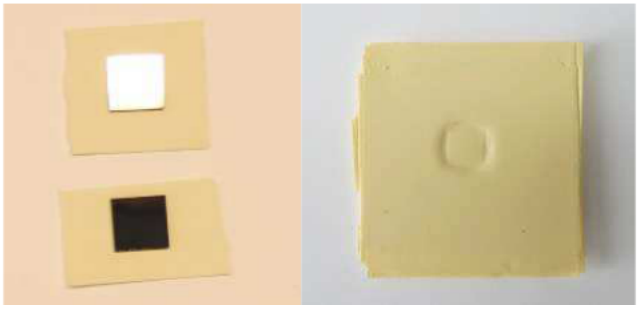


Fig. 9. ULTCC packaging of SiC dummy chips (left: before lamination step, right: after cofiring)

The first results show, that crack and delamination free embedding of SiC dummy chips is possible within ULTCC base material. Nevertheless, further studies related to appropriate shrinkage control and implementation of metallization structures must be done.

V. Conclusion and Outlook

In this contribution we introduced a new approach to embed SiC semiconductor devices in full ceramic pre-packages to provide higher operation temperatures and better switching properties for power electronic applications. Initial investigations showed that the embedding of SiC power chips can be successfully realized in LTCC manufacturing

technology using a pressure assisted sintering process. A major drawback of LTCC materials are the high sintering temperatures (> 700°C) leading to a significant temperature load on the power metallization of the SiC chips. This favors degradation and limits their electrical performance. Besides optimizing the temperature stability of the metallization, the reduction of the ceramic sintering temperature is a decisive step to solve these problems. Thus, a new type of low temperature sintering ceramics (ULTCC) was investigated. ULTCC materials were identified, synthesized, transferred into ceramic green tapes and characterized regarding processability, sintering behavior and microstructural properties. The investigation shows that a sintering of these materials below 500°C is possible, combined with the achievement of an attractive pore free microstructures. First mechanical embedding tests were successfully completed. However, the future work on this topic has to deal with additional challenges as follows:

- Further characterization of the physical properties of selected ULTCC materials,
- Development of new metallizations pastes with suitable constrained shrinkage behavior adapted to ULTCC materials,
- Optimization of sintering parameters to reduce free spaces on the sides walls of the embedded SiC dies using sinter simulations and
- Verification of the approach with real SiC semiconductor devices (transistor) regarding interconnection, isolation and switching behavior at temperatures > 300 °C.

ACKNOWLEDGMENT

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