20 μm copper micro-bump bonding through a silver metallization for advanced packaging under a low-pressure condition

Zheng Zhang[1], Ming-Chun Hsieh[1], Aiji Suetake[1], Hiroshi Yoshida[1], Rieko Okumuara[1], Noriko Kagami[1], Kazamasa Okamoto[1], Chuantong Chen[1], Kei Hashizume[2], Norihiko Hasegawa[2], Ryuji Yoshida[2], Hidekazu Homma[2], and Katsuaki Suganuma[1]

[1]*Flexible 3D System Integration Lab, SANKEN, Osaka University, 5670047, Japan*
[2]*Okuno Chemical Industries Co. Ltd, 5410045, Japan*
Corresponding author email: zhangzheng@sanken.osaka-u.ac.jp

***Abstract*—In this work, we proposed a copper (Cu) micro-bump bonding strategy by using a silver (Ag) metallization layer as an interconnect bridge. Si chips with 20 μm Cu-Ag bumps were bonded under a low pressure (0.4 MPa) and atmospheric conditions at 250 °C. By investigating the surface morphology evolution of the Cu-Ag bump, it is found that severe surface deformation caused by Ag abnormal grain growth and hillock generation plays a critical role in the Cu-Ag bump bonding, which facilitates the approach and bonding of top and bottom Ag surface of the bump structure. Moreover, this bonding strategy is expected to be particularly advantageous for fine-pitch interconnect applications. It not only mitigates the severe bonding condition requirements that are used in thermal compression bonding and hybrid bonding, but also provides higher quality bonding structures for advanced packaging.**

Keywords—micro-bumps, advanced packaging, low pressure bonding, low temperature bonding

I. INTRODUCTION

In the last few decades, the rapid development of material science and high precision engineering have enabled us to scale down the transistor size and integrate more transistors in a confined space. However, scaling down the transistor size are becoming more and more difficult due to the limitation of ultraviolet photolithography, making the two-dimensional integrated circuits (ICs) approach the limit of Moore's law. To address such a dilemma, one popular solution is to utilize the vertical space by stacking Si dies, which is also known as advanced packaging. On the one hand, stacking of Si dies can significantly increase the number of transistors that can be accommodated within the limited space. This greatly benefits the continuation of the enhancement in the performance and functionality of the ICs. On the other hand, the wire distance can be reduced using the through Si vias that are buried in the Si die, which enables faster data transmission with less power consumption.

Micro-bumps bonding technology is one of the critical approaches that has been widely applied in advanced packaging, which can provide the vertical interconnect among the stacked dies. The micro-bumps, consisting of a Cu post with a Ag-Sn solder cap, are made by electroplating. During the packaging procedure, the micro-bumps are aligned and in contact with the bonding pad, and the solder caps act as a bridge that provides the connection between micro-bumps and bonding pads after reflowing. Currently, the most advanced bump bonding used for commercial products owns a 40 μm pitch and 20 μm bump size[1]. In order to meet the rapidly increased input and output number in the high-end devices, researchers are engaging in the development of fine pitch bump bonding (less than 40 μm) as well as the availability of them in a realistic application[2, 3].

Although massive efforts have been made on the fine pitch bump bonding, there are many concerns about the reliability of the bump bonding in a longtime service due to brittle intermetallic compounds (IMCs) generation in the bonding structure. The Sn in the solder cap can react with the Cu in the pillar, resulting in brittle Cu-Sn IMCs at the bonding interface. In addition, current density among the bump becomes higher due to the decrease of the bump size, which gives rise to the voids and degradation caused by electrical migration. Therefore, researchers are seeking for alternatives to replace the solder cap, which not only provides a robust bonding but also high reliability.

Advanced packaging using a pure metal passivation layer is a promising alternative to the current solder-capped micro-bump bonding technique. The Cu-to-Cu interconnect can be achieved through the use of a pure metal intermediate layer at high temperatures and pressures, without concerns about the generation of intermetallic compounds (IMCs). Chen et al. have utilized thin layers of Pd[4], Au[5], Cr[6], and Ag[7] to cover the surface of Cu, resulting in high-quality bonding structures under high-vacuum conditions. Chang et al. [8] prepared pure Ag bumps and conducted Ag-Ag direct bonding under atmospheric conditions at high bonding pressures. The bonding exhibited high strength due to the oxidation-reduction properties of Ag. However, requirements such as high bonding strength or vacuum conditions have greatly limited the widespread application of passivation layer bonding.

In this work, we proposed a Cu bump bonding method with the assistance of a Ag passivation layer. Unlike the previously reported works, we achieved the bonding under a low bonding pressure condition of only 0.4 MPa. In addition, we prepared the 20 μm Cu-Ag bumps via sputtering, and demonstrated the feasibility of the Ag layer in the fine pitch bump interconnect.

II. EXPERIMENT

A. Preparation of bonding samples

Two series of bonding samples, sputtered bare Si chip and sputtered Cu-Ag bumps were prepared for the investigation of bonding performance and demonstration of fine pitch bonding.

The bare Si chips with a size of 5×5 mm^2 and 10×10 mm^2 were sputtering with Ti (100 nm)/Cu (500 nm)/Ti (100 nm)/Ag (500 nm) under a sputtering power of 200 W and a chamber pressure of 0.2 Pa, separately. The small Si chip was

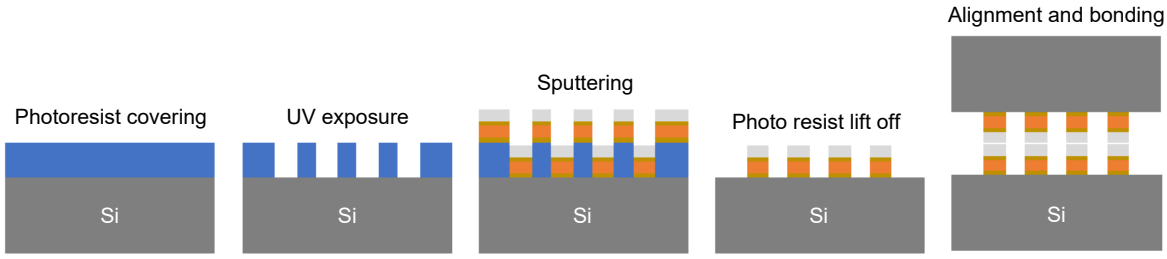

Fig. 1 Schematic drawing of the Cu-Ag bump sample preparation processes.

then bonded to the large Si chip under a low bonding pressure (0.4 MPa) and an atmospheric condition at 250 °C for 30 min. The prepared samples were then carried out the non-destructive and destructive characterizations for investigating the face to face bonding performance.

The process for the preparation of the Cu-Ag bump sample is depicted in Fig.1. At first, bare Si chips (10×10 mm^2) were covered with photoresist and exposed to UV light using a photomask. Once the patterning is complete, the chip is placed in a sputtering machine for metallization with a layer sequence of Ti (50 nm)/Cu (250 nm)/Ti (50 nm)/Ag (250 nm). To enhance the quality of the bumps, the thickness of the metallization layer is reduced, which facilitates the liftoff of the photoresist. At last, the liftoff Si samples are aligned using a flip-chip bonder (T-3000, Tresky) and bonded under low pressure of 0.4 MPa and atmospheric conditions at a temperature of 250 °C for 30 minutes.

B. Characterizations

The bonding quality of the large area bonding sample was investigated via scanning acoustic microscopy (SAM, FineSAT, HITACHI) at first and then cleaved for the cross-sectional structure observation. The cleaved sample was polished by an ion-milling machine (IM4000, HITACHI). Scanning electron microscopy observation was carried out using the SU-8000 (HITACHI high tech.). Surface roughness of the sputtered and annealed Si chip was measured by atomic force microscopic (AFM5000, Hitachi High-tech).

III. Results and Discussion

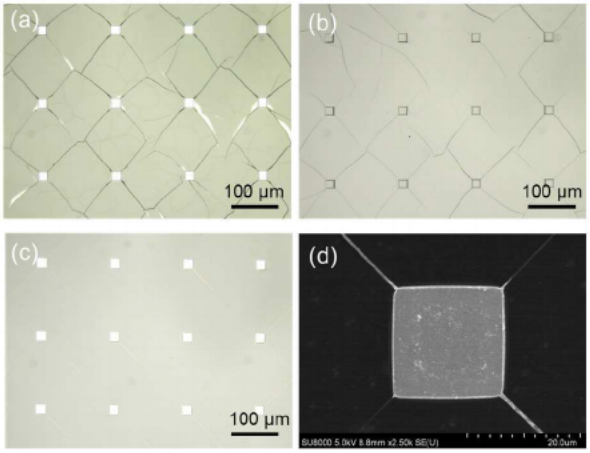

Fig. 2 Images of photoresist after masking (a), after sputtering (b), after liftoff (c), and SEM image of the prepared Cu-Ag bump.

Images in the process of Cu-Ag bump preparation were taken, as shown in Fig. 2. Fig. 2a shows the optical image of the photoresist after masking. Square holes with an edge length of 20 µm and a pitch length of 150 µm were prepared after UV exposure. Then, the Si chips were put into a sputtering machine for continuous Ti/Cu/Ti/Ag metallization. These square holes were filled with the multi-metallization layers as shown in Fig. 2b. After liftoff, the photoresist with the covered sputtering layer was removed and the metallization in the square holes left on the chip as depicted in Figure C. Figure d shows the SEM observation of the prepared Cu-Ag bump. The bump surface shows a clean surface and there is no photoresist residue left at the edge of the bump, which indicated a total removal of the photoresist.

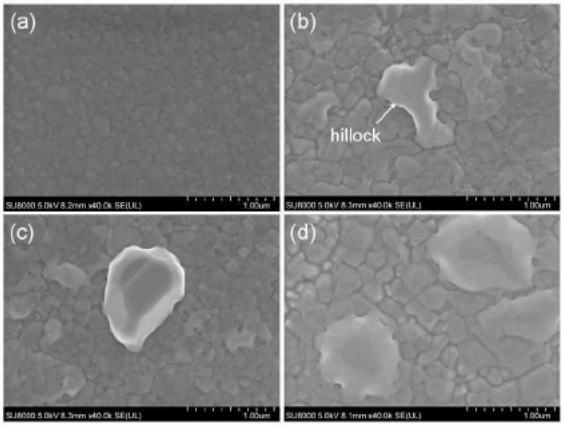

Fig. 3 Surface morphology variation of the Cu-Ag bump. As-sputtering (a), 5 min annealed (b), 15 min annealed (c), and 30 min annealed (d).

Morphologies of the sputtered Ag surface were examined before and after heating, as shown in Fig. 3. The as-sputtered Ag surface (Fig. 3a) appears a smooth surface with fine Ag grains that have a size of around 100 nm. Fig. 3b shows the Ag surface morphology after 5 min annealing at 250 °C. Size of the Ag grains became larger than the as-sputtered grain due to the grain growth at a high temperature. A large Ag grain, approximately 500 nm in size, protrudes from the surface, resulting from abnormal grain growth known as hillock generation. Interestingly, massive nanoparticles are observed on the surface, which can be attributed to the oxidation of Ag grains. Ag trends to absorb the oxygen and generate Ag oxide before 420 K[9]. However, the generated Ag oxide decomposes into pure Ag and oxygen with a further increase of temperature[10]. Thus, this reversible reaction leads to the formation of numerous in-site nanoparticles on the Ag surface. Fig. 3c presents the Ag surface morphology after 15 min annealing. The Ag fine grains merge into together and the hillock becomes larger due to the extended annealing time. With 30 min of annealing, more hillocks appear on the surface due to further abnormal grain growth.

In addition, surface roughness was measured to confirm the variation in Ag surface during the annealing. Fig. 4 presents the AFM images of the initial Ag surface and the surface after 5 min annealing. The as-sputtered Ag surface

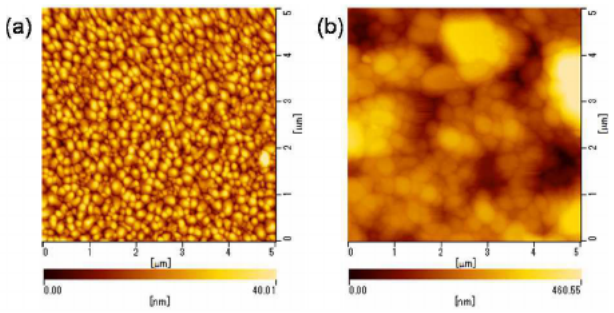

Fig. 4 AFM images of the as-sputtered surface (a) and 5 min annealed surface (b).

shows a uniform morphology with massive fine Ag grains (Fig. 4a). The depth range on the surface is less than 40 nm. However, after 5 min of annealing (Fig. 4b), the surface morphology has completely altered, characterized by the presence of larger Ag grains and hillocks. Simultaneously, the depth range increases to over 460 nm due to severe abnormal grain growth. The surface roughness (arithmetical mean height, Sa) of the as-sputtering Ag surface is 5.12 nm, whereas the roughness significantly increased to 65.84 nm which is almost 13 times higher than the initial state.

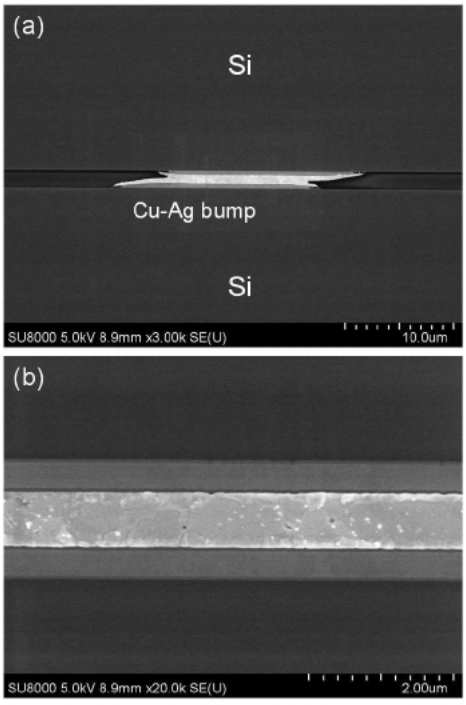

Fig. 5 SEM images of the cross section of the bonded Cu-Ag bump sample.

Cross section of the prepared Cu-Ag bump bonding sample was observed and investigated via SEM. Fig. 5a shows the overall view of the bump structure. The topside Cu-Ag bump intimately bonds to the bottom one through the Ag layer without a gap in between. A slight misalignment of about 4 μm occurred caused by the bonding instrument deviation. A magnified view of the bonding interface is exhibited in Fig. 5b. The multi-layer structure of the Cu-Ag bump can be clearly distinguished. The Ag layer has completely become an entirety and the bonding interface cannot be identified anymore, which is on account of the severe abnormal grain growth and hillock generation. The severe deformation of the Ag makes a much more easy encounter of the top and bottom surface, leading to the bonding of the Cu-Ag bumps. This uniform bonding structure suggests the Ag layer can provide a good bonding quality for the chip to chip interconnect.

IV. Conclusions and Outlook

In this work, we realized a 20 μm Cu bump bonding by applying a Ag intermediate layer as a bonding bridge. The 20 μm bump structure, consisting of Ti/Cu/Ti/Ag was prepared by continuous sputtering. The bonding of the prepared Cu-Ag bump sample was accomplished under low pressure (0.4 MPa) and atmospheric condition at 250 °C by using a flip-chip bonder. By investigating the Ag surface morphology variation, severe deformation due to the abnormal grain growth and hillock generation occurred after the annealing process. The AFM results suggest that surface roughness changed from 5.12 nm to 65.84 nm after the annealing. The deformed surfaces allow the contact of the top and bottom, thus creating a robust and uniform bonding interface. This bonding strategy shows great potential for achieving the mild bonding condition for the advanced packaging, which is expected to cut down manufacturing costs and improve the throughput of the packaging.

Acknowledgment

This paper is based on results obtained from a project from “Research and Development Project of the Enhanced Infrastructures for Post-5G Information and Communication Systems” JPNP20017, subsidized by the New Energy and Industrial Technology Development Organization (NEDO).

References

[1] M. Datta “Manufacturing processes for fabrication of flip-chip micro-bumps used in microelectronic packaging: An overview”. *Journal of Micromanufacturing*, 2020, 3(1): 69-83.

[2] M. Mariappan *et al*., "Tight-Pitched 10 μm-Width Solder Joints for c-2-c and c-2-w 3D-Integration in NCF Environment," *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2022, pp. 1138-1143.

[3] M. H. Chan *et al*., "Comparison of 3D Packages with 20μm bump pitch using reflow soldering and thermal compression bonding," *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2021, pp. 481-486.

[4] Y. -C. Tsai, H. -W. Hu and K. -N. Chen, "Low Temperature Copper-Copper Bonding of Non-Planarized Copper Pillar With Passivation," in *IEEE Electron Device Letters*, 2020,vol. 41, no. 8, pp. 1229-1232.

[5] Z. -J. Hong *et al*., "Room Temperature Cu-Cu Direct Bonding Using Wetting/Passivation Scheme for 3D Integration and Packaging," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 387-388.

[6] D. Liu, P. -C. Chen and K. -N. Chen, "A Novel Low-Temperature Cu-Cu Direct Bonding with Cr Wetting Layer and Au Passivation Layer," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2020, pp. 1322-1327.

[7] T. -C. Chou *et al*., "Electrical and Reliability Investigation of Cu-to-Cu Bonding With Silver Passivation Layer in 3-D Integration," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 1, pp. 36-42, Jan. 2021.

[8] Chang, Leh-Ping, et al. "Low temperature Ag-Ag direct bonding under air atmosphere." *Journal of Alloys and Compounds* 862, 2021pp. 158587.

[9] M. L. Zheludkevich, et al. "Oxidation of silver by atomic oxygen." *Oxidation of metals* 61.1-2, 2004, pp. 39-48.

[10] J.Assal, B. Hallstedt, L. J. Gauckler. "Thermodynamic assessment of the silver–oxygen system". *Journal of the American Ceramic Society*, 1997, 80(12). pp. 3054-3060.