Characterization of Embedded and Thinned RF Chips

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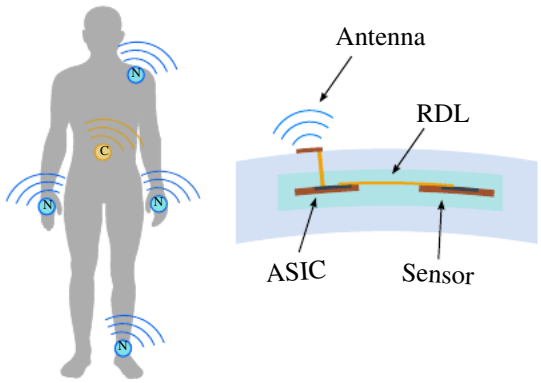
***Abstract*—This work studies the effect of thinning down chips with transmission line structures for flexible embedding technology. Test chips with 90 Ω grounded coplanar waveguide (G-CPW) transmission lines have been designed and manufactured to characterize the high-frequency performance before and after embedding in sheet molding compound (SMC), and thinning down from 300 µm to 20 µm. Molding first technology enables single-die or multiple-die thinning with the embedding material while being held in the exact position, where the subsequent fan-out copper (Cu) redistribution layer (RDL) structuring realizes the direct contacts to the embedded chip, followed by semi-additive manufacturing of traces. The embedded and thinned chips are characterized by S-parameter measurements in the frequency range from 20 MHz to 65 GHz using a vector network analyzer (VNA). The results show the feasibility of the examined embedding and thinning processes which are suitable for millimeter wave (mmWave) components as shown by the example of a G-CPW transmission line without degrading its RF performance in terms of characteristic impedance and attenuation.**

***Index Terms*—chip embedding, chip thinning, flexible packaging, millimeter wave, tactile internet, transmission line**

I. Introduction

In the context of the Tactile Internet, a digital twin (DT) acts as an interface between a human and a machine [1]–[3]. It enables the real-time transmission of tactile sensations via a network, where the DT serves as a virtual image of physical objects or processes that are continuously updated. To allow the human to control the DT, a wireless body area network (WBAN) is used consisting of multiple tactile nodes (N) as shown in Fig. 1(a). Each tactile node has sensors that capture various physiological data such as heart rate, body temperature, movements, contacts, and contact force. This information is pre-processed and wirelessly transmitted to a central unit (C) where it is further processed and analyzed. In addition to sensors a tactile node also consists of an antenna and an application-specific integrated circuit (ASIC) including a radio frequency (RF) transceiver and a data processing unit. The packaging concept of such a node is illustrated in Fig. 1(b).

There are three main requirements for the tactile node: First, for a truly tactile experience, the nodes must be as thin and flexible as possible, forming an electronic skin. Second, they must be as small as possible. Third, depending on the application scenario and the number of sensors and actuators, and the connection of other wearables such as smart glasses to the WBAN, high-bandwidth data streams must be sent and received. The first requirement can be met using thinned electronics connected by a flexible redistribution layer



(a) (b)

Fig. 1. Human with wireless body area network consisting of tactile nodes (a) and packaging concept of a flexible tactile node (b).

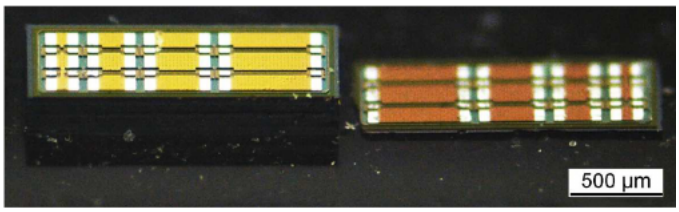
(RDL). The last two points can be addressed by operating the WBAN at mmWave frequencies (30 GHz-300 GHz), e.g. around 60 GHz, as suggested in [4]. In addition to a large amount of available bandwidth, the size of an antenna and other passives used in the transceiver scale inversely with frequency [5]–[11].

Flexible ASICs can be realized either by inherently flexible semiconductors consisting of non-silicon organic and inorganic semiconductors [12]–[15] or by thinning fully processed conventional semiconductors. The latter approach has the advantage of high carrier mobilities in established high-speed silicon technologies needed for operation at mmWave frequencies [16]. Thinned down to 20 µm, silicon chips get flexible and even more stable during bending compared to larger thicknesses between 50 µm to 100 µm [17]–[19]. At mmWave frequencies, thinning down these structures impacts not only the characteristics of active devices such as transistors but also passives such as transmission lines [20], [21].

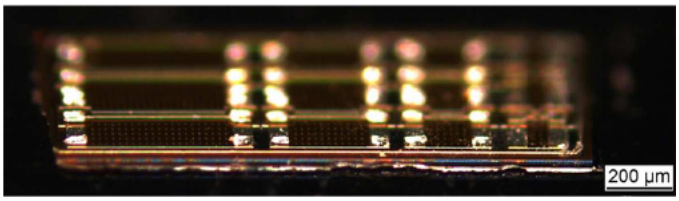
In this work, the process of embedding and thinning of silicon chips with transmission line structures is studied, and the effect of thinning down is investigated by characterization of grounded coplanar waveguide (G-CPW) structures representing passive structures of an ASIC. The process has been intentionally designed to be compatible with conventional semiconductor manufacturing technology.

II. Methodology

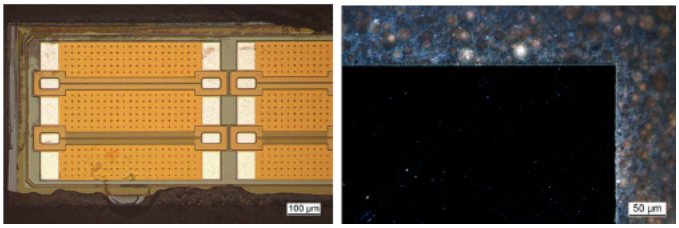
To study the impact of thinning on the RF performance of passive structures on silicon chips, test chips with 90 Ω G-CPW transmission lines have been designed and analyzed. The analysis has been carried out before and after embedding and thinning down. In this work, fully processed ASICs are used which are thinned from approximately 300 µm to a total thickness of 20 µm and encapsulated using the molding first technique. Section II-A discusses the process of chip embedding and thinning. In Section II-B the test vehicle is presented.



(a) Side view of original (left) and thinned bare die (right).



(b) Edge chipping failure, to be prevented by embedding first technology



(c) Top view (left) and back view (right) of the thinned embedded die.

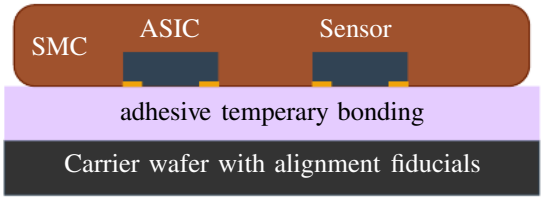
Fig. 2. The microscope images of the transmission line test-structures with 300 µm and 20 µm thickness. In (a) the side view of the original thickness and thinned bare die is shown, and in (b) the edge chipping of the bare die after thinning is shown. in (c) the front side (left) and backside (right) of the embedded die after thinning is shown. The chip size is 0.55 mm × 1.45 mm.

A. Chip Embedding and Thinning Process

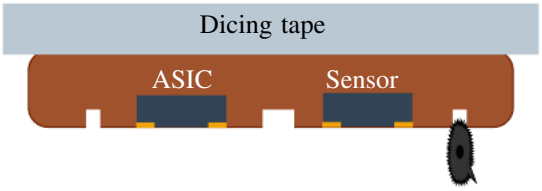
One of the most critical steps in flexible packaging is the thinning of the ASIC. A comparison of the bare test chips before and after thinning is shown in Fig. 2(a). One major issue when thinning silicon die under 50 µm is the damage on the edge due to the mechanical stress on the bare die, as the edge chipping failure shown in Fig. 2(b). In contrast to the back-thinning technology of the entire wafer, embedding first technology is developed and evaluated here for a small amount and application-specific process. Embedding of the die in a sheet mold compound (SMC) before thinning effectively protects the die from edge chipping and warpage. SMC is the molding material in pre-preg shape. It has good fluidity and can realize the molding of complex structures, with low thermal conductivity, and good corrosion resistance [22]. The microscope image of the embedded die is shown in Fig. 2(c).

In the following, the suggested process flow for thinning of an embedded die is shown in Fig. 3 and explained in detail. The main idea is to embed both the ASIC and the sensor in SMC, then thin them down simultaneously. As a lab-based process that was developed on purpose, this embedding first technology is not designed for large-scale manufacturing.

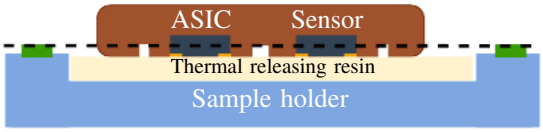
In the first step of the process Fig. 3(a), the ASIC and sensor are placed on a temporary adhesive tape and embedded in SMC on a hot plate with a defined temperature profile [23].



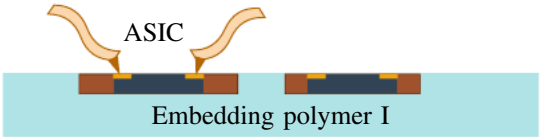
(a) ASIC and sensor embedding.



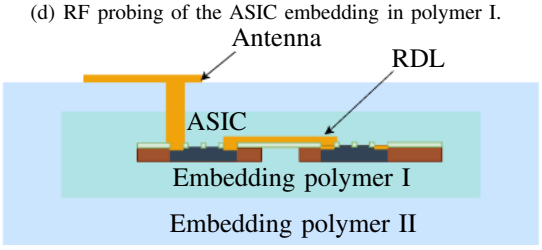
(b) Pre-cut before thinning.



(c) Thinning process with a sample holder.



(d) RF probing of the ASIC embedding in polymer I.

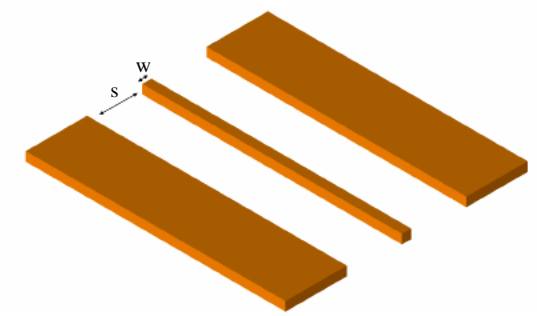


(e) Structuring and embedding in polymer II.

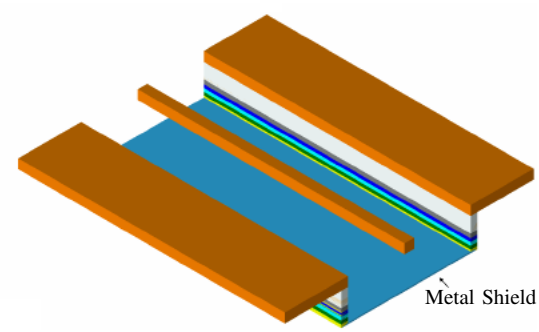
Fig. 3. Proposed process flow of chip embedding and thinning: (a) Chip embedding in SMC with accurate die placement on temporary adhesive tape, (b) pre-dicing before grinding, (c) thinning of the embedded ASIC and sensor with pre-cut marks, (d) characterization of thinned and embedded ASIC, (e) embedding in polymer II and dielectric structuring and metallization.

Alignment marks were used during the placement as the front of both the ASIC and the sensor must be aligned by means of distance and angle.

After the hard cure of SMC, a pre-cut of 20 µm trench depth on these embedded devices at the front side was made by a dicing saw to indicate the final thickness of the chips. In the next step Fig. 3(c), the backside thinning process is done on a mechanical grinder. To do this, the embedded node is detached from the temporary dicing tape and attached to a sample holder using thermal-releasing resin as a temporary bonding layer. In addition, a ceramic spacer (shown in green) is placed on the outer edges of the sample holder to prevent tilting and allow for more homogeneous thinning to the desired thickness. The grinding papers with abrasive particles size from 20 µm to 1 µm were used to make gradual thinning without cracking



(a) CPW



(b) G-CPW

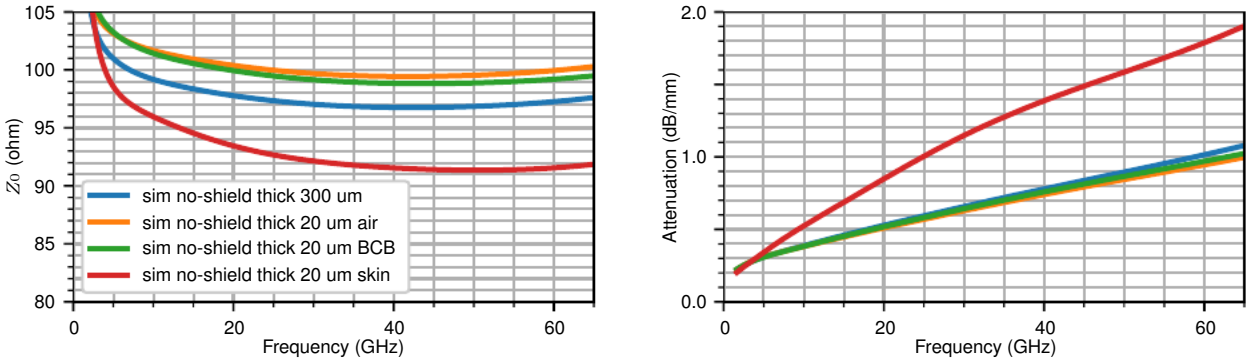
Fig. 4. Sketch of (a) coplanar waveguide (CPW) and (b) grounded coplanar waveguide (G-CPW) transmission line with signal conductor width w and side wall spacing s.

the chip. After each step, the complete removal of the spiral grinding track is inspected under a microscope. The grinding process continues until the pre-cut trenches are visible from the backside. The final polishing step is then performed with the VibroMet vibratory polisher to minimize any remaining micro damage. This produces a stress-reduced surface without the need for the hazardous electrolytes required by electropolishers. Then ASIC and sensor are released from the sample holder and cleaned with acetone.

To validate the effect of thinning and embedding, the RF characteristics of these structures are analyzed by on-wafer S-parameter measurements as indicated in Fig. 3(d), before further processing. The measurement procedure and results are discussed in Section III.

Next, the sample is ready for further flexible embedding and metallization processes. In [24] the DC characterization for the proposed RDL structures is presented. Recent simulation results demonstrate that embedding in the neutral bending plane of a flexible system further reduces the mechanical stress on the chip effectively [25]. To embed these devices in flexible embedding polymer I and II, the elements are precisely placed on an adhesive tape with the top side down, and the liquid state polymer is poured from the back side, then cured with UV exposure. A subsequent semi-additive fan-out Cu-RDL structuring realizes the direct contacts to the embedded chips and connects to through mold via (TMV) to the antenna as the complete system shown in Fig. 3(e).

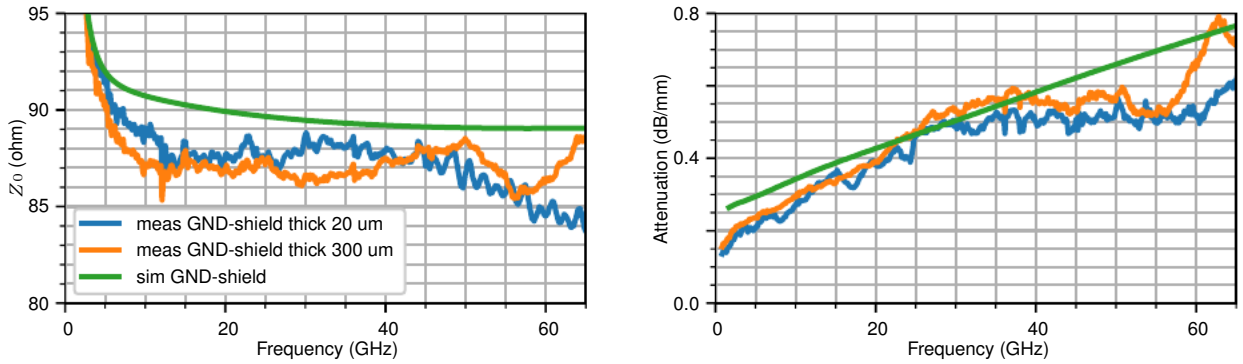
The embedding materials provide step stiffness. After hard cure, SMC has Young's modulus of 24.2 GPa, which protects



(a) Characteristic impedance Z_0.

(b) Attenuation.

Fig. 5. Simulated characteristic impedance Z_0 and attenuation of a CPW transmission line without ground (GND)-shield for 300 µm and 20 µm substrate thickness with different materials underneath the thinned transmission line.



(a) Characteristic impedance Z_0.

(b) Attenuation.

Fig. 6. Measured and simulated characteristic impedance Z_0 and attenuation of a transmission line with the ground (GND)-shield for 300 µm and 20 µm substrate thickness.

the chips with higher stiffness, and also reduces mechanical stress in the interconnect structures between the RDL and the device, resulting in increased reliability. As a unit, the tactile node is encapsulated in two different types of polymer. Polymer I is polyimide, it is an excellent dielectric material with Young's modulus of 8.5 GPa. While polymer II is a flexible resin with Young's modulus of 13 MPa. It is believed, the different stiffness properties create a gradient so that the bending stress is released gradually. The Young's modulus of bulky silicon with the orientation of [110] is 168 GPa, while the thinned silicon has the mechanical strength of 3 GPa [26]. With the active thinned chip sitting in the neutral bending plane, recent simulation results demonstrate that it further reduces the mechanical stress on the chip in a flexible system effectively [25]. Therefore, SMC provides sufficient stiffness within the tactile node just surrounding the ASIC, and the metallization structures of the RDL see less stress while in a bent state.

B. Test vehicle

A typical ASIC consists of passive and active components. For a better understanding of any performance change after chip embedding and thinning, it is important to investigate active and passive components separately. At mmWave frequencies transmission lines are typically used for impedance matching and connections between circuits and pads. Thus, for the characterization of any active component transmission lines are typically involved and their effects can be de-embedded later on. Therefore, this work focuses on the characterization of thinned transmission lines while thinned active components will be subject to future research. A cross-section of a coplanar waveguide (CPW) is shown in Fig. 4(a) with signal conductor width w and side wall spacing s. Compared to microstrip lines the ground metal of CPWs is alongside the signal conductor instead of underneath it [27]. When thinning a CPW the characteristic impedance Z_0 and attenuation of the line change depending on the material underneath the line. Thus, these two parameters are chosen for representing the RF performance of the ASIC.

Fig. 5(a) shows the simulated Z_0 for a thick and thinned CPW while Fig. 5(b) depicts the attenuation of the lines, respectively. In the case of the 20 µm thick CPW different materials were placed underneath it. With air underneath, the highest Z_0 and lowest attenuation can be observed. A 300 µm

thick layer of BCB as a high-quality dielectric material with a permittivity ϵ_r of 2.65 [28] underneath the transmission line results in similar characteristics compared to air. When simulating the transmission line on top of a human body model according to [29], Z_0 deviates by less than 5 % compared to the 300 µm thick version. However, the attenuation of the thinned line on the human body at 60 GHz is 0.8 dB/mm higher than the attenuation of the thick line without a ground shield. This deviation increases with frequency and might degrade the performance of ASICs operating at mmWave frequencies significantly.

As a result, we suggest having a metal ground layer under the signal conductor for thinned transmission lines as shown in Fig. 4(b) shielding the line from the substrate. Such a line is called a grounded coplanar waveguide (G-CPW). As a proof of concept, the BEOL chip with several G-CPW lines of different lengths and a characteristic impedance Z_0 of 90 Ω is used to characterize the RF performance. Measurements are made before and after embedding and thinning, allowing a comparison of both performances. The length of the G-CPW lines ranges from 500 µm to 100 µm, as shown in the photo of the chip in Fig. 2(a).

III. Characterization and Discussion

Thinning of the ASIC for flexible packaging is critical not only because of the fragile mechanical properties of the ultra-thin silicon chip but also because the performance of mmWave components is sensitive to the material properties influenced by the thinning process. Embedding the ASIC in the SMC before thinning reduces the mechanical stress on the die and effectively protects the die from edge chipping and warpage. However, it introduces thermal stress to the components. On the other hand, the molding material SMC has good under-filling properties, and there is a risk of covering the contacting pads during the molding process. Thus, the topography of the die is designed in a way that a line with an oxidation layer is at the highest plane at the edge of the die. During the molding process, it has direct contact with the adhesive layer and prevents the SMC from under-filling the test structures successfully.

To characterize the RF performance Z_0 and attenuation are calculated from on-wafer S-parameter measurements according to [30]. The measurements were performed by a vector network analyzer from 20 MHz up to 65 GHz. Characterizing flexible circuits at mmWave frequencies in the bent state is challenging because conventional methods such as on-wafer probing are not feasible without dedicated measurement equipment and are therefore content for some future research. The pads were de-embedded by measuring two identical lines with different lengths, 500 µm and 100 µm, using the method proposed in [31]. The resulting characteristics correspond to a line with an effective length of 400 µm without pads.

Fig. 6(a) shows measured and simulated Z_0 for a thick and thinned G-CPW while Fig. 6(b) depicts the attenuation of the lines, respectively. It can be observed that despite the thermal stress and mechanical stress introduced by the embedding and thinning processes, it has no effect on both characteristics. This ensures well-defined characteristics independent of the underlying material and shows the feasibility of applying the embedding first technology for mmWave components.

IV. Conclusion

As an important part of the flexible packaging of tactile nodes, thinning processes of chips representing ASIC and sensors as tactile nodes were carried out successfully with embedding first technology to prevent edge chipping. The transmission characteristics of the G-CPW transmission lines were measured before and after thinning. The results show the assessed RF performance characteristics did not degrade through the process flow, it shows the feasibility of the examined embedding and thinning processes is suitable also for mmWave components. As for future work, the RF performance of thinned active components with semi-additive Cu-RDL at the deformed state is yet to be investigated. Furthermore, the mechanical and thermo-mechanical reliability, e.g. through bending cycles.

Acknowledgment

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