Research of Chip Placement Accuracy for Fan-Out WLP using A Novel Self-Assembly Stage

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***Abstract*—This paper discusses the alignment accuracy after self-assembly using a novel self-assembly method with a uniquely developed porous stage. In a preceding paper, we have introduced our process that combines tape expansion technology and self-assembly technology. By using this process and machine device, it is possible to significantly improve the throughput of pick and place process for FO-WLP. Furthermore, it is indicated that our self-assembly method using the porous chuck stage enables achievement of high precision chip alignment and high throughput. In this study, two factors are evaluated to clarify the impact on the chip accuracy after self-assembly; 1) the influence of chip position before self-assembly, 2) the relationship between stage size of self-assembly area and chip size. As a result of evaluation, if the chip size is the same as the porous stage size, the alignment accuracy after self-assembly is within 5 µm or less even with varied chip positions before self-assembly. On the other hand, when the porous stage size and chip size are different, the chip position before self-assembly has an impact on the alignment accuracy after self-assembly. Based on the results obtained in this study, further development of machine device and process will be pursued to improve the alignment accuracy after self-assembly.**

Keywords- FO-WLP; pick-up and place; tape expansion; self-assembly;

I. INTRODUCTION

Die attach is also commonly known in the semiconductor industry as die bonding or die mount. It is the process of attaching a silicon chip to a substrate or package. This process is an essential for creating a reliable electrical and mechanical connection between the chip and the rest of the electronic devices. Various precision die attach equipment are used to accurately pick and place the chip onto the substrate. These devices are an essential tool in semiconductor backend process, but it faces challenges in terms of throughput. In order to solve this problem, the self-assembly technology has the potential to address the throughput problem associated with traditional pick and place assembly process. Self-assembly technology is known for higher placement accuracy process using liquid surface tension and it has long been reported in the field of semiconductor devices. In 2005, Fukushima *et al*., demonstrated self-assembly technique for the first time to apply for 3D integration [1]. They have employed self-assembly technologies for advanced chip-to-wafer 3D integration [2] [3]. CEA-LETI has been working since several years on self-assembly process. Recently, they have demonstrated collective D2W direct bonding self-assembly process [4] [5]. These previous papers mainly reported on the method of self-assembly technique. Although there have been previous papers on self-assembly technique, there have been no papers on process or devices specifically applying self-assembly technique. In 2021, we have introduced for the first time our novel process that combines tape expansion technology and self-assembly technology [6]. Our proposal process flow is illustrated in Figure 1. There are two parts basically, one is tape expansion and the other is self-assembly. Figure 2 shows the photograph of tape expansion process. We have developed the tape expansion machine device with a function allowing that tape can be expanded in four directions individually [7]. To achieve precise alignment after tape expansion, we have developed our own self-assembly technique using a novel porous stage. Our unique self-assembly process is illustrated in Figure 3. Generally, self-assembly technique uses a supporting wafer which surface is formed with hydrophilic and hydrophobic area. This process enables high precision alignment, but throughput is a challenge due to the required steps of liquid dropping before self-assembly and liquid drying after self-assembly. On the other hand, our method performs liquid supply and recovery through the porous stage. Due to the elimination of liquid dropping step and liquid drying step, our method enables high throughput. We have confirmed that it is possible to achieve high precision chip alignment through self-assembly using our novel porous stage (see Figure 4).

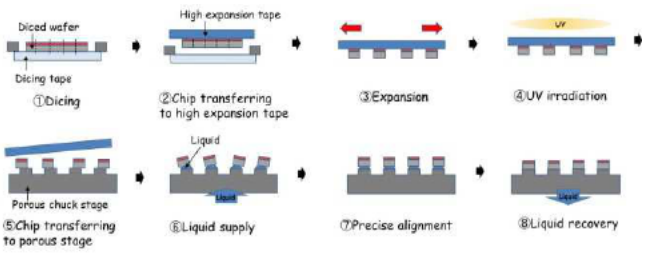


Figure 1. A novel chip placement process using tape expansion technology and self-assembly technology.

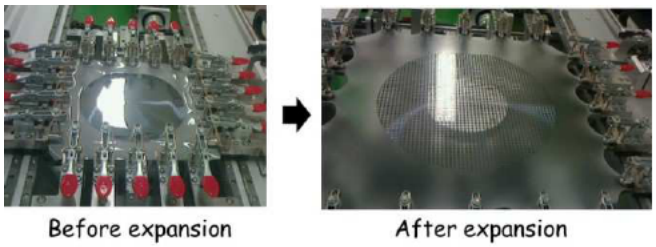


Figure 2. Before and after photos of tape expansion.

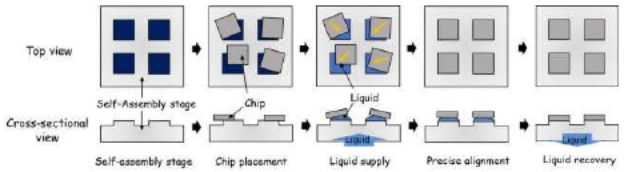


Figure 3. Self-assembly process using a novel porous stage.

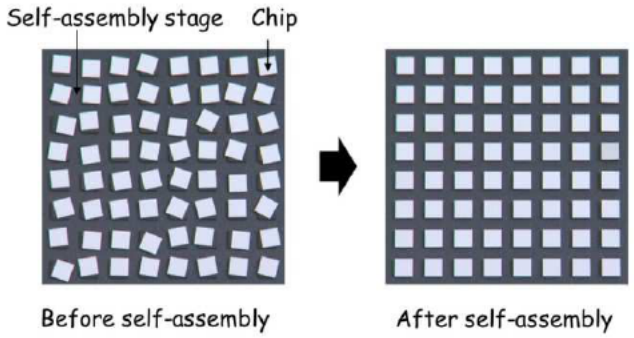


Figure 4. Before and after photos of self-assembly using a novel porous stage.

We are initially proposing this process for FO-WLP applications. One of the highest cost manufacturing process for FO-WLP is pick and place process. To reduce the process cost, pick and place equipment try to provide the high productivity machines [8]. However, since the conventional pick and place process is a one chip at a time process, it is difficult to improve the throughput dramatically. Figure 5 shows the comparison of throughput between our novel chip placement device and conventional pick and place device. Throughput comparison is performed under following conditions; WPH of our device is 15 wafer which size is 8 inch, CPH of pick and place device is 20K chips. As shown in Figure 5, a significant advantage of our device is its remarkably higher throughput compared to conventional device. Since our process is designed to manufacture based on wafer size, it is possible to produce 15 wafer per hour regardless of chip size. On the other hand, since the porous chuck stage is still in the prototype stage, there are remaining challenges regarding alignment accuracy. In this study, two factors are evaluated to clarify the impact on the alignment accuracy after self-assembly, 1) the influence of chip position before self-assembly, 2) the relationship between stage size of self-assembly area and chip size.

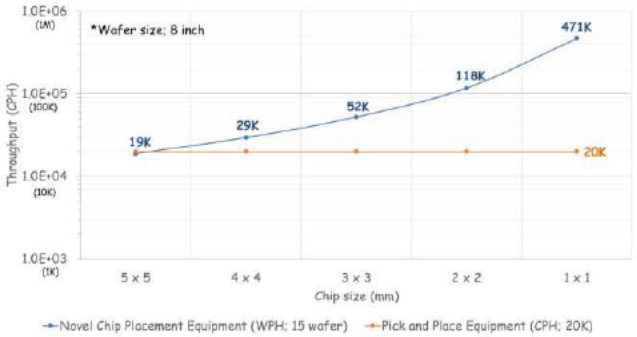


Figure 5. Comparison of throughput between a novel chip placement device and conventional pick and place device.

II. EXPERIMENTAL AND RESULTS

A. Evaluation method of self-assembly

First, a porous stage with the following specifications is prepared for this study; self-assembly area size of 3 mm square and the distance between self-assembly areas is 2 mm. Evaluation method of self-assembly is illustrated in Figure 6. Chip is randomly placed on the porous stage, allowing it to extend beyond its edges. Then, the distance between the center of chip and the center of stage is measured with CNC vision measuring system (Mitutoyo Corporation; Quick Vision ACCEL) and its distance is defined as the misalignment distance. Liquid is supplied through the porous stage until it reaches the surface of the stage and chip is precisely aligned by liquid surface tension. Water is used as the liquid for self-assembly in this study. After chip is aligned, liquid is recovered through the porous stage. Then, the distance between the center of chip and the center of stage is measured with CNC vision measuring system again.

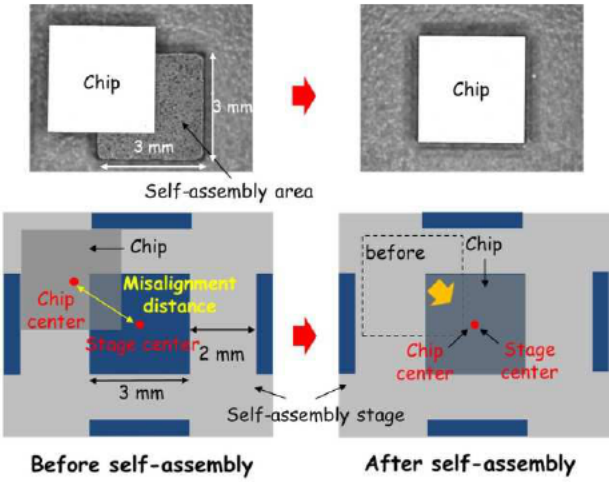


Figure 6. Evaluation method of self-assembly.

B. Influence of chip position before self-assembly

In this section, we evaluated the influence of the chip position before self-assembly on the alignment accuracy after self-assembly. We prepared chips with size of 3 mm

square and thickness of 350 μm for this evaluation. As shown in Figure 7, the chip positions before self-assembly are divided into four areas; 1) 501~1,000 μm, 2) 1,001~1,500 μm, 3) 1,501~2,000 μm, 4) 2,001~2,500 μm. Each chip in four areas are aligned by self-assembly and the alignment accuracy is measured as described in paragraph A. Figure 8 shows the result of alignment accuracy after self-assembly. Chip alignment is possible even when the chip is placed in other area, as long as the chip has a large contact area with target location of self-assembly. Furthermore, regardless of the initial chip position, the alignment accuracy after self-assembly shows a median value of 5 μm or less. As indicated by the evaluation results, high precision chip alignment is achievable regardless of the chip position before self-assembly, as long as the chip size is the same as the porous stage size.

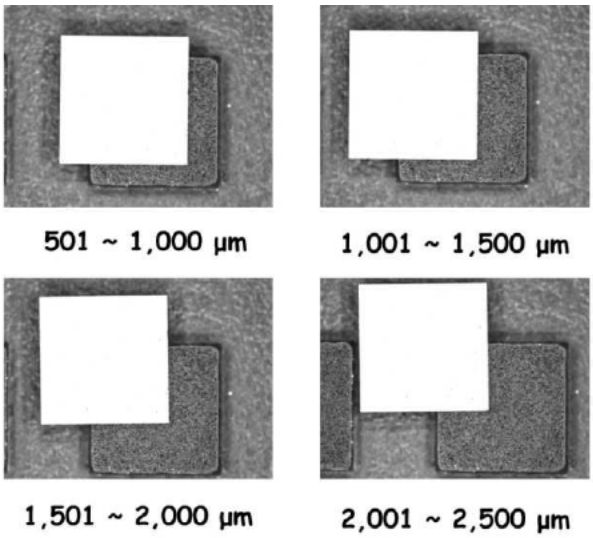


Figure 7. Photos of chips with different positions before self-assembly.

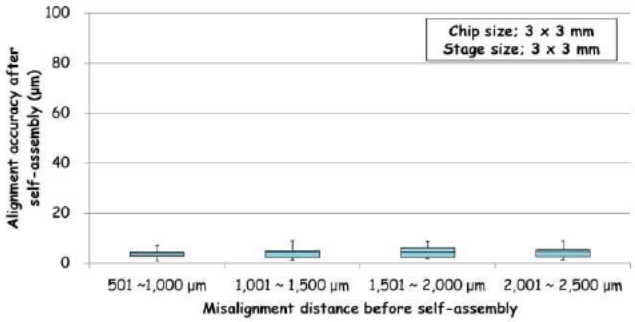


Figure 8. Alignment accuracy after self-assembly with different misalignment distances.

C. *Relationship between stage size and chip size*

In this section, we evaluated the influence of relationship between stage size of self-assembly area and chip size. We prepared seven different chip sizes; 2.7 mm, 2,8 mm, 2,9 mm, 3.0 mm, 3.1mm, 3.2 mm and 3.3 mm, all chips were square in shape. Before self-assembly, the chips are randomly positioned to surround the stage in 360-degree arrangement. Misalignment distance before self-assembly is below 1,200 μm for this evaluation. Evaluation result shows in Figure 9 and 10. When the chip size is 3 mm square, the alignment accuracy shows a median value of 3 μm. As the chip size becomes smaller, the alignment accuracy becomes lower. For the chip size of 2.7 mm square, the alignment accuracy shows a median value of 120 μm. As the chip size becomes larger, the alignment accuracy becomes lower as well. However, the alignment accuracy is still better compared to when the chip size is smaller. For the chip size of 3.3 mm square, the alignment accuracy shows a median value of 37 μm. From these results, it is indicated that when the stage size and chip size are different, the alignment accuracy becomes lower. Particularly, when the chip size becomes smaller, this tendency becomes more pronounced.

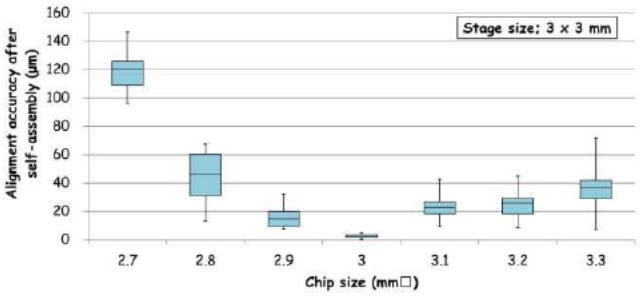


Figure 9. Alignment accuracy after self-assembly with different chip sizes.

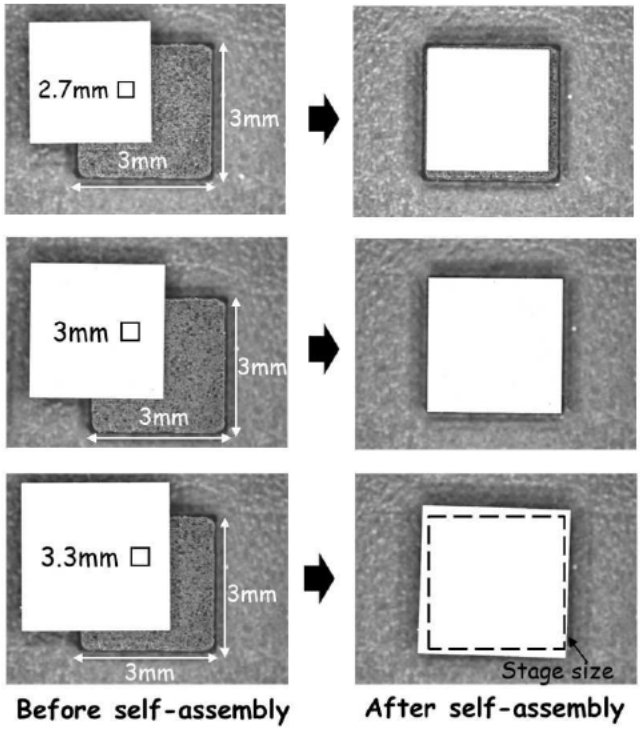
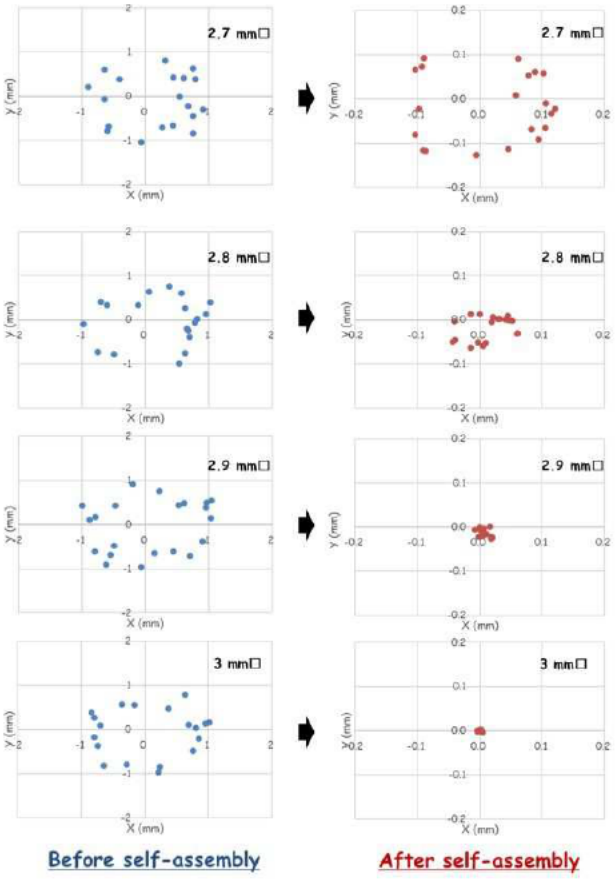


Figure 10. Before and after photos of self-assembly with different chip sizes.

III. Discussion

As I stated above, when the stage size and the chip size are different, the alignment accuracy becomes lower. This tendency becomes more pronounced when the chip size is smaller. The question we have to consider is why the chip size affects the alignment accuracy after self-assembly. To clarify the reason, the positions of chips before and after self-assembly are plotted in Figure 11. The chips after self-assembly align around the center of stage when the chip size is 3 mm square. On the other hand, the chips after self-assembly tend to move away from the center of stage when the chip size differs from the stage size. Furthermore, as the chip size becomes smaller, the positions of the chips move even further away from the center. For further analysis, the positions of chips before and after self-assembly are compared. Although the distance from the center may vary before and after self-assembly, the overall trend of chip placement remains the same. Based on these results, it can be concluded that when the stage size and chip size are different, the initial position of the chip before self-assembly has an impact on the alignment accuracy after self-assembly.



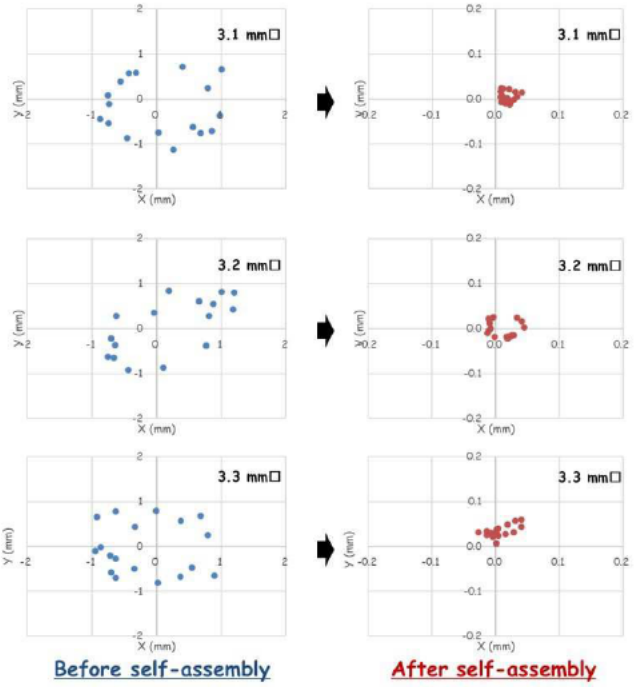


Figure 11. Chip positions before and after self-assembly with different chip sizes.

To discuss the reason why the position of the chip before self-assembly has an impact on the alignment accuracy, the movement of chips during self-assembly is illustrated in Figure 12. Chips are capable of moving due to the surface tension of liquid even when the chip size is changed. However, when the stage size and chip size are different, the chips come into contact with the corner of the stage during movement and then unable to continue moving. The evaluation results for chip size of 2.7 mm square and 3.3 mm square with different initial chip positions before self-assembly are presented in Figure 13 and 14. Looking at the photographs after self-assembly, it can be observed that both sizes of chips are stopped at the corners of the stage. Additionally, it can be observed that the corners of the stage where the chips come to stop vary depending on the initial positions of the chips before self-assembly. This tendency is particularly strong in chip size of 2.7 mm square. With 3.3 mm square chip, a similar tendency can be observed where the chip stops at the corners of the stage. However, there is a possibility of chip tilting after self-assembly due to the chip being larger than the stage. Based on these results, the following measures are necessary; 1) adjusting the dimensions and shape of the stage to accommodate different chip size, 2) to further enhance the tape expansion technique for controlling the initial chip positions of self-assembly.

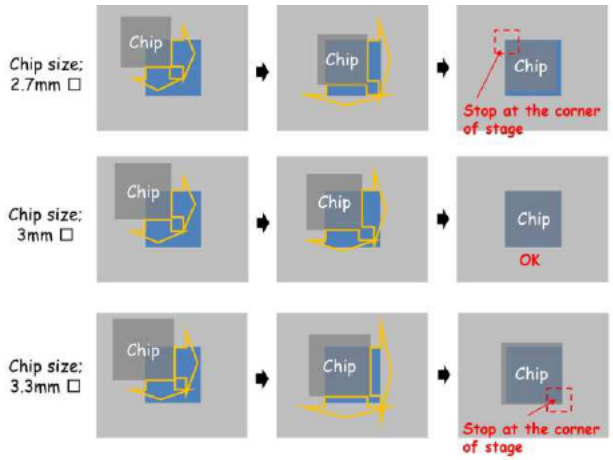


Figure 12. Movement of chips during self-assembly with different chip sizes.

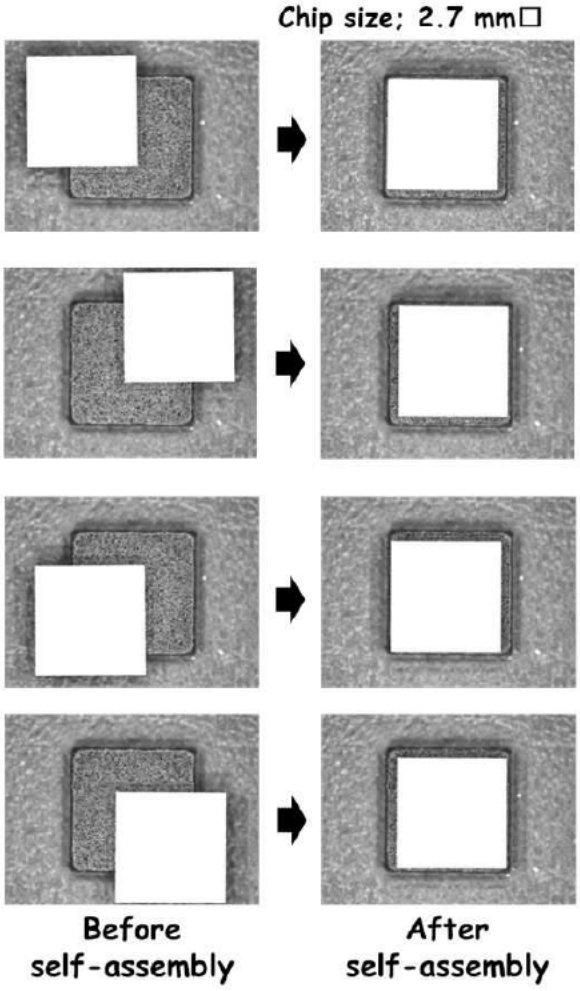


Figure 13. Before and after photos of self-assembly with different initial chip positions with the chip size of 2.7 mm square.

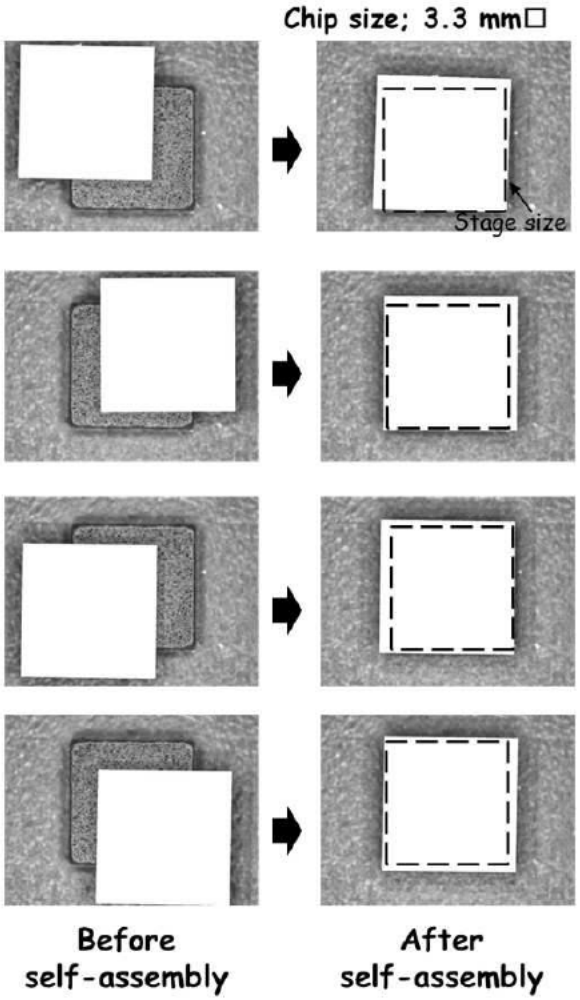


Figure 14. Before and after photos of self-assembly with different initial chip positions with the chip size of 3.3 mm square.

IV. Conclusion

In order to improve the throughput of Fan-out WLP process, we have developed the machine device that incorporates a unique self-assembly method. In this study, two factors are evaluated to clarify the impact on the alignment accuracy after self-assembly; 1) the influence of chip position before self-assembly, 2) the relationship between stage size of self-assembly area and chip size. As a result of evaluation, if the chip size is the same as the porous stage size, the alignment accuracy after self-assembly is within 5 μm or less even with varied chip positions before self-assembly. On the other hand, when the porous stage size and chip size are different, the chip position before self-assembly has an impact on the alignment accuracy after self-assembly. Based on the results obtained in this study, further development of machine device and process will be pursued to improve the alignment accuracy after self-assembly.

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