Thickness effect of copper clips on power module packaging design

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***Abstract*—The superior switching performance of SiC MOSFETs compared to Si devices is limited by packaging-related issues. High electromagnetic parasitics which lead to high voltage overshoots, and higher power losses are the main challenges of high frequency operation. Hence, packaging design modification and optimisation are necessary to accommodate faster switching. Copper clips replacing the bonding wires show promising results in reducing stray inductances, while enhancing the current conduction and heat dissipation since the clip are in contact with a larger area of the semiconductor chip. Silver sintering instead of soldering further improves the electrothermal behaviour. This paper investigates numerically various thicknesses of the copper clips and their effect on double-sided silver sintering, half-bridge 1200V/400A SiC MOSFET power module. Moreover, the silver layer thickness is varied to reduce the maximum stresses on the chip - silver interface.**

***Index Terms*—SiC MOSFETs, copper clips, parasitic inductance, thermal stress**

I. Introduction

The decarbonisation of the transport section with the widespread adoption of electric vehicles (EVs) has led to more stringent requirements for power electronic converter technologies. Power electronic converters are crucial to the EV operation and are used as rectifiers for battery charging and as inverters for motor drivers.

At system level, the power electronics voltage rating and the power requirements are increasing as the battery DC level is increasing towards 800V, or even higher in the future. This trend aims to achieve higher system efficiency, higher mile autonomy, at a smaller system footprint. Further, to achieve charging duration of several minutes (<30mins), DC fast chargers are pushed towards hundreds of kWs. At a power electronic module level, to supply the higher load demands, power modules tend to use higher switching frequencies which are currently in the range of tens of kHz, with a potential to reach hundreds of kHz in the future.

Currently, most of the EVs use Si-based technologies such as Si insulated gate bipolar transistor (IGBT). However, conventional Si IGBT-based technologies have material limitations at higher operating frequencies and higher operating temperatures. There is an ongoing trend of EV companies to replace Si IGBT power modules with advanced SiC MOSFETs modules. SiC has 10 times higher dielectric breakdown voltage and 3 times higher thermal conductivity than Si. Further, SiC's bandgap is 3.3eV for 4-H SiC structures, which enables higher temperature operation. Moreover, SiC devices have low junction capacitance and gate charge, which allows for higher switching frequency. As unipolar devices, MOSFETs enable even faster switching frequency, thereby reducing the size of the whole system and increasing power density [1].

However, higher switching frequencies lead to higher di/dt, which combined with high parasitic inductances cause higher voltage overshoots, increased heat power losses, and increased electromagnetic interference (EMI) [2]. Even though the switching frequency is an operating parameter that can be changed, the parasitic inductances are inherent in electrical circuits and are subject to the power module design. Further, due to the miniaturisation of the SiC MOSFET chips, thermal issues rise due to the higher power density and subsequent high and localised heat fluxes. Therefore, the commercial packaging designs need to consider the implications that rise at higher switching frequencies from both the electromagnetic and the thermal perspective.

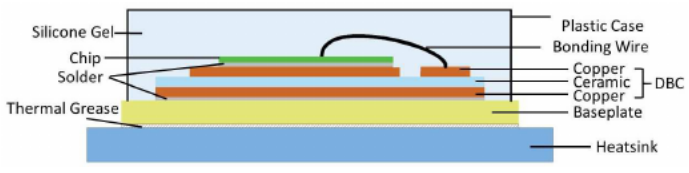

Fig. 1. Traditional power module packaging structure.

The traditional structure of a power module consists of 7 layers, Fig. 1. The semiconductor chips are soldered on

top of Direct-Bonded-Copper (DBC) substrates. The top side copper of the DBC is used for the electrical connections that carry the current, the DBC ceramic is used for electrical insulation between the current conducting parts and the rest of the package. The bottom DBC copper is soldered to a metallic baseplate to provide mechanical support and enable heat dissipation and connection with external cooling solutions such as water heatsinks or air fans. Aluminium wires are used to link the power terminals with the chips. A plastic case surrounds the package, and is filled with a dielectric material such as silicone gel or epoxy to provide electrical insulation and protection against harmful environment such as humidity and dust.

Wire bonding is the most widely adopted method for electrical interconnections due to its low-cost, flexibility, and established assembly infrastructure. However, the bonding wires are usually thin aluminium wires and cause a long current path to provide enough height and space for the connection, which results in very high parasitic inductance. Further, due to the small diameter of the bonding wires, many wire connections are required to achieve higher current levels, lower on-state resistance and increased power density; resulting in productivity, material cost and reliability issues. Large number of wires cause accumulation of current and heat on the contact points. The higher temperature on the contact points could lead to wire bond degradation or even lift-off, which would result in uneven distribution of the current through the remaining wires. Moreover, as the total area of the chip is shrinking with SiC technology, and for increased current rating modules with multiple wires bonded on the SiC MOSFET's source, the reliability of the wires decreases at high switching frequencies due to the increased heat power losses [3].

Practical realisation of high-temperature operation of power modules is also restricted by the rest of the packaging materials. The interface materials are usually tin-lead or led-free solder alloys, which have relatively low melting points. Considering the higher heat fluxes and elevated temperature of a package at higher frequency operation, these interface materials might degrade over time, thus decreasing the life-time of the device. The thermal stresses that are generated during operation in the multiple layers of the power modules vary according to their material properties. The mismatch between the coefficient of thermal expansion of adjacent layers causes increased stresses and increased degradation during temperature cycling. These stresses are exacerbated during high frequency operation due to the faster power cycling. Often power module failure mechanisms associated with temperature cycling include wire bond lift-off, solder degradation and cracking, semiconductor die cracking [4].

To this end, advanced packaging designs with lower parasitic inductance and capable of continuous operation at higher temperatures should be explored to enable higher switching frequency operation of SiC MOSFET modules to meet the EV application power demands. Innovative interconnection methods such as wire bondless structures using directly deposited copper or copper clip connection, flexible PCB connection, novel 3D layouts, and component integration have been proposed in literature to reduce the parasitic inductances [5]. To enhance the thermal performance of package, new interconnection methods are used to reduce thermal resistance, such as welding or sintering multiple copper pillars to the mold metal, using a lead frame to increase the contact area. To achieve high temperature working capability, new materials and innovative methods to replace traditional soldering have been proposed. For instance, gold alloy solders such as eutectic AuSn have been used in small mold conditions [6]. Silver sintering has been proposed due to its high melting point (961°C). It also has high thermal and electrical conductivity, high temperature reliability, and the sintering process takes places in relatively low temperatures.

In this paper, copper clips are adopted as interconnections replacing the bonding wires. Double-sided silver sintering is proposed as bonding method for die and copper clip attachment. Copper clips offer many advantages compared with bonding wires. Copper clips enable larger contact area for current conduction, which results in lower parasitic inductances, lower contact resistance, lower thermal resistance, and more uniform heat dissipation. However, introducing a copper layer on top of the SiC chip would result in thermal stresses during operation [7]. This study analyses the electromagnetic, thermal, and thermomechanical effect for various thicknesses of copper clips to optimise the performance of the SiC MOSFET power module. Therefore, the copper clip geometric and thickness need to be carefully selected so that the thermal stresses generated during operation do not outweight the electrical and thermal advantages of copper clips. The design under investigation, Fig. 2, is a 1200V/400A MOSFET half-bridge introduced in [8].

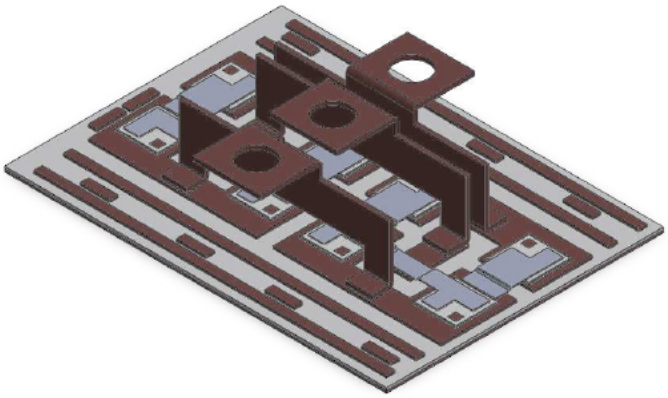

Fig. 2. Half-bridge structure under investigation.

II. Electromagnetic Performance Analysis

This section analyses the electromagnetic performance of the power module for thicknesses of copper clips ranging from 0.1mm to 1mm. ANSYS Q3D is used to extract the parasitic inductance at various frequencies. The DC links are set to the

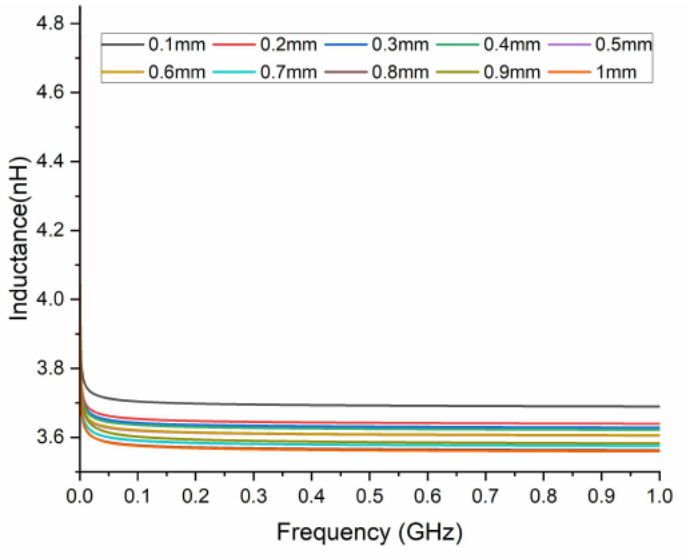

Fig. 3. Total inductance with frequency for various copper clip thicknesses.

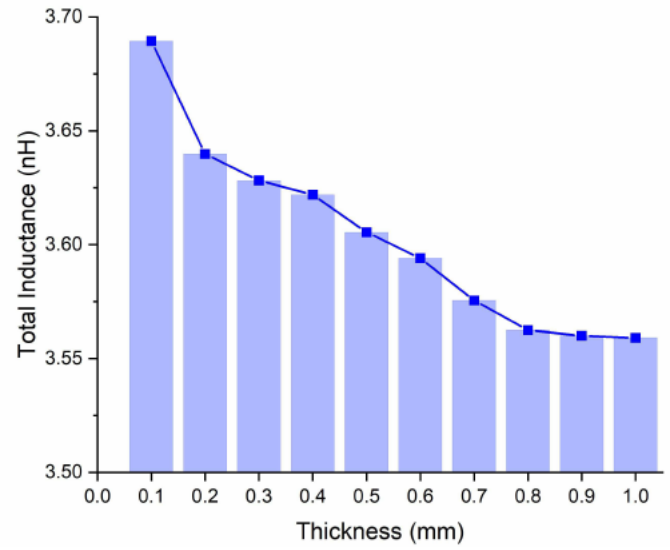

Fig. 4. Total inductance for various copper clip thicknesses at 1GHz.

electric source and sink, respectively, and the total parasitic inductance is calculated.

The inductance decreases with frequency according to the skin effect [**?**] Fig. 3, with maximum inductance at DC point. The turn-on and turn-off process time of SiC MOSFETs are usually in the nanosecond or GHz scale. Fig. 4 suggests that at 1GHz, increasing the copper clip thickness from 0.1mm to 1mm, the total inductance decreases slightly, with a total of 0.13nH difference or 3.6% reduction.

III. Thermal Performance Analysis

Replacing the bonding wires with copper clips leads to better current and heat flow paths. The copper clips are in direct contact with a larger area of the SiC MOSFET's source, thus the current and the heat are distributed more evenly.

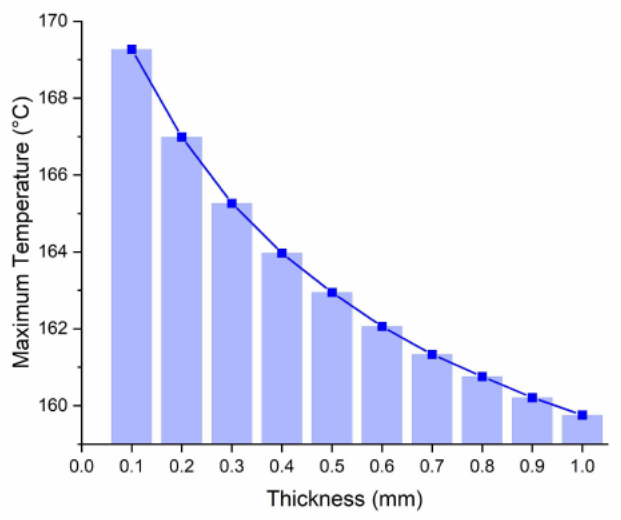

Fig. 5. Maximum junction temperature for various copper clip thicknesses.

Moreover, the localised current and heat accumulation that is often present on the bonding wire - SiC source interface is avoided. To further increase the electrothermal performance, the bond between SiC die and copper clip is realised by silver sintering. Despite the thermal enhancement, the addition of copper clips on the top side of the SiC die induces stresses on the sintered layer and on the SiC die. Therefore, a sensitivity analysis of the copper clip thickness on the thermal and structural performance of the power module is required to find the optimal thickness of copper clips.

A. Junction temperature

To examine the thermal performance of the copper clips for various thicknesses, the SiC MOSFETs are used as heat sources. Since each SiC MOSFET is rated at 100A with a $15m\Omega$ on-state resistance, a total of 150W is dissipated for short-circuit conditions. The copper clip thickness is varied from 0.1mm to 1mm, and the silver sintering layer is set to 25μm. Fig. 5 shows the maximum SiC junction temperature for various copper clip thicknesses at steady state. As the copper clip thickness is increasing, the MOSFET chip's temperature is decreasing; from 169°C to 159 °C for copper clip thicknesses of 0.1mm to 1mm, respectively. Fig. 6 indicates a uniform distribution of temperatures in the semiconductor area.

B. Thermomechanical Analysis

To examine the structural integrity of the structure, a thermomechanical analysis is performed for the range of copper clip thicknesses. The maximum stresses are located on the edge of the chip - silver sintering layer interface. Fig. 7 shows the Von Mises stress distribution for 0.5mm copper clips and 25μm silver layer. Moreover, as the copper clip thickness increases, the maximum thermal stresses increase. For 0.1mm thick copper clips, a maximum stress of 469MPa was calculated, whereas the stresses reach 923MPa for 1mm

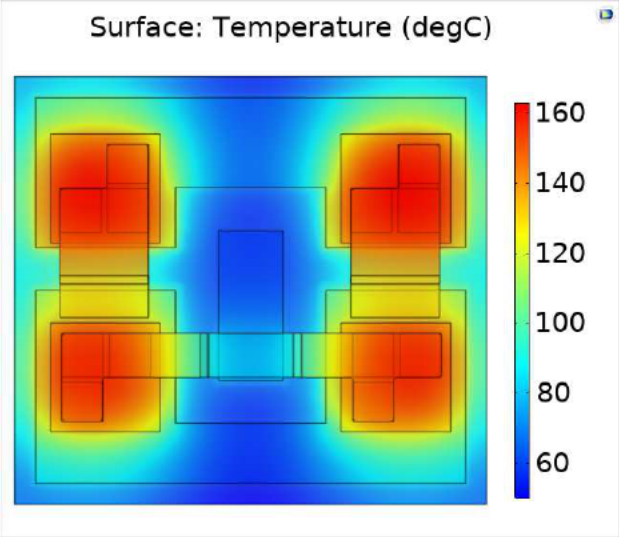

Fig. 6. Temperature distribution of a 0.5mm copper clip design at steady state.

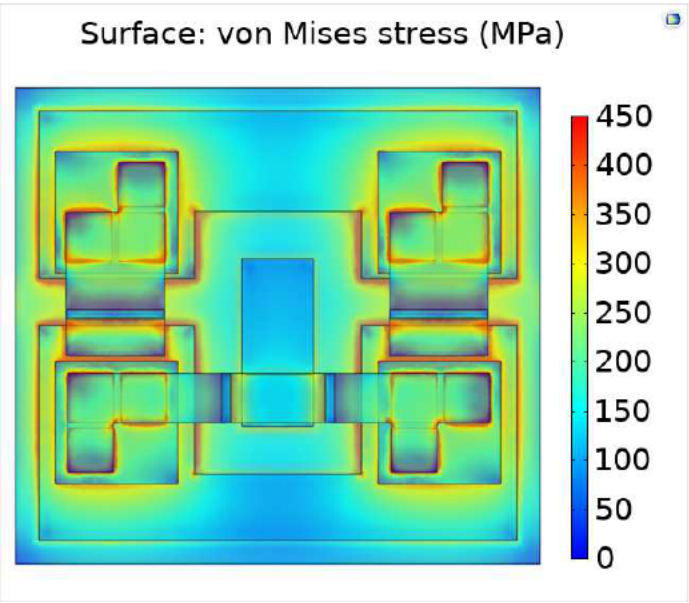

Fig. 7. Maximum thermal stress distribution of a 0.5mm copper clip design at 163°C.

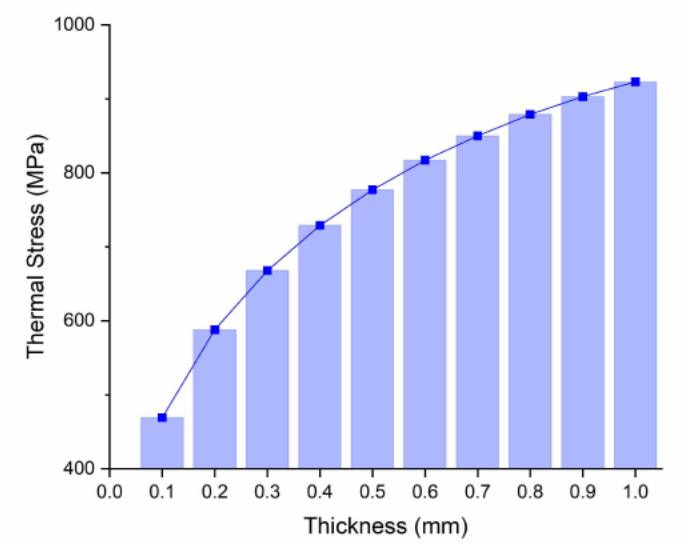

Fig. 8. Maximum thermal stress for various copper clip thicknesses.

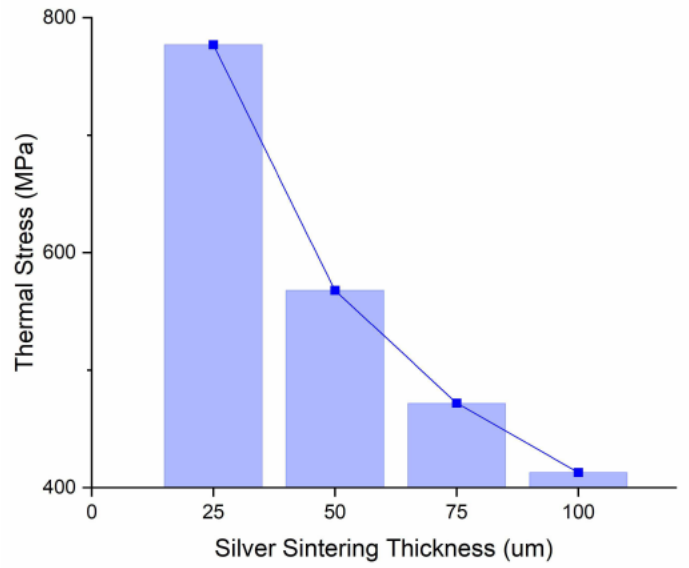

Fig. 9. Maximum thermal stress for various silver thicknesses.

thick copper clips, Fig. 8. Therefore, there is an apparent trade-off between the thermal benefits of using copper clips against the induced thermal stresses. For a 10°C chip temperature reduction, the maximum thermal stresses on the chip - silver interface are doubled.

To further optimise the structure and reduce the thermal stresses, the silver layer thickness could be modified. Fig. 8 demonstrates the maximum thermal stresses of the package for a design with 0.5mm thick copper clips, and silver layers of 25μm, 50μm, 75μm, 100μm. Lower thermal stresses are found for thicker silver layers, with a nearly 50% reduction in the von Mises stresses from 777MPa to 410MPa in the 0.5mm copper clip design. The chip temperature is not affected significantly by introducing thicker silver layers, and remains between 155°C to 155.5°C for the 0.5mm thick copper clip design; hence, suggesting that thicker silver layers could act as stress dampeners whilst maintaining the same thermal performance. The simulation results are summarised in a colourmap which demonstrates the chip temperature and the maximum Von Mises stresses for various copper clip and silver thickness combinations, Fig. 10. Finally, Fig. 11 indicates that the maximum displacement occurs on the copper clip interconnection, where the copper clips are bent. A maximum displacement of 9μm is found, which is less than 2% compared to the 0.5mm thickness of the clip.

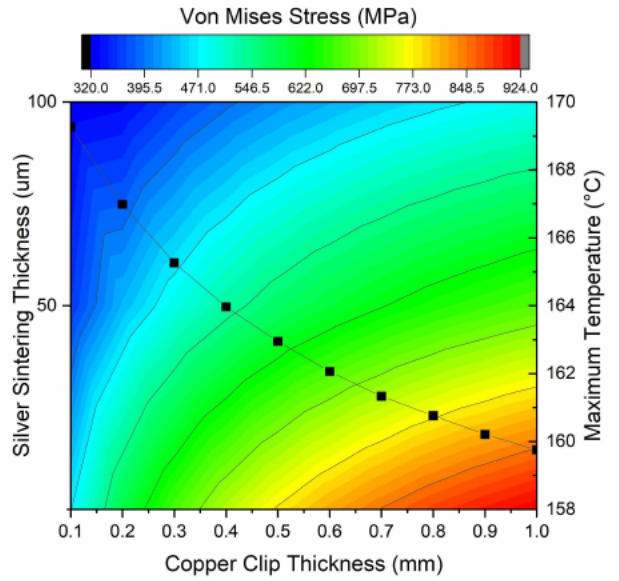

Fig. 10. Thermomechanical performance of the power module for various copper clip and silver thicknesses.

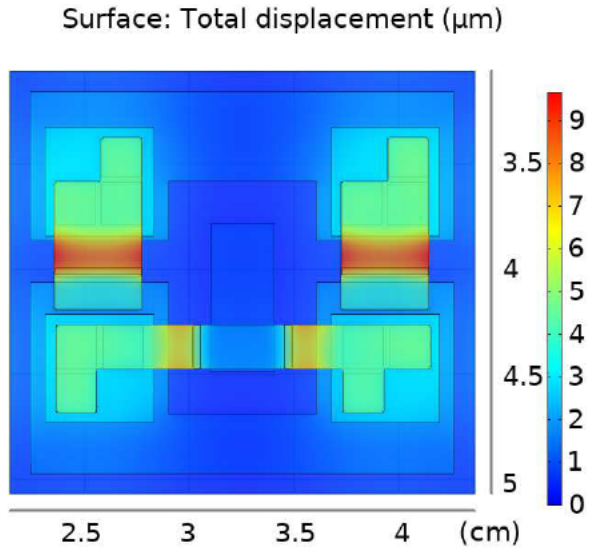

Fig. 11. Total displacement of a 0.5mm copper clip design at 163°C.

IV. Conclusion

Copper clips replace traditional bonding wires to reduce the parasitic inductances and enhance the current and heat conduction. The copper clip bonds are realised by double-sided silver sintering, which further improves the electrothermal behaviour of the power module. This paper investigates the effect of different thicknesses of copper clips and silver layers on the electromagnetic, thermal, and thermomechanical behaviour of a 1200V/400A SiC MOSFET half-bridge power module with four chips in parallel. Results suggest that increasing the thickness of the copper clips results in a minor improvement in parasitic inductances, from 3.69nH to 3.56nH at 1GHz for copper clip thicknesses from 0.1mm to 1mm, respectively. For the same copper clip thickness range, the maximum junction temperature of the SiC MOSFET reduces for thicker copper clips, from 169°C to 159°C. However, as the copper clips become thicker, the thermal stresses are increasing significantly, with Von Mises stresses reaching a maximum of 920MPa on the edge of the chip - silver interface for 1mm thick copper clips. To further optimise the package, the silver layer is increased from an initial thickness of 25μm to 100μm, which resulted in a 50% reduction of stresses, from 777MPa to 410MPa for a 0.5mm copper clip design. The maximum displacement is negligible compared with the copper clip dimensions. The results indicate a trade-off between thermal and thermomechanical behaviour. However, the design should consider the assembly process and the implications that would rise in a practical assembly process of the power module, i.e., the fabrication of very thick preformed copper clips, and the porosity in thick silver sintering layers.

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