Measurement and simulation of mechanical strength of Back-End-Of-Line layer in advanced CMOS dies

Bart Vandevelde
Imec
Leuven, Belgium
bart.vandevelde@imec.be

Riet Labie
Imec
Leuven, Belgium
riet.labie@imec.be

Kris Vanstreels
Imec
Leuven, Belgium
kris.vanstreels@imec.be

Kevin Cox
Tektronix Component Solutions
Beaverton, US
kevin.cox@tektronix.com

Jason Krantz
Tektronix Component Solutions
Beaverton, US
jason.krantz@tektronix.com

Mario Gonzalez
Imec
Leuven, Belgium
mario.gonzalez@imec.be

Reza Moloudi
Imec
Leuven, Belgium
reza.moloudi@imec.be

Matt Borden
Tektronix Component Solutions
Beaverton, US
matt.borden@tektronix.com

***Abstract*— The back-end-of-line (BEOL) layers of ICs are subjected to considerably high mechanical forces during processing and when operating in harsh conditions. Without proper design and flip chip process control, the forces induced from flip chip bumps may exceed the ultimate strength of the BEOL resulting in critical failures. It is therefore of high interest to have a measurement method to quantify the strength of the BEOL structure of a functional IC. Ultimate fracture stress values are extracted from these measurements which can be used in thermo-mechanical simulations of flip chip assemblies for survivability evaluations.**

Keywords—BEOL, thermo-mechanical stress, flip chip assemblies,

I. Thermo-Mechanically Induced Stress Failures in Back End Of Line

Over the last few years, Tektronix Component Solutions has been working to advance package reliability through selecting optimal material sets, using best-in-class simulation methods, and refining processing techniques. In this research, Tektronix partnered with IMEC to establish die strength characterization methods and to evaluate the risk of failure of an advanced node CMOS die in a flip chip package.

Due to temperature changes during processing and in operation, forces and bending moments are induced on the solder joints of flip chip assemblies (Fig. 1). The origin of these forces and moments are the thermal expansion mismatch between the silicon chip (~ 3 ppm/°C) and substrate (~ 14 ppm/C°).

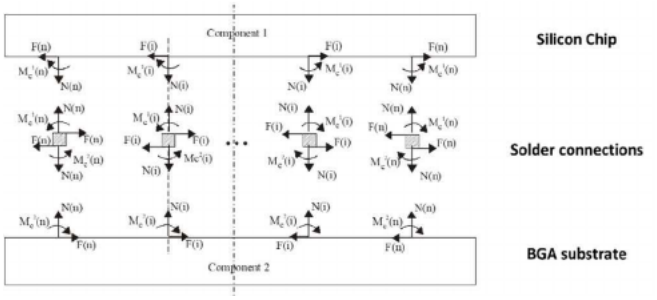

Fig. 1. Schematic drawing of forces and bending moments acting in a flip chip assembly during temperature variations

In reference [1], an analytical model is available which calculates the forces and bending moments acting on solder joints and at the interfaces with chip and substrate. These forces cause the bending of the structure.

The analytical model is based on linear elastic equations, and obviously and luckily, solder joints will deform plastically and by creep which reduces the forces acting on the structure. However, the forces and bending moments are still significant.

In a historical case (not part of the work reported hereafter), fractures in the BEOL were found after flip chip assembly processing. As shown in the scanning acoustic microscopy (SAM) picture in Fig. 2, a lot of so-called “white bumps” [2] are seen which show fracture in the BEOL of silicon die. The cross-section confirms the fracture in the BEOL below the solder bump. On other cross-sections, underfill material was seen in the fracture which indicates that the fractures occurred during the solder flip chip reflow, and before underfilling.

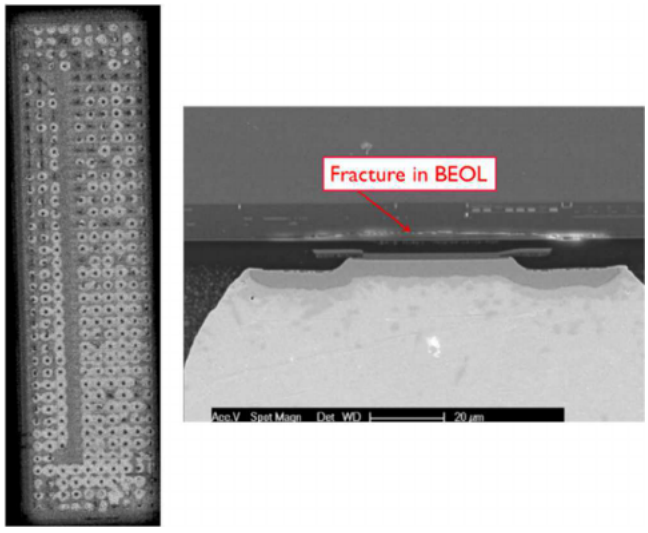

Fig. 2. Left: Scanning Acoustic Measurement (SAM) showing white bumps after flip chip assembly: Right: Cross-section showing the fracture inthe BEOL.

The fractures could be explained very well through calculating the forces and bending moments induced after cooling down from solder reflow temperature down to room temperature. Fig. 3 shows the bending moments and forces for three flip chip assemblies. It was seen that the bending moments were largest when there was a large pitch between the solder joints. This was more important than the size of the chip. This was also confirmed in the processing tests.

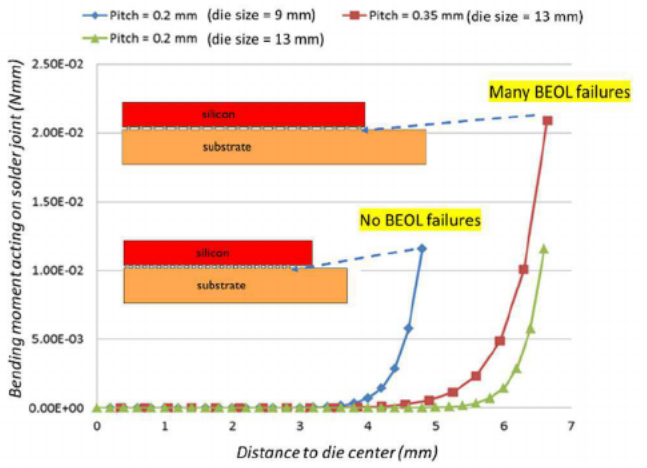

Fig. 3. Calculated bending moments in solder joints with varyaing die size and solder bump pitch

Underfills obviously reduce the forces acting on the solder joints and underlying BEOL layers. But there is still the solder reflow phase where underfill is not yet applied and therefore may be a critical phase in the assembly process. But also, the underfill must be well-chosen. Underfills with large CTE (coefficient of thermal expansion) mismatch with the solder bump material can cause high vertical forces which can also result in BEOL fractures.

A method to avoid these potential BEOL fractures during flip chip processing and thermal cycling qualification testing is through finite element modelling (FEM) of the thermo-mechanically induced stresses in the flip chip structure [3] [4] [5] . The outputs of the simulation study are stresses and deformations acting in the BEOL during the solder reflow process and during operational or qualification temperature cycling. To know if these stresses are causing fractures, measurements are needed to quantify the strength of BEOL layers. In this paper, a method is described and applied to a flip chip assembly structure.

II. Four Point Bending Method to Characterise the Strengths of BEOL

The method of measuring the BEOL strength utilized a four-point bending mechanism to generate delamination in the BEOL layers (Fig. 4) [6]. To create this mode of failure, two silicon strips were adhered to each other, and a notch was cut to act as the crack initiator during loading. The intent is that the crack should first grow downward through the silicon until it meets the BEOL layers where it then propagates laterally to create BEOL delamination. This is a highly dynamic process, and the crack propagates towards the weakest interface. It is no guarantee that the crack propagates through the BEOL layer. Therefore, inspection of the fractured samples after the bending test was needed.

The outcome of the four-point bending experiment is the force displacement curve (Fig. 5). There are different stages in this curve which refer to the fracturing at the notch, the fracturing towards the BEOL layer and the delamination of the BEOL itself. In the graph, the plateau refers to delamination growth of the BEOL; this plateau force can be transferred into an energy release rate value.

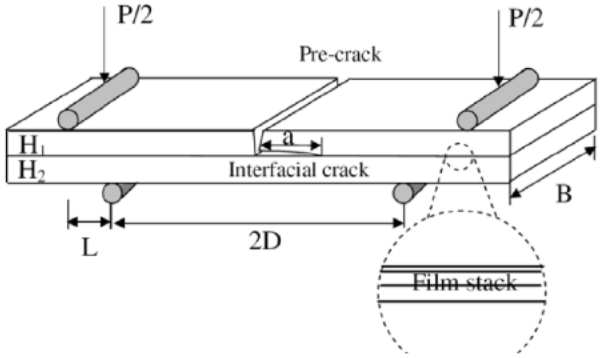

Fig. 4. 4-point bending setup on a stack of two dies

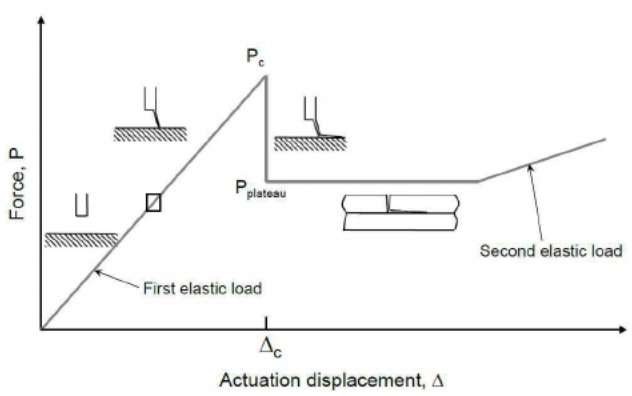

Fig. 5. A typical force versus displacement curve measured during a bending test

The critical strain energy release rate, G_c, can be calculated from the steady state fracture plateau load P as follows:

$$G_c = \frac{21}{16}\frac{(1-\nu_{substrate}^{\ 2})P^2L^2}{E_{substrate}B^2H^3}$$

where L is the distance between an inner and an outer load pin (i.e. the moment arm), and 2D is the distance between the two inner load pins. The two substrates have thickness H_1 and H_2, width B, Young's modulus E, and Poisson's ratio ν; $H = (H_1 + H_2)/2$.

The energy release rate is an appropriate value for the average strength of a specific BEOL structure. It allows to benchmark different BEOL technologies (oxide, low-k, ultra-lowK, airgap etc), different suppliers, and different number of stack-up layers.It is however less obvious to use this value in thermo-mechanical simulation studies. There are basically two methods in FEM which can handle these energy release rate values: cohesive zone material elements (CZM) and virtual crack closure technique (VCCT).

Cohesive zone material elements (CZM) are special interface elements that are inserted in the model. The idea behind cohesive elements is that fracturing is a gradual phenomenon in which separation takes place across an extended crack 'tip', or cohesive zone, and is resisted by cohesive tractions. Consequently, cohesive elements do not

represent any physical material, but describe the cohesive forces which occur when material elements (such as grains) are being pulled apart [6].

The VCCT technique is based on the principle that the work required to extend a crack by an infinitesimal distance is equal to the work required to close the crack to its original length [7]. Fracture growth is then simulated by comparing energy release rate G to critical energy Gc, set as a criterion. An advantage of this technique is that it calculates the different energy mode components at the crack tip, and that mode separation can be included in the failure criterion.

Implementation of both techniques in a complex 3D structure with 2000 solder bumps is basically impossible. For VCCT, you need to implement a crack which is not obvious in 3D. The cohesive element also substantially increases the model size.

At the end, the modelling is meant as a first order sanity check to assess the risk for BEOL fracture for a specific flip chip assembly. In this work, it was chosen to extract a critical stress value from the four point bending experiment.

III. Extracting Ultimate Stress Values for BEOL

Four-point bending experiments were performed on a Tektronix-designed advanced node CMOS that goes into a Tektronix product. The IC was 10x8 mm in size with 180-micron bump pitch and included low-k and ultra-low-k layers. Around 50% of the samples showed a plateau force which indicated a delamination in the BEOL structure. One curve representative for all measurements is shown in Fig. 6. In that case, a plateau force was measured at 10.5N. Due to complex multilayer structure of the BEOL, the force was not constant and slightly varied during the continued displacement as shown in the figure (between ~400 to 500 µm displacement).

For the samples that showed a plateau force, the values were found to be within 10 and 15N for this specific bending setup. SEM (Scanning Acoustic Microscopy) analyses confirmed that the crack propagated from the notch, through the glue, and into the thickness of the BEOL (Fig. 7). Delamination had occurred between the BEOL layers: specifically, between silicon oxide passivation and low-k dielectric passivation. (Fig. 8)

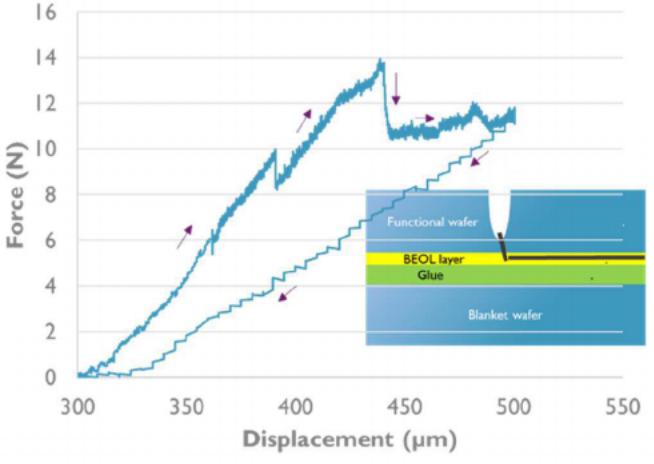

Fig. 6. Representative force displacement curve with a plateau force around 10.5N

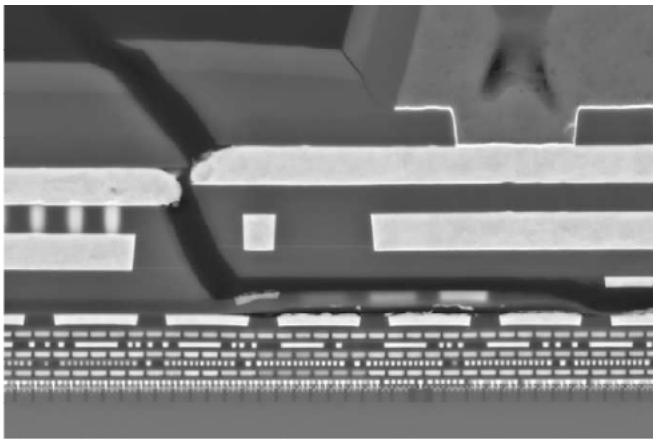

Fig. 7. Picture shows how fracture enters through the bulk chip through the BEOL to further propagate in the weakest area of the BEOL

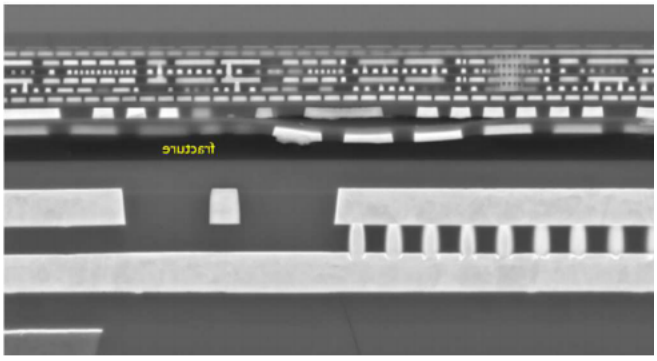

Fig. 8. Fracture zone in the BEOL after four point bending delamination test

Having verified that the test method correctly induced the delamination failure mode, a 2D plain strain FEM simulation of the four-point bending test was created to extract critical stress values (Fig. 9). It simulated the structure which had already cracked at the notch and has about 1 mm delamination in the BEOL.

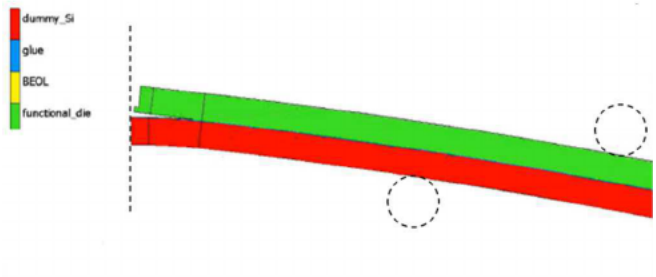

Fig. 9. 2D plain strain FEM of the 4 point bending experiment

With this approach, there was the issue of the stress singularity at the crack tip which made the stress value dependent on the mesh density. Therefore, a pragmatic approach was followed by having a similar mesh density in this 2D model as was used in a complex 3D model for flip chip assembly.

Fig. 10 shows the out-of-plane (or vertical) stress distribution at crack tip for a 10N bending. The stress was also linear to the applied force.

This critical stress is also just an average value for the BEOL. Some zones in BEOL will be weaker, other zones will

be stronger. Typically, in the region of (solder) bumps, BEOL are made stronger with higher copper density.

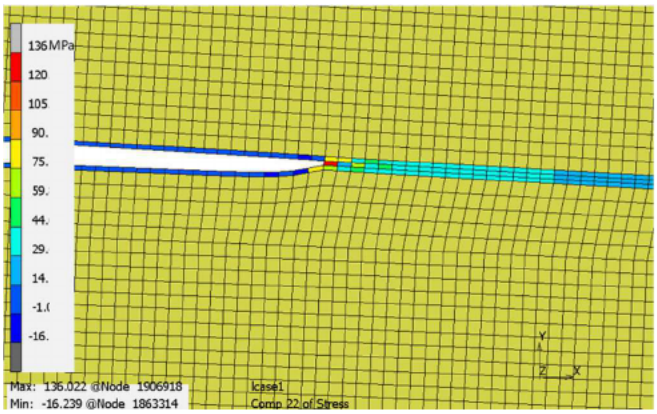

Fig. 10. 2D plain strain FEM of the 4 point bending experiment

IV. Application of Measured Ultimate Stress Values to a Flip Chip Assembly

A detailed simulation model was made for a standard solder flip chip assembly package with about 2000 solder bumps (Fig. 11). A visco-plastic model was applied to the solder elements while the underfill and BGA substrate had visco-elastic models. Additional details about the flip-chip simulation model are described in [10].

The aim was to calculate the stress evolution in the BEOL over the complete process of the flip chip BGA and also during temperature cycling (Fig. 12). This meant that in the first phases of the modelling, the underfill and stiffener ring were deactivated.

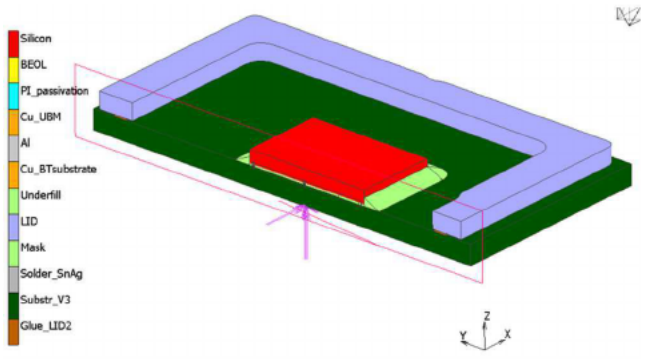

Fig. 11. Full 3D FEM of a flip chip assembly

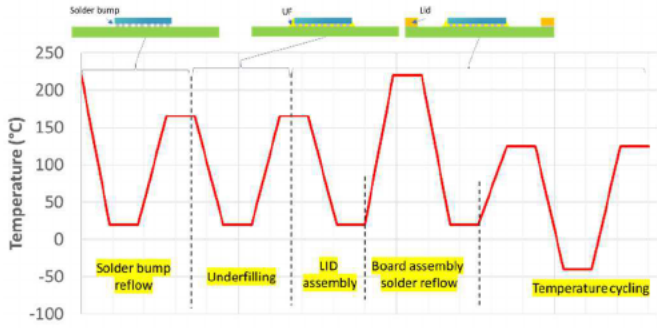

Fig. 12. Simulation process including all temperature variations

The highest vertical (peel) stress was seen in the BEOL during the cooling down from solder reflow to room temperature. Due to the large CTE mismatch between the large die and the substrate. As shown in Fig. 13, the highest value occurred near the die corner and was substantially below the ultimate stress value measured in the 4pt bending experiments.

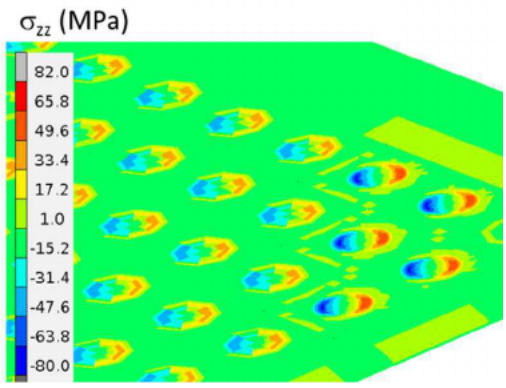

Fig. 13. Map of the vertical (out-of-plane) stress in the BEOL in the corner area during the cooling down from solder reflow to room temperature (first step in the processing)

The stresses during underfilling, lid assembly and temperature cycling were lower, but this was dependent on the chosen underfill and stiffener ring material. With worse choices of these materials, the BEOL stress may be even higher than in the first phase of the process and could cause BEOL damage.

V. Conclusions

Four-point bending experiments provided quantitative data on BEOL strengths. It allows for searching for the weakest interface in BEOL and has the capability to benchmark different technologies and suppliers of CMOS wafers.. These data can be used to perform sanity checks in thermo-mechanical simulations whether BEOL fractures are possible during packaging processes and during qualification and operational cycles.

Acknowledgment

The authors would like to thank Myriam Vandepeer for the sample preparation and bending experiments and Jan d'Haen from the IMOMEC group within imec for the SEM study on the tested samples.

References

[1] Vandevelde, B., Beyne, E., Vandepitte , D., and Baelmans, M., Analytical Thermo-Mechanical Model for Non-Underfilled Area Array Flip Chip Assemblies, ASME. J. Electron. Packag. September 2004; 126(3): 351–358. https://doi.org/10.1115/1.1772416.

[2] J. Kawahara et al., A simple model-base prediction method for delamination failures in Low-k/cu interconnects with flip chip packages, 2013 IEEE International Interconnect Technology Conference - IITC, Kyoto, Japan, 2013, pp. 1-3, doi: 10.1109/IITC.2013.6615560.

[3] M. Gonzalez et al., "Chip package interaction (CPI): Thermo mechanical challenges in 3D technologies," 2012 IEEE 14th Electronics Packaging Technology Conference (EPTC), Singapore, 2012, pp. 547-551, doi: 10.1109/EPTC.2012.6507142.

[4] Lei Fu, Milind Bhagavat, Ivor Barber, Bumping Process Impact on the Chip Package Interaction (CPI) Reliability, IMAPS 2018 - 51st

International Symposium on Microelectronics - Pasadena, CA USA - Oct. 8-11, 2018

[5] Bart Vandevelde, A. Ivankovic, B. Debecker, M. Lofrano, K. Vanstreels, W. Guo, V. Cherman, M. Gonzalez, G. Van der Plas, I. De Wolf, E. Beyne, Z. Tokei, Chip-Package Interaction in 3D stacked IC packages using Finite Element Modelling, Microelectronics Reliability, Volume 54, Issues 6–7, 2014, Pages 1200-1205, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2014.02.026.

[6] Ortiz M. and Pandol A. "Finite-Deformation Irreversible Cohesive Elements for ThreeDimensional Crack-Propagation Analysis", Int. J. Num. Meth. Eng., Vol. 44, pp. 1267-1282, 1999

[7] Krueger R., "The Virtual Crack Closure Technique: History, Approach and Applications", Appl. Mech. Rev., Vol. 57(2), pp. 109-143, 2004

[8] B. Debecker, K. Vanstreels, M. Gonzalez and B. Vandevelde, "Delamination in BEOL: Analysis of interface failure by combined experimental & modeling approaches," 2013 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2013.

[9] Luka Kljucar, Mario Gonzalez, Kris Vanstreels, Andrej Ivankovic, Michael Hecker, Ingrid De Wolf, Effect of 4-point bending test procedure on crack propagation in thin film stacks, Elsevier, Microelectronic Engineering, Volume 137, 2 April 2015, Pages 59-63.

[10] Kevin Cox, Jason Krantz, Matt Borden, Steven Tonthat, “Validating Flip Chip package models through experimental deflection measurements”, IMAPS 19th International Conference & Exhibition on Device Packaging, Fountain Hills, AZ USA, Mar 13-16, 2023.