Numerical Study on the Influence of Polyimide Thickness and Curing Temperature on Wafer Bow in Wafer Level Packaging

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***Abstract*—In wafer level packaging, polyimide and electroplated copper are dielectric and conducting materials respectively in the so-called redistribution layers. During the wafer fabrication process large amount of stress is generated in those layers due to curing shrinkage of the polyimide and the coefficient of thermal expansion mismatch of both materials to silicon which can lead to severe wafer bow after a high temperature curing. In different applications polyimide can be used either only as passivation layer over electroplated copper, or polyimide is applied before the redistribution layer and then a second polyimide layer is applied as passivation. In the current study the effect of different polyimide integrations is investigated. In-situ wafer bow measurements and finite element method studies were conducted with samples, with and without polyimide below redistribution layer, exposed to different curing temperatures to understand the change in wafer bow and copper residual stress. It is observed that wafers with polyimide before redistribution layer show higher stress relaxation in copper with decreasing curing temperature, resulting therefore in a lower wafer bow. A good agreement is achieved between the experimentally measured and the simulated wafer bow.**

Keywords— Wafer level packaging, redistribution layer, wafer bow, residual stress, finite element modeling

I. INTRODUCTION

Wafer level packaging (WLP) has been one of the fastest growing technologies in semiconductor packaging industry due to high demands, reduced fabrication cost and enhanced performance [1][2]. In a WLP, the redistribution layer (RDL) is used to re-route the I/O signal to the solder bumps. Polyimide (PI) as dielectric layer and electro-chemically deposited (ECD) copper as metallization is widely adapted in the RDL. Depending upon the I/O requirements the RDL can consist of five or more layers [3]. In RDL fabrication processes the wafer undergoes different high temperature process steps that result in reliability risks due to stresses induced in the wafer during fabrication. For example, during the RDL fabrication PI is cured at high temperature that results in stresses induced in the wafer due to cure shrinkage of the PI [4]. Simultaneously, thermal stress is also induced in the wafer due to coefficient of thermal expansion (CTE) mismatch between the different materials used in the RDL processing. These stresses might be high and result in large amount of wafer bow that affect handling of the wafer and subsequent processing steps on the wafer that can lead to reliability risks like delamination and passivation cracks [4]. Therefore, it is important to predict the wafer bow and limit the stress evolution for different films in the RDL.

The thermal stress induced into the wafer due to CTE mismatch during the high temperature process step is at least partially recovered after the wafer is cooled down to room temperature (RT) again. To minimize the stresses a change in material used in RDL is usually not an option because most of the materials are optimized to have the best I/O response of the signal to the solder bumps and lower down the reliability risks. The stresses generated due to cure shrinkage of PI also cannot be avoided due to volume loss during the polymerization reaction. In past, different studies have been done to reduce warpage by deposition of an additional passivation layer on copper [5]. The effect of passivation on RDL copper still needs to be investigated, because the effect of passivation layer on stress relaxation behavior of copper is different for patterned structures deposited with ECD process than that of the copper film deposited with sputter method without patterning.

This study focuses on reducing the stresses which are generated due to the deformation of copper by using PI, for which the imidization can be achieved at lower curing temperatures. In some investigations the variation in

mechanical response has been observed when PI is integrated only as passivation layer above the copper/PI patterned structures in comparison to PI that is integrated both as passivation over the copper/PI patterned structures and as a stress relief layer between the silicon substrate and the RDL [6]. In this paper, finite element method (FEM) based models with experimental verifications were used to predict the wafer bow for different PI integrations and to understand the effect of different curing temperatures on proposed PI integrations. Moreover, the work demonstrated measures to lower the wafer bow induced in the wafer during RDL fabrication process.

II. EXPERIMENT

A. Test Vehicle

In the experimental setup two sets of multi-layered thin films were fabricated on a 300 mm wafer. The variation in experimental setup on both the test vehicles is performed as follow:

(1) PI is used both as passivation over copper and as stress relief layer between substrate and RDL (see Figure 1 a). On the other hand, in the second setup PI is only used as passivation over the copper (see Figure 1 b).
(2) In addition, PI in both the cases have been cured at three different curing temperatures which are 250°C, 230°C and 210°C to understand the effect of curing temperatures on wafer bow.

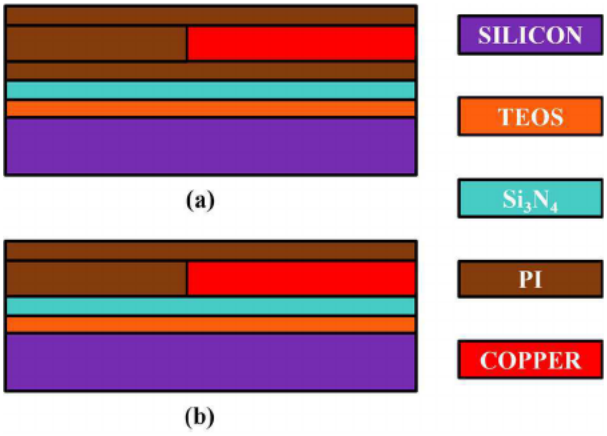

Figure 1: Schematic for fabricated RDL stacks: Sample with PI as stress relief layer (a) and sample without PI as stress relief layer (b)

In the wafer fabrication process for the samples with PI as stress relief layer (see Figure 1 a), TEOS is deposited on a silicon substrate followed by a Si_3N_4 passivation (see Figure 2). In the next step 1st PI layer (stress relief layer) is deposited followed by a curing at different temperatures, *i.e.* at 250°C for sample 1, 230°C for sample 2 and 210°C for sample 3. In the next step a 2nd PI layer is deposited on the wafer samples, the PI openings for the copper redistribution are exposed and a second curing is done at 250°C, 230°C and 210°C respectively for each sample. Before curing, the PI is structured using a lithography process and copper is deposited at RT. In the final step a 3rd PI layer is deposited as passivation on the patterned copper and again a third curing is done with 250°C, 230°C and 210°C respectively for each sample. The design of experiments (DOE) keeps all the process parameters and material thicknesses constant to investigate the change in wafer bow with the variation in curing temperature. Moreover, after the deposition of 3rd PI layer in-situ measurements are conducted to measure the wafer bow of all three sample sets with the Patterned Wafer Geometry (PWG) Metrology [7]. The above steps are repeated to also fabricate the samples without the 1st PI layer (stress relief layer) as shown in Figure 1 b to investigate the influence of 1st PI layer on the stress evolution in copper for both the test vehicles.

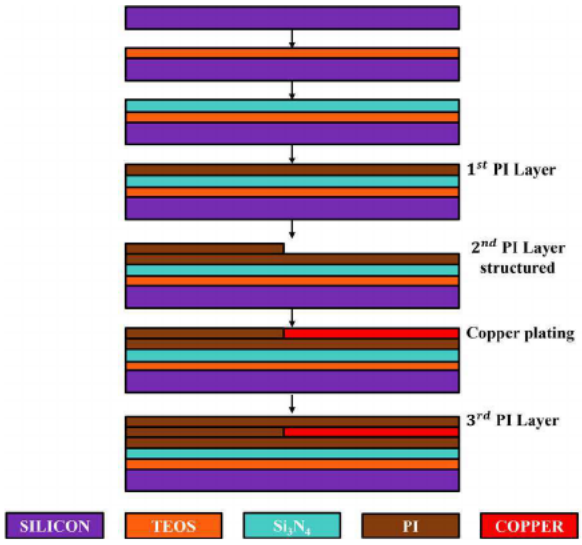

Figure 2: Schematic for steps involved in the fabrication process for test vehicles

III. FINITE ELEMENT METHOD MODELING

In addition to the experimental study, FEM based models were also developed to predict the wafer bow for different test vehicles processed at different curing temperatures. The FEM model setup involved a local to global modeling approach which was already presented in earlier work [7]. Firstly, the residual stress is calculated for different test structures in a local model. In the next step, both the material data and residual stress is added to a global full wafer level model to predict the wafer bow.

A. Residual stress calculation

The residual stress for the test vehicle (see Figure 1 a) is calculated by taking into consideration a die level model (see Figure 3 b) projected from a wafer reticle schematic (see Figure 3 a). The copper traces are also modelled in the local die level model embedded in the PI using GDS data [7]. In the next step, other layers are also modelled (see Figure 4 a) to complete the layer stack (see Figure 1 a).

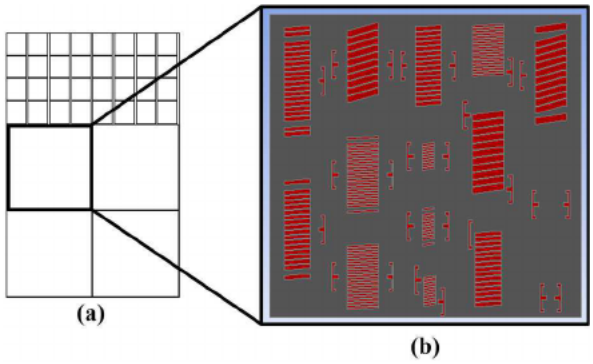

Figure 3: Wafer reticle schematic (a) and FEM model with copper traces embedded between the PI (b)

As the next step the residual stress is calculated by process modeling approach at die level model using element birth and death modeling technique. The test vehicle layer stack selected for this calculation is sample with PI as stress relief layer (see Figure 1 a). The curing temperature profile for each PI layer is shown in Figure 5.

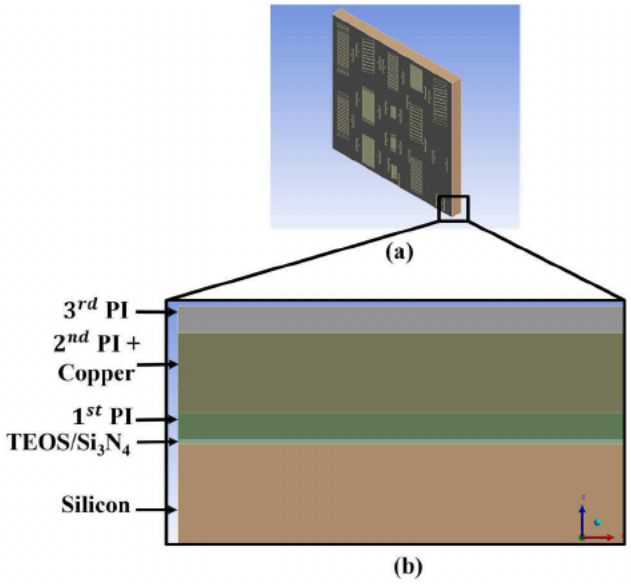

Figure 4: Full die level FEM model with copper traces (a) and cross-section of the model with complete test vehicle stack (b)

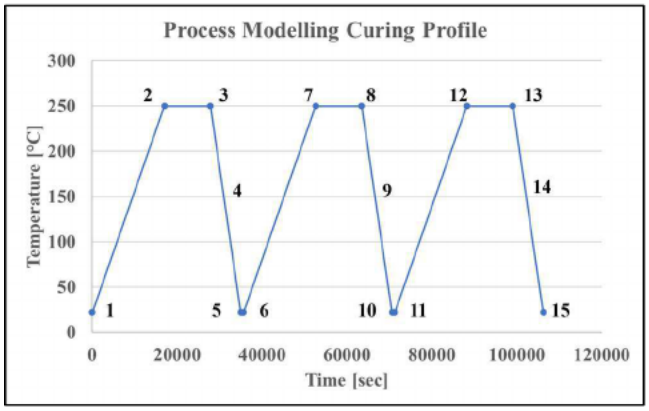

Figure 5: Curing temperature profile at 250°C for test vehicle with stress relief layer (see Figure 1 a)

In setting up the residual stress simulation model linear elastic material data is selected for all the layers. In addition, bilinear isotropic hardening (BISO) plasticity model is used for copper and prony series viscoelastic model is used for PI. The process flow for the modeling step is shown in Figure 6. The simulation starts from step 1 and the model only has substrate, TEOS and Si_3N_4 layer activated. At step 2 1st PI layer is activated, and the curing is done at the peak temperature of 250°C for 3 hours. Once the model is cooled down to 150°C at step 4 the cure shrinkage strain is applied to the PI. Later the model is further cooled down to RT. The model is again heated to step 7 and the 2nd PI layer is activated with structured pattern (wherein copper is deposited in subsequent steps) and cured. Like 1st PI layer, cure shrinkage strain is again applied to 2nd PI layer at 150°C and the model is further cooled down to RT. At step 10 the copper is deposited in the structured pattern of 2nd PI layer, and the complete model is again heated to peak curing temperature. At step 12 the 3rd PI layer is activated and cured. At step 14 the cure shrinkage due to PI curing is applied and the model is cooled down to RT. The remaining stress at step 15 is considered as residual stress and used in further simulation setup for global wafer level model to calculate the wafer bow. Above steps are also repeated to calculate the residual stress for both the stacks used in this investigation (see Figure 1) at different curing temperatures. The actual non-uniform metallization pattern (see Figure 3 b) is also simulated to calculate the pattern dependent orthotropic material data [7] for the copper embedded between the 2nd PI layer. In addition to the calculated residual stress, the orthotropic material properties, *i.e.* Young's modulus, Poisson's ratio and CTE would be used as an input parameter for full wafer level model.

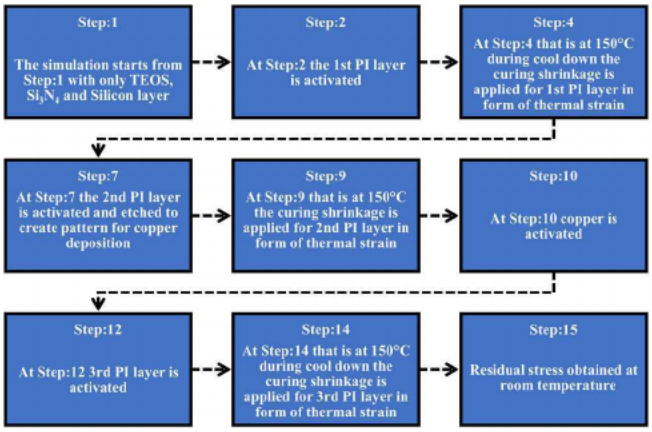

Figure 6: Process flow for the FEM modeling setup to calculate the residual stress

B. *Full wafer level model*

The full wafer level model is constructed based on the actual reticle layout (see Figure 3 a). Firstly, a reticle level model is constructed (see Figure 7 a) that is extended to a full wafer level model (see Figure 7 b). The full wafer level model also consists of all the thin film layers modelled with similar thickness as shown in Figure 4 b.

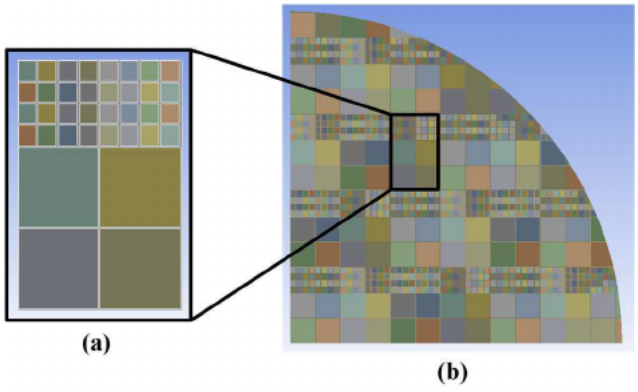

Figure 7: Reticle-level model (a) and quarter wafer level model (b)

The input parameter for the full wafer level model are the metallization pattern dependent orthotropic material data derived from the die level model. Also residual stress is applied for all the thin film layers shown in Figure 4 b calculated from local model discussed in section III A. For the residual stress calculation of PI layer embedded within

copper, an effective stress approach is used and input in the model [7]. To reduce the computational time a quarter model was established and the geometry is meshed with SOLSH190 mesh elements (see Figure 8 b) in Ansys with eight elements in the substrate thickness (see Figure 8 c). Symmetric boundary conditions were applied on the two symmetry planes and the center node is fixed in all the three directions to avoid rigid body motion (see Figure 8 a).

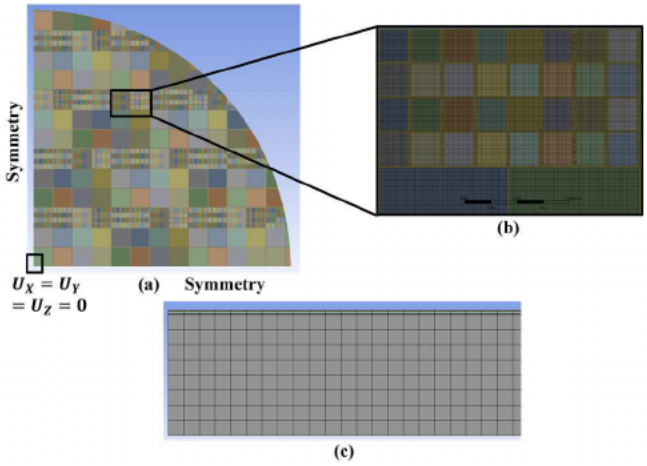

Figure 8: Boundary conditions applied in quarter wafer level model (a), mesh on wafer level model scoped to defined reticle location (b) and mesh structure in substrate thickness in the wafer level model (c)

IV. RESULTS AND DISCUSSION

A. Experimental Results

The wafer bow in each sample is measured after the curing of 3rd PI layer and cooled down to RT using the methodology discussed in section II A. Figure 9 shows the increase in wafer bow for the wafer samples without the 1st PI layer (stress relief layer).

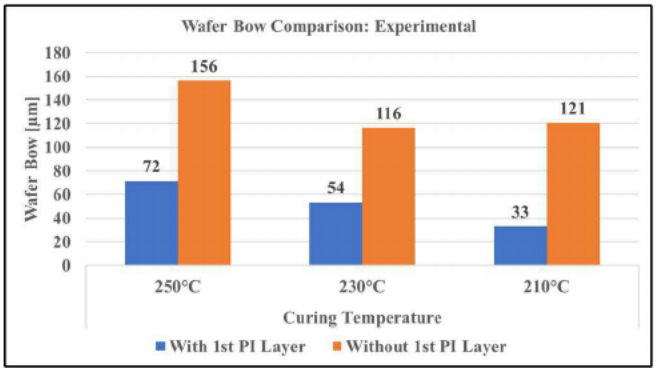

Figure 9: Experimental wafer bow comparison for stack with 1st PI layer (see Figure 1 a) and without 1st PI layer (see Figure 1 b) at different curing temperatures

At 250°C curing temperature wafer bow obtained for the samples with 1st PI layer is 72 µm and without 1st PI layer is 156 µm. The percentage deviation of wafer bow for wafer samples without 1st PI layer from sample with 1st PI layer is 118% (see Figure 10). At 230°C curing temperature wafer bow obtained for the samples with 1st PI layer is 54 µm and without 1st PI layer is 116 µm. The percentage deviation of wafer bow for wafer samples without 1st PI layer from sample with 1st PI layer is 117%. Similarly, at 210°C curing temperature wafer bow obtained for the samples with 1st PI layer is 33 µm and without 1st PI layer is 121 µm. The percentage deviation of wafer bow for wafer samples without 1st PI layer from sample with 1st PI layer is 267%. The measured wafer bow was then compared to simulation results (see section IV C).

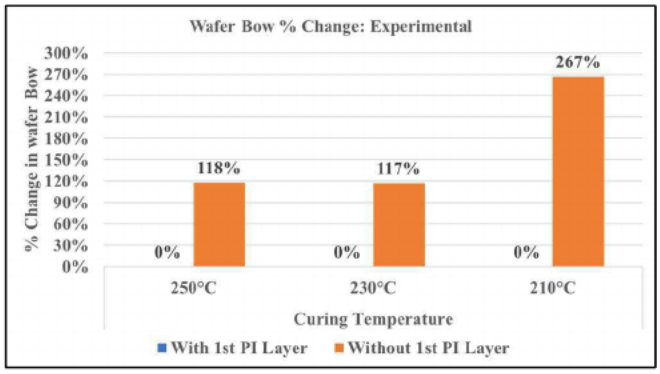

Figure 10: Percentage change in experimental wafer bow for wafer samples without 1st PI layer relative to wafer samples with 1st PI layer at different curing temperatures

B. Simulation Results

Wafer level models were setup as discussed in section III B and their input parameters including the residual stress for copper were derived from local die level models (see section III A). This was carried out for both the wafer samples configuration (see Figure 1) at different curing temperatures. Figure 11 shows the residual stress distribution in copper on both the samples discussed in Figure 1 at 250°C curing temperature. The samples without 1st PI layer show higher stresses within copper as compared to samples with 1st PI layer considered in the model.

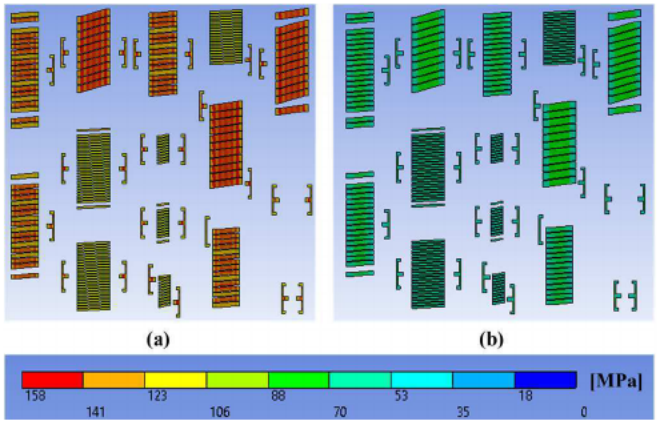

Figure 11: Simulated residual stress distribution: Sample without 1st PI layer (a) and sample with 1st PI layer (b)

Figure 12 shows the stress comparison at different curing temperatures for varied sample configuration (see Figure 1). The residual stress obtained at 250°C curing temperature in copper for sample without 1st PI layer and with 1st PI layer is 158 MPa and 78 MPa respectively. Residual stress obtained at 230°C curing temperature in copper for wafer sample without 1st PI layer and with 1st PI layer is 146 MPa and 58 MPa respectively. Similarly, the residual stress obtained in copper at 210°C curing

temperature for wafer sample without 1st PI layer and with 1st PI layer is 138 MPa and 39 MPa respectively. The residual stress thus obtained was used in the wafer level simulation model to predict the wafer bow. Figure 13 shows the calculated wafer bow for the sample configurations (see Figure 1), at 250°C curing temperature. The results in the images are scaled up five times from true scale. Here again we see that the wafer bow is lower for samples with 1st PI layer.

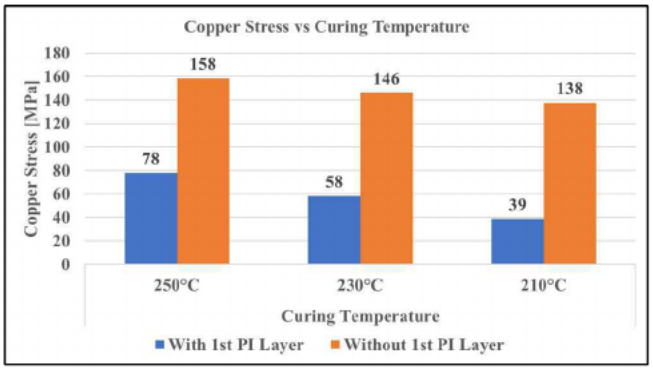

Figure 12: Residual stress calculated with simulation for copper at different curing temperatures for both sample configurations

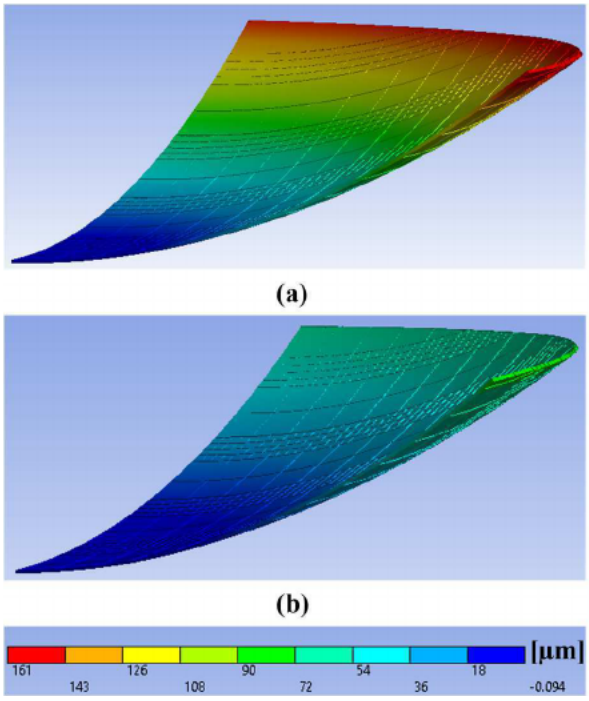

Figure 13: Wafer bow simulated results at 250°C curing temperature: Sample without 1st PI layer (a) and sample with 1st PI layer (b)

Figure 14 shows the wafer bow comparison at different curing temperatures for varied sample configuration (see Figure 1). The wafer bow obtained at 250°C curing temperature were 161 µm and 76 µm for samples without 1st PI layer and with 1st PI layer respectively. The percentage deviation in wafer bow for samples without 1st PI layer relative to sample with 1st PI layer is 122% (see Figure 15). At 230°C curing temperature wafer bow obtained for sample without 1st PI layer and with 1st PI layer were 122 µm and 58 µm respectively. The percentage deviation in wafer bow for samples without 1st PI layer relative to sample with 1st PI layer is 109%. Similarly, at 210°C curing temperature wafer bow obtained for sample without 1st PI layer and with 1st PI layer were 115 µm and 36 µm respectively. The percentage deviation in wafer bow for samples without 1st PI layer relative to sample with 1st PI layer is 223%.

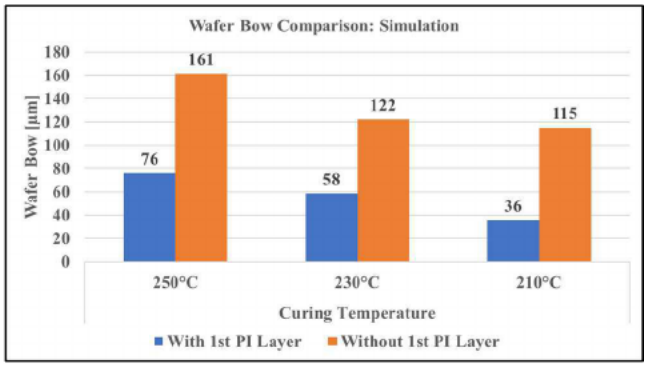

Figure 14: Simulated wafer bow comparison for stack with 1st PI layer (see Figure 1 a) and without 1st PI layer (see Figure 1 b) at different curing temperatures

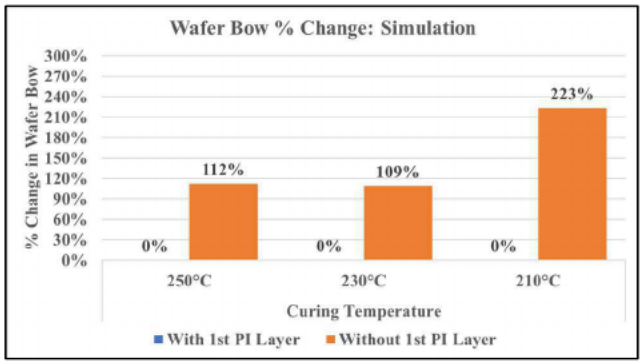

Figure 15: Percentage change in simulated wafer bow for wafer samples without 1st PI layer relative to wafer samples with 1st PI layer at different curing temperatures

C. *Experimental vs. Simulation Results*

The section IV A and IV B of this study shows the wafer bow development for different PI integrations schemes at varied curing temperatures. Both experimental and simulation shows dependence of wafer bow on PI integration methods and curing temperature. Due to the introduction of 1st PI layer the overall residual stress in the copper is relaxed (see Figure 12). The residual stress of copper obtained from simulation for samples with and without 1st PI layer are 78 MPa and 158 MPa respectively for a 250°C cure temperature, that shows higher stress relaxation in copper when the 1st PI layer is integrated within the sample. Similarly, as the PI acts as a stress relief layer, there is a reduction in the wafer bow observed with the introduction of 1st PI layer. Moreover, in copper films surface diffusion and vertical grain boundary diffusion are dominant stress relaxation mechanism. The traditional in-organic passivation on copper restricts this surface diffusion in vertical direction therefore restricting the grain growth which would lead to lower wafer bow. However, the PI as the passivation layer is softer than traditional passivation

layers, hence there is a behavior change when it is integrated within copper RDL, *i.e.* the PI passivation (3rd PI layer) does not have influence on the wafer bow reduction efforts. Moreover, the 1st PI layer acting as a decoupling layer together with Si_3N_4 between substrate and copper can restrict the atomic migration and grain boundary diffusion that results in lower wafer bow.

In addition to the PI integration method, the curing temperature indicates a rather linear dependence on the wafer bow within the given temperature range. For instance, at 210°C curing temperature the wafer bow observed experimentally for samples with and without 1st PI layer are 33 µm and 121 µm (see Figure 9) respectively, which are lower than the wafer bow obtained at 250°C. Similarly, in simulation investigation at 210°C curing temperature the wafer bow observed for sample with and without 1st PI layer are 36 µm and 115 µm (see Figure 14) respectively, that are lower than the simulated wafer bow obtained at 250°C. These data lead to the conclusion, that there is a clear dependence of wafer bow on the curing temperature. Moreover, Figure 12 also confirms the indication of a linear reduction in simulated copper residual stress with reduction of curing temperature. Since the PI viscoelastic behavior did not contribute significantly to the residual stresses and deformations caused in the wafer. Also the plastic behavior of the copper was just not triggered because the residual stress did not exceed the yield stress of copper. Hence the linear dependency of wafer bow is well supported by simulation findings. Moreover, a lower curing temperature with appropriate imidization percentage of PI is proposed for wafer bow reduction efforts.

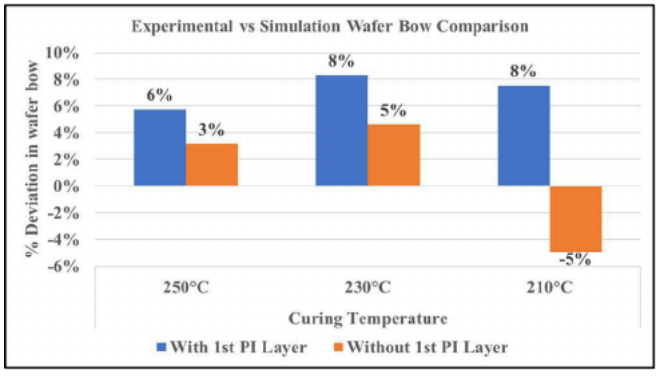

Figure 16: Percentage deviation between simulated and experimental wafer bow for stack with 1st PI layer (see Figure 1 a) and without 1st PI layer (see Figure 1 b) at different curing temperatures

The percentage deviation of simulated from experimentally generated wafer bow magnitude is 6% for wafer sample with 1st PI layer and 3% for wafer sample without 1st PI layer cured at 250°C (see Figure 16). At 230°C percentage deviation of simulated from experimentally generated wafer bow magnitude is 8% for wafer sample with 1st PI layer and 5% for wafer sample without 1st PI layer. Similarly, at 210°C percentage deviation of simulated from experimentally generated wafer bow magnitude is 8% for wafer sample with 1st PI layer and -5% for wafer sample without 1st PI layer. At 210°C experimental and simulation deviation for samples without 1st PI layer is -5% this can be due to the increase in experimental wafer bow at 210°C in comparison to 230°C. This increase in wafer bow at 210°C can be the effect of averaging the results obtained at 210°C on three different wafer samples. Overall, the simulation results show a good correlation to the experimental data.

V. CONCLUSION

In this study the wafer bow development was studied for multi-layered structures. Experimental and simulation models were setup to understand the effect of different PI integration schemes and curing temperature on wafer bow. Since the modeling results are in a good correlation with the experimentally generated data, the FEM model had been validated. In next steps the validated FEM model can be used for further optimization of PI thickness and copper design for wafer bow reduction efforts. The experimental and simulation results show lower wafer bow obtained for test structures integrated with 1st PI layer (stress relief layer) when compared to test structures without 1st PI layer. Hence the PI-1 integration should be taken into account during the WLP fabrication phase to reduce the final wafer bow.

In addition to the PI integration schemes, curing temperature has a linear effect on the wafer bow. In both the test vehicles, the wafer bow decreases with the decrease in curing temperature. From this study, the authors propose to have a 1st PI layer integrated as decoupling layer and to have a curing temperature not to be more than 210°C during fabrication phase to reduce the final wafer bow.

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