Fine Pitch Micro Indium Bump Interconnect Flip Chip Bonding

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***Abstract*—Quantum computing processors, micro LED displays and Focal Plane Array (FPA) imaging and detector devices such as infrared (IR) thermal imaging sensors are seeing higher demand as more practical applications requiring these components are coming into research and development, industrial, military and consumer markets. This paired with higher pixel and Qubit count and interconnect density, on larger and larger chips is driving hybridization and monolithic integration in these technologies. This is showing a marked increase in demand for fine pitch micro bump interconnection flip chip die bonding. However, some critical challenges facing these technologies are; larger component sizes mean higher density interconnections over increasing surface area. Sub-micron accuracy required to align fine pitch micro interconnect arrays. This together with the challenges facing the materials that are becoming the industry standard for these applications, such as the requirement for the assembled components to remain stable in extreme conditions such as cryogenic application environments. Combined with low loss high strength mechanical / electrical interconnect requirements on components containing sensitive materials, structures and unmatched coefficient of thermal expansion (CTE) means that processing gases such as formic acid or high temperature reflow bonding can no longer be used to bond these devices. These challenges mean that the industry is fast approaching the limitations of even state-of-the-art die bonders and die bonding methods on the market today. This paper is going to highlight these challenges and the methods used to address them to produce large format, high density IR thermal imaging FPA devices, Quantum processors and micro LED displays using fine pitch micro Indium bump array interconnections that meet today's industry requirements.**

Keywords— Focal Plane Array / Quantum / Super – computing / Fine pitch micro Indium bump / flip chip die bonding / hybridization / Monolithic – integration

I. BACKGROUND

The application material of fine pitch micro Indium bump arrays, such as quantum computer processors, Infrared (IR) thermal imaging focal plane arrays (FPA) and micro LED displays covered by this paper usually consists of one or more components bonded to a substrate using a fine pitch array of vacuum deposited micro Indium bumps.

There are many challenges involved in bringing these components together to form a fully functional assembly, such as co-planarity, accuracy, interconnect yield, mechanical/electrical strength and interconnect quality while maintaining a competitive throughput in the industry.

To ensure a highly repeatable high yield flip-chip bonding process that meets these requirements, a number of solutions were developed and tested to address these challenges. As well as addressing tertiary issues such as handling and cleaning of the material and reducing oxides and organic materials on the Indium or UBM interconnect surfaces were trailed and or solved to reduce the time required to prepare the material for bonding and reduce the risk of damaging the material via manual handling.

In this paper the details and solutions to these challenges will be outlined.

II. FLIP CHIP DIE BONDING OF FINE PITCH MICRO INDIUM BUMP ARRAYS

Die Bonding process

Due to the high cost of the application materials, Infrared (IR) Focal Plane Arrays (FPA) and their Read Out Integrated Circuit (ROIC) components, and Quantum processors as well as the time and difficulty involved to produce high quality functional material, it was vital that the initial bonding trials can produce successful parts with minimal trial and error or failure.

The following processes and preparations as well as software and hardware solutions were used in the trial bonds to achieve the desired results.

The trials described here were all carried out on a FINEPLACER® femto 2 automated die bonder.

Die bonder requirements

Accuracy requirements for bonding 5 µm bump, 15 µm pitch, 640x512 resolution Indium bump array on 10x8mm components:

- Post bond accuracy < 0.5 µm @ 3 sigma over 10-25mm components
- Automatic systematic error correction of the die bonder is required to maintain post bond accuracy over multiple days and high temperature duty cycles within the die bonder
- Controlled handling and accurate fine force control during touching down to components as well as the initial touchdown and force control during the bonding process is critical to maintain post bond accuracy and mitigate any damage to the Indium bump array or sliding / shearing during the bonding.

Bond Process

Bond force

- Low bond forces are required to mitigate damage to the delicate indium bumps. Low forces used in component handling in the die bonder in the range or 0.05 N – 1.0 N showed no visible change to the bump surfaces.
- Fine control of force ramps in the bonding profile were desired to ensure no slipping or shearing occurred during force build up _ 0.1 – 0.5 N/s was used and showed stable results.

Bond profile

The temperature and force bond profile depends on the chosen bonding method.

- Cold compression Bonding = room temp - 90°C
- Thermal Compression Bonding = 100 - 164°C
- Reflow Bonding = 165°C +
- Formic acid reflow bonding = ~210°C
- FAC reduction at ~210°C and bonding at ~165 - 180°C

Material preparation and handling

Compression die bonding of fine pitch micro indium bump arrays usually consists of one or more components, and a substrate. In this paper we will use the example of an Infrared thermal imaging sensor (IR Sensor) and Substrate (ROIC) both containing an interconnect layer of fine pitch micro Indium bump array (Indium bump to bump bonding), as this is the example with the smallest bumps and bump array pitch over the largest surface area, making it one of the more challenging applications to address.

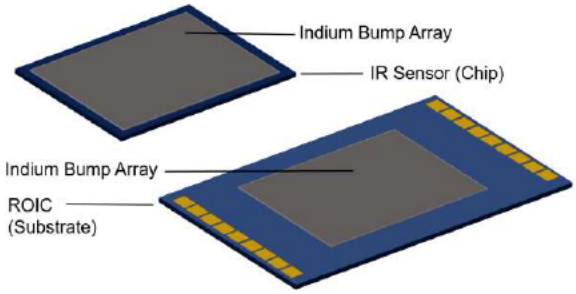

Fig. 1. IR FPA and ROIC components

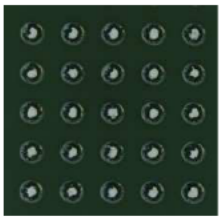

Fig. 2. 5 µm bump, 15 µm pitch Indium bump array

Material

The fine pitch micro Indium bump array is usually grown on the component and/or substrate material using a vacuum-evaporation deposition process supported by a photolithography exposure mask of photoresist. In some cases, after the bump array has been grown on the wafer, the deposition mask is removed and a fresh layer of photoresist is deposited to protect the delicate indium bumps from physical damage, prevent oxidization and prolong the shelf life of the material.

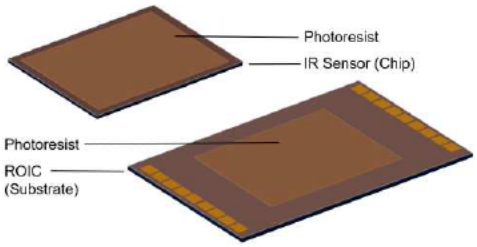

Fig. 3. Photoresist-coated components

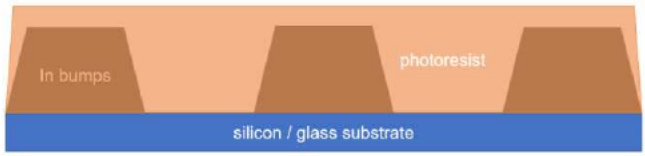

Fig. 4. Photoresist-coated Indium bumps

Preparation

The first challenge most encounter when preparing to bond fine pitch micro indium bump arrays, is the removal of the protective photoresist layer and the cleaning and removal of all contamination and particles (Particles > 1.0 µm) from the Indium bump array area. To address this challenge a material cleaning and preparation station was developed to allow for a seamless tweezer free chemical cleaning and material kitting process, to prepare material and packs for automated bonding of multiple assemblies with minimal handling of the components to reduce risk of contamination or damage.

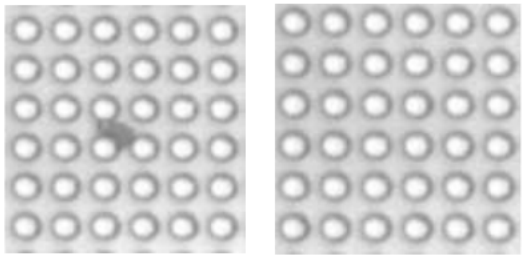

Fig. 5. ~10 µm contamination removed between Indium bumps

Handling

Handling the material during the cleaning, kitting and material to die bonder loading process poses the greatest risk of damaging or contamination of the components and more critically the Indium bump array. To address this challenge a tray handling and loading system that completely removes the requirement of tweezer handling was developed. Once the components have been loaded into the handling trays they can be easily cleaned, inspected, flipped to be presented “Indium up” or “Indium down” for the automated die bonding process and loaded into the die bonder, all without the use of tweezers, this method significantly reduced the occurrence of particle contamination, photoresist and acetone residues while reducing the chance of damaging the indium bump array or dropping the components. This also reduced the material preparation time by ~ 50% for a single assembly, but allows for enough component material to be cleaned and prepared for 4-6 assemblies, which is a significant improvement in process time and risk reduction.

All materials of the handling pack can aggressively be cleaned with acetone without risk of generating particles or contamination. The functional elements of the kit can also withstand high compression bond forces, high reflow bond temperatures and formic acid process gas and plasma cleaning meaning that it is suitable for both cold compression bonding or formic acid reflow bonding.

For standard components (640x512 resolution, 10x8mm) for example, the kit will allow for the simultaneous cleaning, kitting, flipping and loading of 4-6 components and 4-6 substrates to the bonding area.

All clamping and work holding was supplied by vacuum and the pockets were defined to either avoid all contact with the Indium bump array or sensitive areas on the components or limiting the "fall gap" of the component during flipping to <500 µm ensuring that the maximum force exerted on the Indium bump array would only be the weight of the component itself.

Tooling requirements

The tooling required to carry out the automated die bonding of fine pitch micro indium bump arrays will be broken down into tooling for the die handling and tooling for the substrate handling, but the mechanical requirements for both chip and substrate handling and their contact/bonding surfaces are very similar.

Material and Flatness

The materials and as well as the flatness of the tooling and bonding surfaces required to withstand high force and high temperature bonding environments with corrosive processing gases such as formic acid were a critical consideration during this project.

As the technology for fine pitch micro bump growth/deposition develops the tendency is for the interconnect size to decrease as the density increases, meaning that bump height and diameter is steadily heading into the ranges of single microns and potentially sub-micron bumps or interconnects in the near future.

In the more extreme case of IR FPAs with component sizes are getting larger, 20 - 50 mm, coated almost completely in Indium bump arrays of ~5-7 µm bumps, 15 µm pitch, with an ROIC component containing only metallised pads or vice versa, leaving only 3-4 µm bump height across the bond.

Due to this, one of the main requirements of the component handling and die bonding surfaces is flatness. In these extreme cases bonding surfaces need to meet flatness requirements below 0.5 – 1.0 µm over a surface area larger than the components themselves (< 0.5 µm over 20mm for example).

There are a range of solutions to solve the flatness requirement. These range from precision lapped and polished surfaces, compound tools made of two or more components/materials and speciality materials for the bonding interface surfaces depending on the chosen process. For the reflow and formic acid processes materials such as Copper Tungsten (WCu) were evaluated for higher coefficient of thermal expansion (CTE), and composite Tungsten (W) tools were tested for cold compression bonding to preserve flatness..

Vacuum structure

A bonding impression is when the resulting image of a sensor has a "ghost" pattern or regular pattern breaking the uniform image of the sensor. This is usually caused by non-uniform force distributed across the bonding surface.

A common example of this in sensor bonding is the shape of the vacuum structure, used to hold the component on the bond tool, being transferred and seen in the final output image of the sensor as a result of less force being applied in the gap between tool and component left by the vacuum structure.

Larger vacuum channels can also deform and bend the chip itself into the vacuum channel if the chip is thin enough and the vacuum structure is too wide.

To mitigate this phenomenon, tooling and work holding were all defined with the narrowest and smallest vacuum channel depending on the tool material and component size. This thinner vacuum structure also showed improved surface flatness specifically around the vacuum structures.

Modules

The automated FINEPLACER® die bonder system used for the experiments was fitted with the following modules to address bonding specific challenges. Each module aims to address a specific challenge faced when carrying out cold, reflow and formic acid reflow flip chip bonding of fine pitch micro bumps.

Heated Modules

For thermal compression bonding, reflow bonding and formic acid reflow bonding processes the bonding surfaces of the bond head and substrate carrier may be required to reach the elevated temperatures required to melt and reflow the Indium bumps (165°C +) as well as reaching the activation temperature required to reduce the oxide layer found on the Indium using formic acid (~ 210°C).

Tool Tip Changer Module

To allow multiple tools to be used in a bonding process the tool tip module was used. Allowing the automated loading and unloading of operation specific tools, for example, and the automated systematic error calibration could be carried out using the calibration tool and then the bonder could immediately proceed to the automated bonding process.

This was useful specifically during the high temperature duty cycle processes. To maintain very high accuracy.

Tool Levelling Station for co-planarity

Due to the height of the micro bump array as well as the large component size, co-planarity is vital to the bonding process, to allow for even pressure and a parallel, even bond line across the entire bump array.

To compensate and correct the co-planarity of the tooling, a passive levelling method was used that was observed to correct tool co-planarity to within < 0.5 µm over a 25mm tool surface.

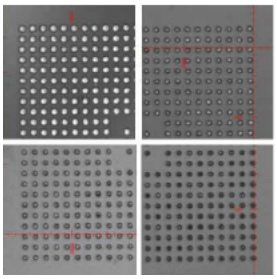

Fig. 6. ~ **5 µm** co-planarity

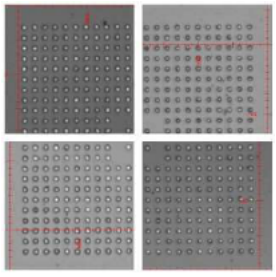

Fig. 7. < **1 µm** co-planarity

Inert Gas / Formic Acid

For reflow and formic acid reflow bonding processes the bonding area was supplied with inert gases to create an inert environment using Nitrogen (N2), or a processing gas like formic acid to reduce oxides on metal surfaces to expose fresh Indium bonding surfaces/materials.

To reduce oxide on the Indium bumps or to reform the pyramid shaped bumps into more uniform and less amorphous spheres the Indium can be reflowed in a formic acid environment with a laminar flow to carry away the oxides.

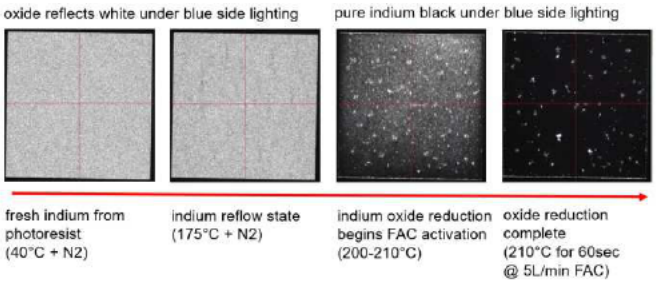

Fig. 8. Indium oxide reduction under FAC process gas

Once formic acid reflow is complete the components can be observed to contain far less oxide, with a majority of the surface being pure Indium or a very thin layer of oxide covering the Indium making for a higher strength and higher electrical quality bond surface.

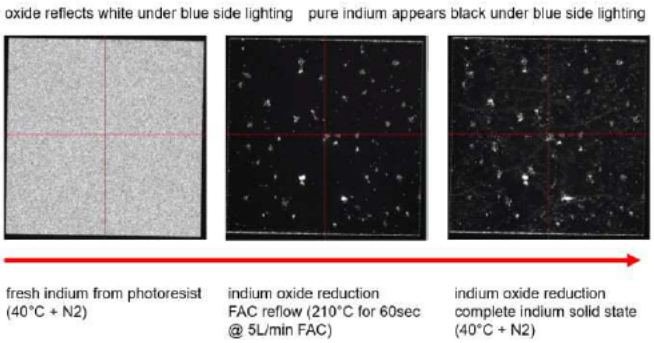

Fig. 9. Indium oxide reduction under FAC and cooled to solid state under N2

Laser Height Measurement

The automated Fineplacer system used for bonding is fitted with a Laser Height Module for various measurement, evaluation and qualification functions.

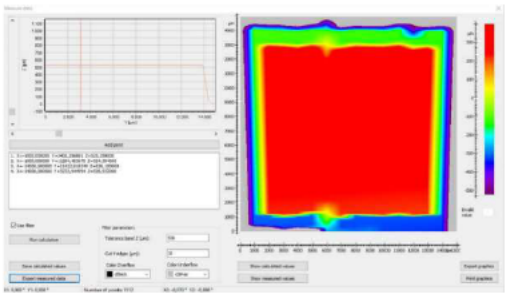

Fig. 10. Laser height measurement (Surface Height Measurement)

The module can be used to measure and evaluate tool surfaces, bonding surfaces and component surfaces for flatness and co-planarity or the height between the top surface of the substrate and component using 3 or more points in a point height measurement process, or a more detailed line scanning process (pictured above) to generate a topographical map of the surface being measured with a sub-micron resolution.

The results of these measurements were useful when evaluation the trial bond for flatness, co-planarity and estimating the bond line thickness of assemblies.

III. Results

Accuracy

To develop the tooling requirements, bonding process and fine tune the bonding parameters a transparent chip with indium bump array was bonded to an ROIC with indium bump array. This trial was also used to asses post bond accuracy.

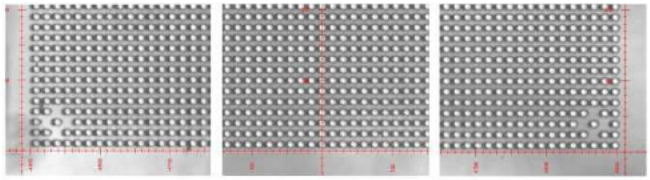

Fig. 11. ~ 4-5 µm offset error_ observed through transparent component 130N over 5 µm bump, 15 µm pitch 10x8mm Indium bump array. Substrate bumps (black) can be seen between chip bumps (white)

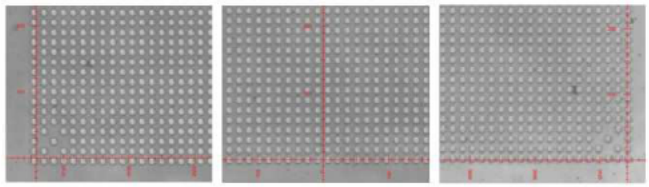

Fig. 12. < 1 µm offset error_ observed through transparent component 130N over 5 µm bump, 15 µm pitch 10x8mm Indium bump array. Chip and Substrate bumps perfectly aligned, only top chip bumps (white) can be seen.

By optimizing the tooling, cleaning, process preparation, and bonding parameters in combination with systematic error correction, it was possible to consistently bond the components within 1µm over many trials per day and maintain this quality over extended periods of time (1 – 2 weeks) without having to adjust the system.

Flatness and co-planarity

Optimizing the hardware and tooling design, in addition to the passive levelling of the tools enabled consistent, repeatable and controllable flatness and co-planarity in the bonds.

The flatness and co-planarity achieved on the 5 µm bump, 15 µm pitch 8x10mm IR FPA trials was consistently below 1 µm.

Fig. 13. ~ **5-6 µm** co-planarity error

Fig. 14. ~ **1 µm** co-planarity

(Newton ring effect, each 4 lines is estimated to be ~ 1 µm. Observed through transparent component, 130N over 5 µm bump, 15 µm pitch 10x8mm Indium bump array)

Interconnect Quality

Real IR FPAs were bonded using these methods and underwent functional testing and stress testing for operation in cryogenic environments. Unfortunately these results cannot be shared but the results showed and interconnection yield of above 90 - 95%+ of the components with good dark current characteristics while withstanding high stress duty and temperature cycles.

IV. Discussion

Fine Pitch Micro Indium Bump Arrays

Indium bump arrays are seeing larger adoption in quantum computing with very demanding requirements for co-planarity and control of bond line thickness as well as high quality electrical interconnections, IR FPAs are showing a constant drive for higher resolution meaning smaller bumps, higher density and larger surface areas, and finally the higher consumer market demand for µLEDs or Micro LEDs means that much higher through put will be required for fine pitch indium interconnects.

These requirements will become quite demanding for the die bonders on the market today and will drive further innovation to solve these challenges in novel ways.

V. Conclusion

Fine pitch micro Indium bump bonding is a challenging application, but using the methods described above it was possible to take challenging bonding process and streamline it into a more stable version of a low volume production process, removing risk of damage or failure while improving yield and bond quality in a more controllable and repeatable manner.

The FINEPLACER® femto 2 automated die bonder and the tooling and modules in combination with the cleaning and handling methods developed for this process is an Ideal solution for low level production or RnD development of any fine pitch micro Indium bump array application for IR FPAs, quantum computing processors or µLED displays.

VI. References

[1] International Data Corporation (IDC), (2020): "Worldwide Quantum Computing Spending Guide" https://www.idc.com/getdoc.jsp?containerId=prUS48414121

[2] Quantum Industry Report, (2020): "2020 Quantum Industry Survey" https://www.globenewswire.com/en/news-release/2020/11/10/2123434/28124/en/Global-Quantum-Technology-Market-Report-2020-Much-More-than-Computing-the-Market-will-Reach-21-6-Billion-by-2025.html

[3] Gartner, (2021): "Hype Cycle for Emerging Technologies" https://infocert.digital/analyst-reports/2021-gartner-hype-cycle-for-emerging-technologies/#menuid2

[4] Yole Développement, (2021): "MicroLED Displays - Market, Industry and Technology Trends" https://s3.i-micronews.com/uploads/2021/08/YINTR21162-MicroLED-Displays-Market-Industry-and-Technology-Trends-2021-Sample.pdf

[5] R. K. Bhan (2019): "Recent infrared detector technologies, applications, trends and development of HgCdTe based cooled infrared focal plane arrays and their characterization" http://dx.doi.org/10.1016/j.opelre.2019.04.004