High Speed Transmission Characteristics on Glass based interposers

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Abstract— **Interposers for system in package will became more and more important for advanced electronic systems. As the industry moves toward HPC (High Performance Computing) for huge data transmission with low power consumption. The major engineering requirements for HPC application are high-density, high speed data transmission, low loss, precision manufacturing and low cost. On the 2.5D heterogenous package structure, key technology is fine wiring connected with CPU chip and HBM chips. The fine wires needed high speed transmission.**

This paper presents the demonstration of Glass-based twin type interposers, Glass interposer with fine pitch metalized through via and RDL interposer with low loss dielectrics on Glass carrier. We compare twin types of Interposes fabrication process capability with panel size format 300x400mm. Finally, we compare the transmission characteristics using eye diagram for heterogenous integration application

Glass Interposer has low loss glass via, it is effective vertical interconnection. RDL interposer has low loss dielectric layers, excellent transmission characteristics obtained on fine pitch trace area.

Keywords— Glass Interposer RDL Interposer

I. INTRODUCTION

As electronic product becomes smaller and lighter with an increasing number of functions, the demand for high density and high integration becomes stronger. As the industry moves toward HPC (High Performance Computing) for huge data transmission with low power consumption. The requirements for PKG structure have become more challenging. The major engineering requirements for HPC application are high-density, high speed data transmission, low loss, precision manufacturing and low cost. On the 2.5D heterogenous package structure, key technology is fine wiring connected with CPU chip and HBM chips. The fine wires needed high speed transmission. On the other hand, Fanout panel level packaging (FOPLP) technology spread out 2.5D system integration. FOPLP has no core substrate like silicon TSV or glass TGV, it has advantage on manufacturing cost and panel scale productivity.

This paper presents first the demonstration of glass interposers with fine pitch metalized through via and low loss dielectric layers.

Firstly we demonstrate TGV process capability with panel size format 300x400mm. We model high frequency characteristics for high-speed transmission applications using basic high frequency characteristics.

Secondary we show process flow and demonstrate RDL interposer with low loss dielectrics layers. High speed transmission characteristics for RDL interposer modeled with eye diagram. Excellent transmission obtained on fine pitch trace area using low loss dielectrics.

II. GLASS BASED INTERPOSERS

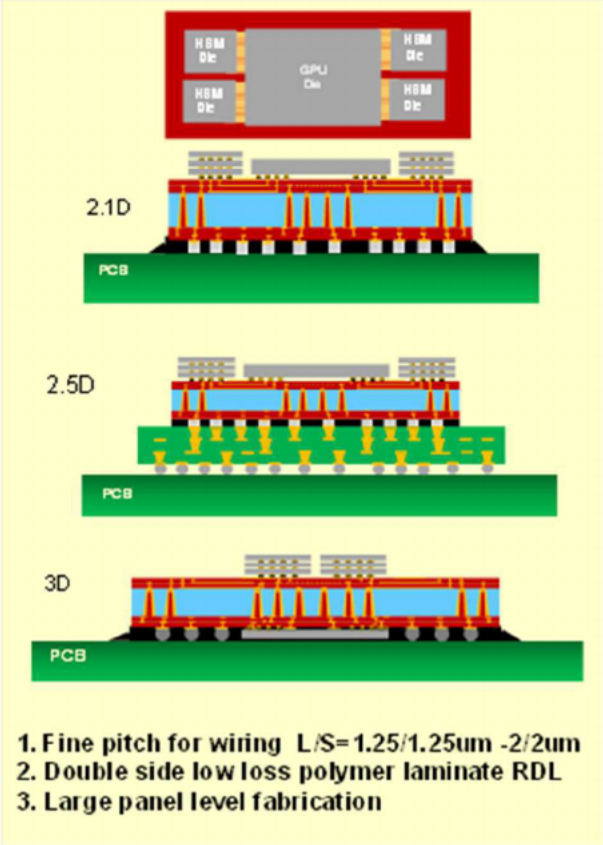


Figure 1. Schematic structure of Glass based Interposer

III. GLASS INTERPOSERS

Figure 2 shows process flow of Glass interposer.

First of all, TGVs of 80μm in diameter and 200μm in pitch were formed on 400μm thick alkali-free glass. Ti/Cu seed layer deposition. Then the via was deposited with Cu by conformal electroplating. Thick dielectric polymer layer was laminated on the wafer as RDL passivation film. Redistribution lines were patterned with photo resist. Cu RDL line of 5 μm thickness was deposited by Cu electroplating followed by photo resist and Cu seed layer removal

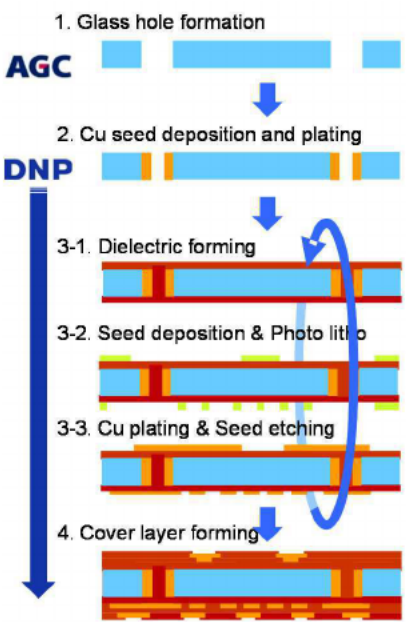


Figure 2 Cross sectional view of via formation

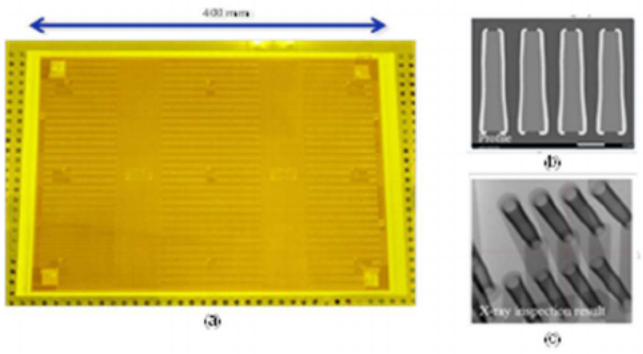


Figure 3 Cross sectional view of via formation

The conformal plating method has great advantage of process time of plating. After depositing the seed layer, plasma ashing was done from the both sides of the wafer to improve the hydrophilic property of the surface of Cu seed layer. Conformal TGV with 300x400mm panel demonstrated shown in Figure 3.

A. High frequency characteristics

High frequency electrical characteristics of interposers were evaluated with three type metalized method. We have selected a combination of a transmission wiring with coplanar waveguide structure (CPW) and TGV in order to study the influence of TGV on high frequency region. The measurement of TGV only itself is difficult because measurement TEG needs outer pad for probing. It is not ignored influence of the outer pad. We choice the method compared CPW and CPW+TGV show in Figure 4. The data are corrected from TEG which have Line and space are 30μm and 15μm for impedance 50ohm matching. Length of CPW is 10mm.

Double side metal layer test vehicle containing co-planer waveguides (CPW) with TGV transmission were designed. Electrical measurement was performed after SOLT calibration and the CPW transmission characterized up to 40GHz. Figure 5(a) shows test vehicle containing co-planer waveguides (CPW) with filled types of metalized method. Figure 5(b) shows test vehicle containing co-planer waveguides (CPW) with conformal types of metalized method. The network analyzer S-parameter measurements indicate that CPW has lower loss than CPW+TGV in transmission shown in Figure 5.

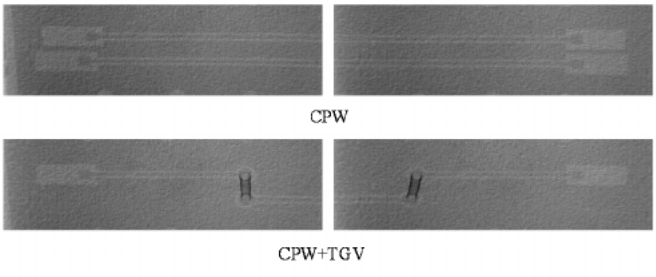


Figure 4 CPW transmission line TEG

Both types of metalized TGV have excellent transmission. Filled via has slightly lower loss than Conformal via in transmission shown in Figure 5.

It causes reflection on the joint with trace and TGV. Highly bulk resistance of TGV resulted in an insertion loss less than -0.5dB at 30GHz. It causes reflection on the joint with trace and TGV.

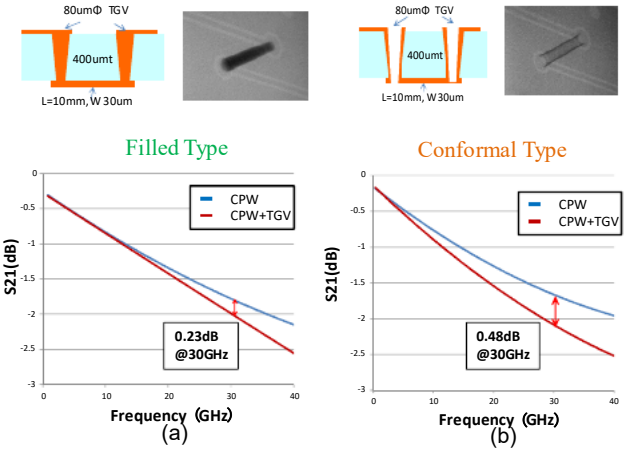


Figure 5 Co-planer waveguide test vehicle

The new types of partial filling plating method applied for measurement. Partial filling types have great advantage of fine pitch arrangement due to half diameter of conventional ones. [1] AGC developed high aspect small diameter TGV. Figure 6 shows test vehicle containing co-planer waveguides (CPW) with partial filling types of metalized method using small diameter TGV. Figure 7 shows measurement result CPW and CPW with TGV. The differential of S21 summarized in Table 1. Three types of TGV were all very low loss.

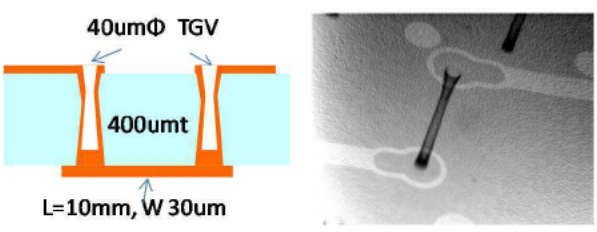


Figure 6 Co-planer waveguide test vehicle

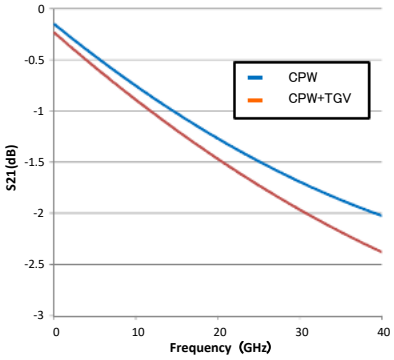


Figure 7 Measurement result of partial filling TGV

Table 1

Types of TGV plating method	Difference of S21
Filled type	0.23 @30GHz
Conformal type	0.48 @30GHz
Half fill type	0.34 @30GHz

Fused quartz has an amorphous structure which is composed of Si-O-Si network and no periodic atomic configuration. Therefore, the dielectric characteristics of fused quartz, especially its loss tangent, is lower than other typical materials. [2]

Quartz glass and conventional glass demonstrated TEG for high frequency measurement as core glass.

Table2

Core Glass	Er	Tanδ
AQ Synthetic fused silica Glass	3.8	0.0002 @10GHz
EN-A1 Conventional Glass	5.8	0.006 @10GHz

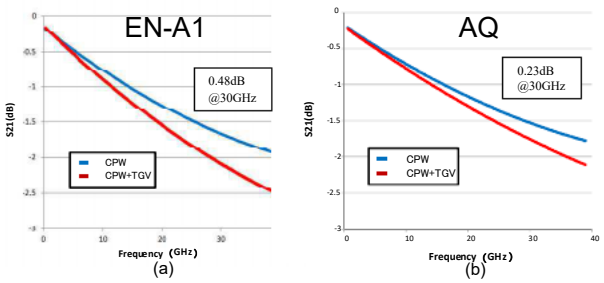


Figure 8(a) and 8(b) shows comparison of insertion loss.

Figure 8 Measurement result of AQ fused silica glass

AQ fused silica glass indicates lower less than ENA1 conventional glass.

Differential of S21 with TQV also smaller than TGV are shown in Table 3. AQ fused silica glass has lower dielectric tangent than Conventional glass. Extremely low dielectric tangent of Quartz glass resulted in an insertion loss of less than -0.23dB at 30GHz.

Table 3

Core Glass	Differential of S21(dB)
AQ Synthetic fused silica Glass	0.23dB @30GHz
EN-A1 Conventional Glass	0.48dB @30GHz

Figure 9 shows modeling method of Eye diagram. Measurement result of insertion loss was converted to Eye diagram of transmission 10Gbbs input pulse signals.

Figure 9(a)(b) and 9(c)(d) shows comparison of Eye diagram. AQ fused silica glass indicates lower rise time less than ENA1 conventional glass. TGV(TQV) is very low influence for the rise time.

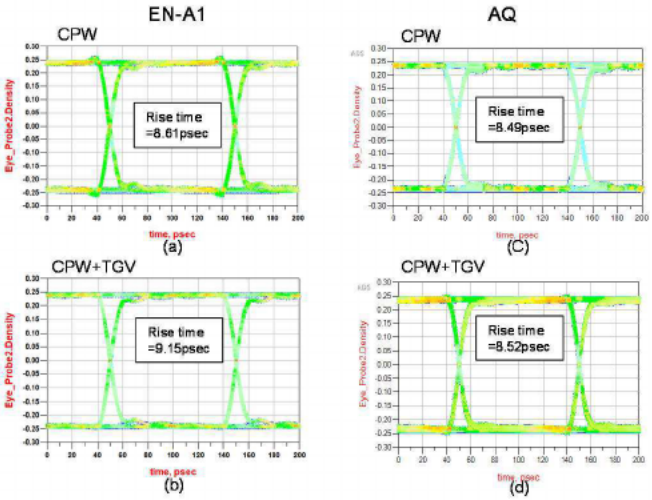


Figure 9 Modeling result of Eye diagram

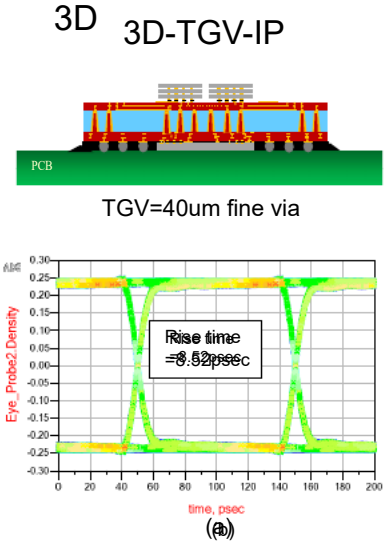


Figure 10 schematic structure of heterogenous 3D -TGV PKG

Figure 10 show high speed transmission characteristics for 3D-TGV PKG modeled with eye diagram. Excellent transmission obtained on fine pitch trace area.

IV. RDL INTERPOSERS

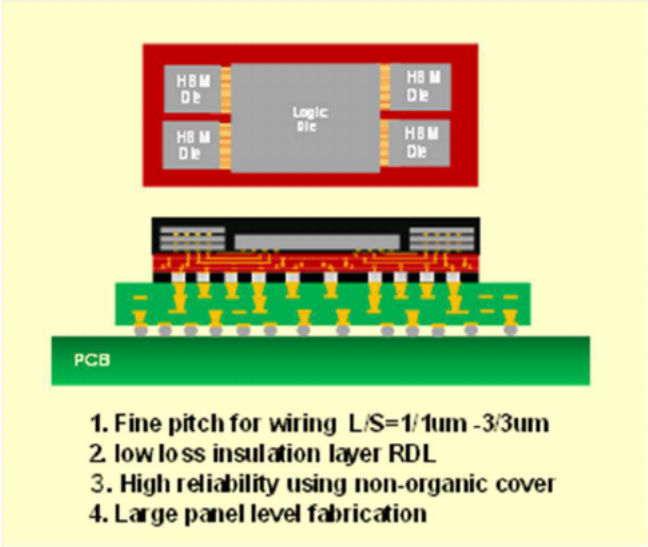


Figure 11 (a)Schematic structure and feature of RDL Interposer.

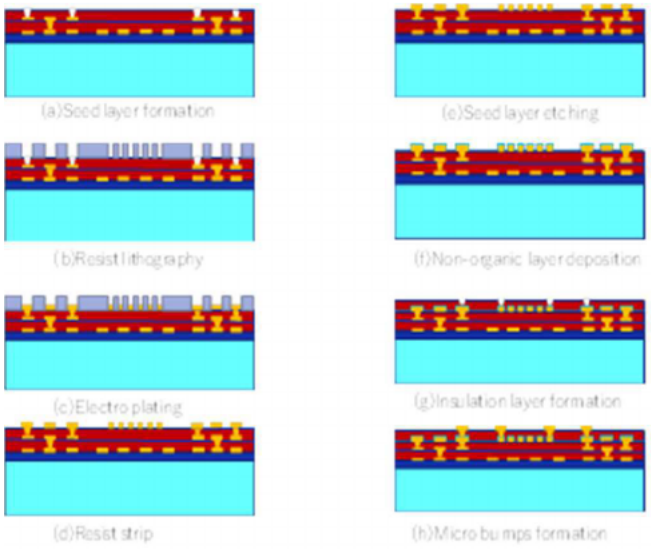


Figure 12 Process flow of RDL interposer

Figure12 shows Process flow of RDL layers. At first, seed layer formation on lower steps on the insulation layer. (a) Secondary, Photo resist formation and open the wiring area with developer. Thirdly, electro-plating applied open area of photo resist. (c) After resist striped(d), seed layer metal was etched. (e) And then non-organic layer deposit on the Cu trace(f). It is original process for high reliability of the RDL layer. After insulation layer formation, Nonorganic layer was dry-etched through opening area of insulation layer. Finally micro bumps formation on the top layer. [3]
Figure13. shows fine wiring layers on 300x400mm Glass panel format. 2-µm-pitch Cu trace fabricated on the glass.

Figure14 show L/S=1/1um trace with protective layer. Non-organic layer enhance highly reliability on the narrow pitch under 4um [3].

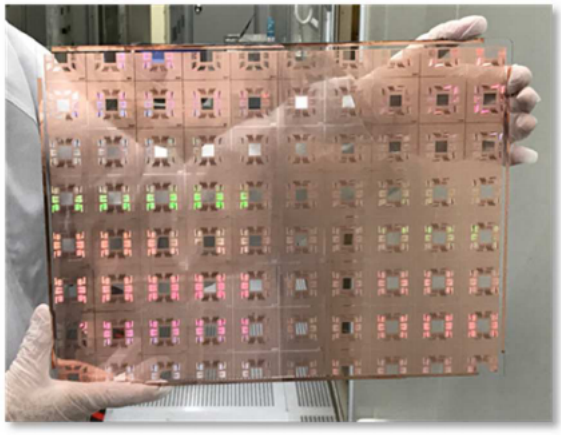
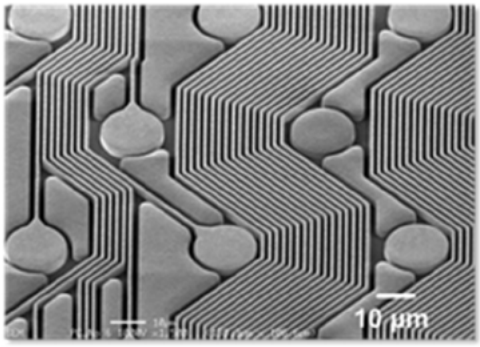
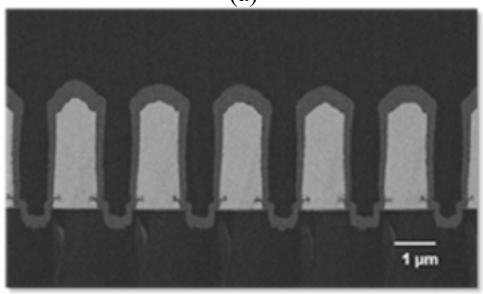


Figure 13. Fine wiring layers on 300x400mm Glass panel format.



(a)



(b)

Figure 14(a) L/S=1/1um trace
(b)trace profile with protective layer

Insulation layer materials is important role of RDL properties. Insulation layer materials needed small size micro via, Low stress for reduction warping and low loss tangent for high-speed signal transmission.
Figure 15 Shows result of via diameter reproduction PI-A. Via shapes is taper forms, minimum diameter was top 5.5um and bottom 2.4um with H line LDI.
Figure 16. shows multi-layer stack of RDL. 5metal RDL layer include fine pitch layer demonstrated stacking on carrier glass. Fine wiring layer fabricated on flat intermediate RDL surface.

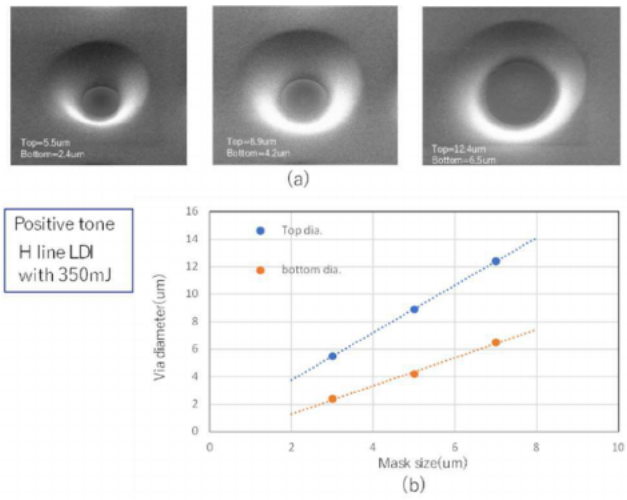


Figure 15. Via diameter of insulation materials PID

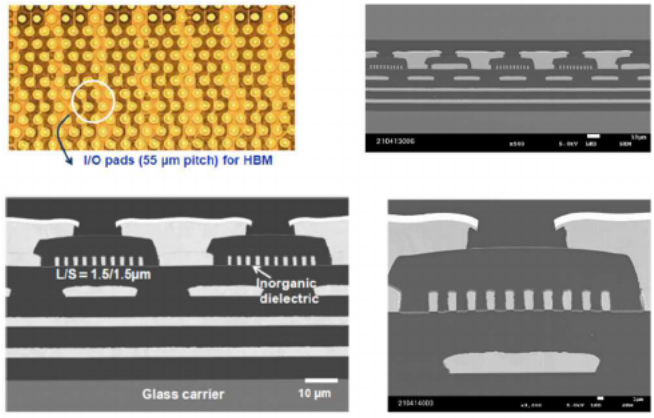


Figure 16. Profile of 5metal layer stack

We demonstrate CPW transmission line with fine wiring layers. TEG fabricated on core glass to measure high frequency characteristics. We calculated insertion loss with fine line. Figure 24 shows real measurement result of fine wiring consist of CPW structure. Insertion loss has large value with fine wiring pitch due to the conductive loss will be large.[4]

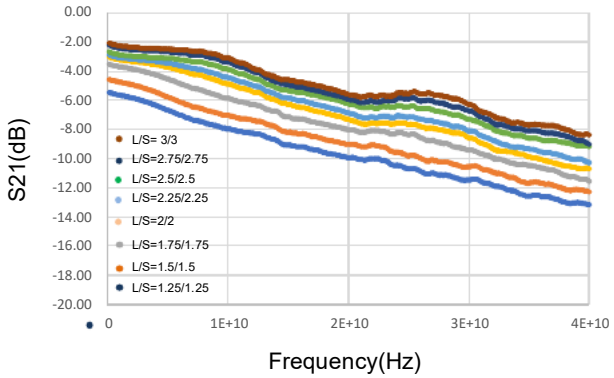


Figure 17 Measurement result of fine wiring consist with CPW structure.

Figure 18 shows simulation result of analysis on 10Gbps. CPW 10mm length wiring with dielectric polymer calculated for conversion Eye diagrams. Wiring width is small, eye opening is small with wiring width.
Eye diagram of L/S=0.5/0.5um show signal delay is large with rising time. It indicates that typical BEOL damacine process same factor as L/S=0.5/0.5um. 10Gbps will next standard after HBM3. In the next generation, It needed more critical signal integrity.

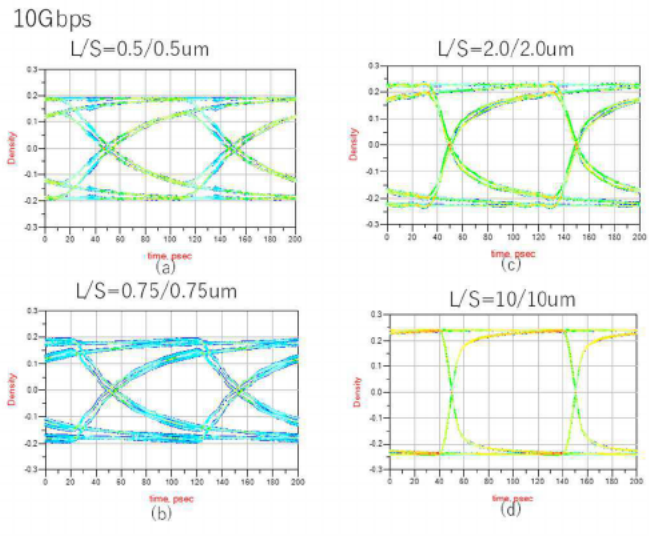


Figure 19. Simulation result of CPW on RDL

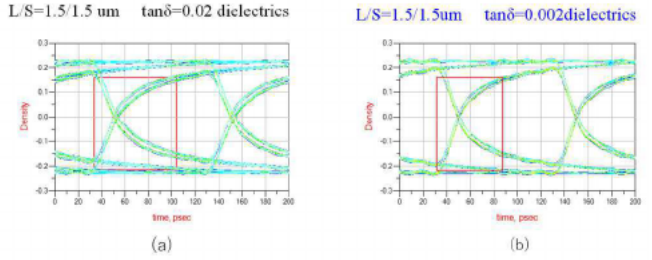


Figure 20. Eye diagram analysis with insulation layer

Figure 20(a) show the ED (eye diagram) of 10Gbps, L/S=1.5/1.5um CPW with tanδ=0.02 dielectrics.
Figure 20(b) show the ED (eye diagram) of 10Gbps, L/S=1.5/1.5um CPW with tanδ=0.002 dielectrics.

Table 4 summarized result of low loss tangent of dielectric layers. Rising time of the eye diagram using low loss dielectrics 30% smaller than other.

Table 4

Model	Eye height(V)	Rising time(psec)
CPW tanδ=0.002 dielectrics	0.30	25.7
CPW tanδ=0.02 dielectrics	0.27	33.8

It indicates that trace width will be optimized as wide as possible to route between the chips with low loss dielectric insulator.

The specification opened in UCIe 1.0 is expected to provide standardization of chiplet-based communication for advanced packages. In the specification of advanced packaging, the required processing speed is ranged from 4 to 32 Gbps/line, which corresponds to the bandwidth density of from 1.0 to 10.5 Tbs/mm. On the basis of the specification of the UCIe1.0, we set signal line length between chiplets to 1.0 mm in the I/O sections (1.0 mm x 2) and 0.4 mm in the middle section, so the total length was 2.4 mm (Fig. 21). This is 20% longer that of the required signal line length/channel length between chiplets (2.0 mm) in the specification of UCIe 1.0.

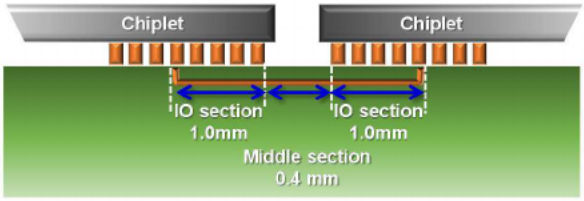


Figure21 Length of signal line consisting of both IO sections and middle section for specification of UCIe 1.0.

Cross-sectional dimensions used in the simulation for the topologies of GSG, SSG and SSS are shown Figure. 21 (a), (b) and (c).

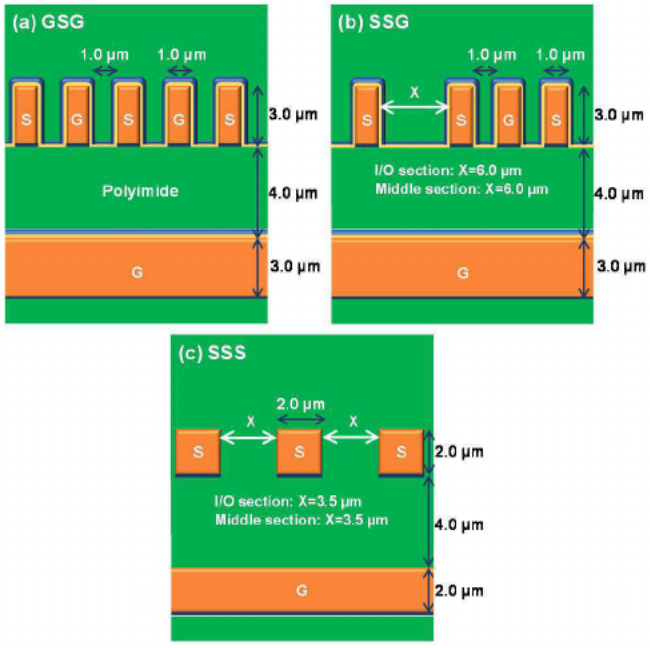


Figure 22 Cross-sectional dimension of signal line for topologies of GSG (a), SSG (b) and SSS (C).

The wave form for the topology of SSG did not cross the keep-out area, indicating a shield effect created by the ground line neighboring the signal line reduced the cross-talk (Figure.23 (b)). The wave form for the topology of GSG was away from the keep-out area enough (Fig.23 (a)). Both side ground lines neighboring the signal line greatly removed electromagnetic force generated around the signal lines. Both topologies of GSG and SSG met the specification of UCIe 1.0 at 32 Gbps.

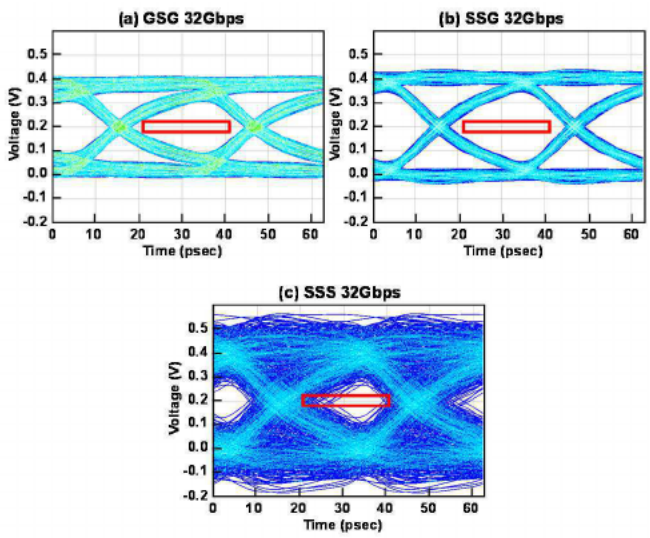


Figure23 Simulated eye diagram of topology GSG (a), SSG (b) and SSS (c) at 32 Gbps in specification of UCIe 1.0.

V. SUMMARY

Interposers with TGV interconnects was demonstrated with fine pitch through via. High speed transmission characteristics for 3D-TGV interposer modeled with eye diagram. Excellent transmission obtained on fine pitch trace area.

Fine wiring L/S=1/1um demonstrated using Semi-Additive-Process on the 300x400 panel format. Excellent uniformity of resistance obtained for HPC application.

Modeling transmission structure, Excellent transmission characteristics obtain fine pitch area using low loss dielectrics.

ACKNOWLEDGMENT

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