Analysis and Characterization of Castellated Holes as RF Interconnects for Modular Millimeter-Wave Devices

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Abstract´ This paper presents an innovative approach to the use of Castellated Holes or Plated Half Holes (PHH) as transmission elements for high frequency interconnections between printed circuit boards in a frequency range of up to 40 GHz. The basic design was examined using commonly used design parameters for PCB modules with Castellated Holes which were then investigated and subsequently optimized to improve their RF performance, with a particular focus on design considerations according to today's industrial manufacturing capabilities. Therefor the FEM-based full wave simulation technique was used to compare and optimize the design parameters in the aim to improve the capability of PHHs as low-loss, low-disturbant RF interconnection alternative in modular PCB designs. Based on these results test samples were developed, which were subsequently measured and thus verified the findings of the simulation. To provide a general comparability, this study focused on the S-Parameter to quantify the performance in terms of transmission losses and reflection. With an optimized design feasible results were achieved with a maximum transmission loss of less than 2 dB at the maximum of the desired frequency range and about 1dB at 20 GHz over the entire signal path. These insights make PHHs suitable for seamless integration into modular designs in RF and millimeter-wave applications.

Keywords´ castellated holes, PHH, millimeter wave application, board to board soldering, RF

I. Introduction

In modern PCB design, the approach of modular design has emerged as a standard process due its the benefits of improving efficiency, flexibility and scalability throughout the product development lifecycle. By breaking down complex systems into individual subgroups with specific functions, developer and manufacturers are able to optimize and improve design, prototyping and production processes. The modular approach plays also a significant role in RF design. Sensitive circuits and components can be better shielded in contained modules, expensive RF substrates and special design rules do not have to be applied to the entire system, thus reducing the complexity and cost of the entire system. In addition, a modular design offers further key advantages: It allows the parallel development and testing of individual functional groups and also simplifies the prototyping, debugging and validation processes. It also increases the reliablity, as many new developments often make use of existing and well-known subgroups and modules. This considerably reduces the development effort and fasten design processes. It also streamlines the production process and reduces the need for complex multi-layer PCBs, thereby reducing costs, simplifying assembly and increasing overall efficiency.

For connecting separate modules with each other or with the main system, several options exist: the widespread method of using connectors (with cables or directly to the board) or board-to-board soldering as a common technique among developers and manufacturers to integrate smaller PCBs into larger ones. Soldered connections serve hereby as an interface for establishing a fixed mechanical connection between the modules and the main system as well as providing the electrical connections for power supply or signal transmission. This can be achieved by using Ball Grid Arrays (BGA) or - the most common method - by using castellated holes, also known as PHHs. The latter approach is one important factor in establishing modular design processes, enabling scalability and facilitating customization of products, as it uses standard PCB manufacturing and assembly processes to providing an effective electronic packaging solution.

A. Comparison of RF interconnection approaches

Modular design is also well established in RF applications [4]. To establish a RF interconnection between two boards, specific RF connectors are used as the primary method. Despite their explicit function, their usage can result in signal degradation due to impedance mismatch and insertion loss, particularly at high frequencies or have to be optimized with great effort [1][2]. They also require more board space, leading to size constraints, and are susceptible to mechanical issues. In addition, the assembly process of connectors can be very complicated. BGA-based methods bring challenges, such as soldering complexity, limited accessibility after soldering, and potential thermal issues. Design complexity increases, especially for higher density BGAs, requiring careful unbundling and consideration of signal integrity [3].

PHHs are a good alternative for connecting two boards. These are inexpensive to manufacture and do not increase the complexity of the assembly. Despite their common usage as module interconnections, PHH are not yet quantified as RF transmission elements. To use the full capabilities of the modular approach, investigations in this field of view are needed. So the primary objective of this study is to comprehensively evaluate their applicability and effectiveness in terms of reflection parameters and transmission losses in this domain.

B. Via interconnects

Numerous studies have been published, investigating the profound impact of geometry variations in via interconnects within the RF domain [5][6][7]. These studies show relationships between PTH interconnect geometries - such as via diameter, length, and spacing - and their consequential effects on signal integrity, impedance matching, and overall RF circuit performance. Findings from these studies were used to understand and examine the influences of design parameters and the importance of well-defined return current paths.

II. Modeling and Simulation

In order to examine the usage of PHHs as RF interconnects, an investigation on which design parameters are typical for modules with castellated holes was conducted and used as a baseline for a virtual model. The primary goal is to explore the performance of the baseline model in the targeted frequency range, represented by S-Parameter with S11 for the reflection and S21 for the transmission. As secondary object an optimization of various design parameters for the baseline model is targeted. Based on this, the optimized virtual model should be transferred back to reality in which an optimized PHH design is to be created, manufactured and measured.

A. Simulation model

For the investigation of the high-frequency behavior of PHH, full wave simulations based on the finite element method (FEM) were performed in this work. This method provides the possibility to detect and observe local effects such as near-field coupling and impedance matching, which are critical in high frequency applications. In particular, the simulation software Ansys HFSS V 2023.1 was used for this purpose. As simulation results, the S-Parameters were analyzed and evaluated. As the solution setup, the Driven Modal solution type was employed. The simulation was carried out at a frequency of 40 GHz, employing a maximum of 15 passes and a targeted Delta S of 0.002.

In order to create a realistic scenario, a model consisting of two boards was designed, shown in Fig.1. The upper board features the PHH while the lower one provides the landing pads where the vias are soldered. To excite the signal properly, a short 50 'n impedance-matched grounded coplanar microstrip line was introduced for providing a connection between the PHH and the waveports as well as serving as contact pads for the later measurements with GSG probes. While this arrangement induced losses to the microstrip line, effective matching ensured that these losses remained within a few hundredths˜ decibel up to 40 GHz. In the subsequent measurement phase, these lines served the purpose of contacting the sample with the GSG probes.

As a typical RF design setup, a six-layered stack up was used while the upper substrate layer serves as the RF layer. Megtron 7 was therefore chosen as high frequency laminate, a commonly used material in RF applications due to its constant dielectric constant of 3.31 from 14 to 59 GHz [1] and exceptionally low loss tangent of 0.0025 at 14 GHz respectively 0.0028 at 36 GHz. As substrates for the layers below standard FR4 laminates were used. The RF substrate layer has a thickness of 300 ı m while the FR4 layers have a thickness of 200 ı m each. As a standard configuration for modules with castellated holes, a via diameter of 1 mm and a

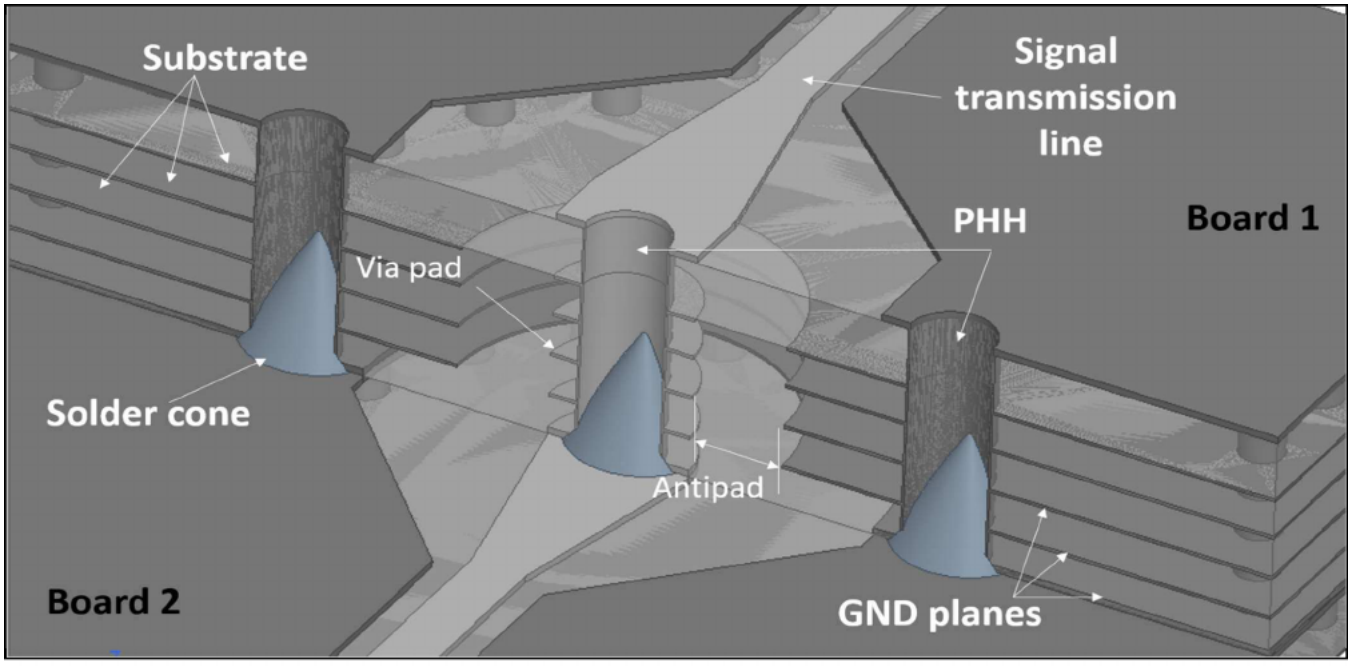

Fig. 1: Simulation model of a 6 layered and a 2 layered PCB with PHH, solder cones, and transmission line

[1] Panasonic Industry, Megtron7 Laminate R-5785(N) Datasheet, No. 22040127, pp. 2-3, Apr. 2022

pitch of 2.54 mm were used. The via pads have a restring of 125 µm and the antipads a gap of 150 µm. Additional shielding vias with a diameter of 200 µm were distributed strategically within the PCB.

A separation of 10 µm was established between the two boards models in vertical direction to represent the separation of the boards after the soldering process. To provide a realistic electrical connection between those two boards, solder cones (Solder Lead-Free Sn-3.5Ag with 8.12×10^6 siemens/m) were introduced as a simple approximation to the later experimental situation.

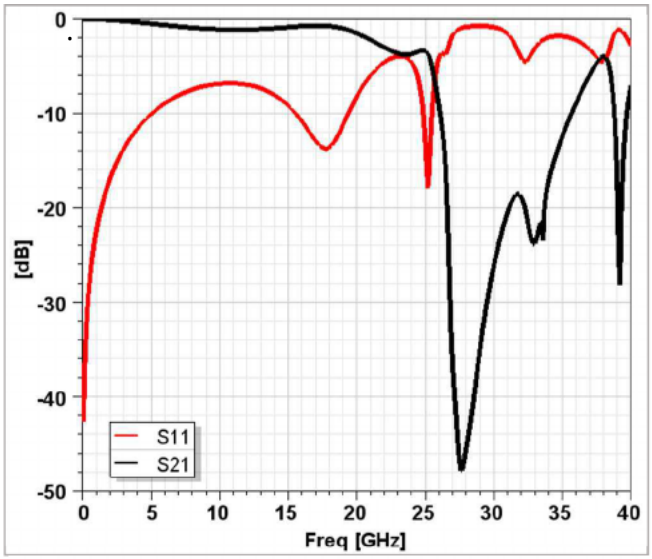

Fig. 2: Simulation results for standard PHH design values

The simulation shows a decent result for S21 (transmission) in a frequency range up to 25 GHz with less than -2 dB and -1 dB up to 20 GHz (Fig. 2). However, the S11 parameter shows rather unsuitable values with crossing the crucial -10 dB limit already at 5 GHz. For frequencies higher than 25 GHz this PHH configuration is completely unusable due to the high transmission losses and reflection, represented by S21 and S11 respectively. In [6] it was described, that these drops result from resonances occurring due to uncontrolled return currents.

B. Optimization by design parameter variations

To achieve better transmission performance by adjusting various design parameters, the specifications of PCB manufacturers for a conventional production process were considered to reach a realistic set-up and provide a practical relevance. In order to avoid reaching a multitude of solutions by examining a seemingly random variety of parameters and their combinations, a more methodical approach was chosen in which certain solutions were already determined from previous findings, so that the number of parameters to be varied is limited to a few.

In order to reach a S21 of better than -3 dB and a S11 of less than -10 dB over the whole frequency range, first measures were taken to ensure that the return current path is as short and homogeneous as possible, based on the results of previous studies [4][7]. For this purpose, the smallest possible via pitch for the PHH of 1.5 mm according to standard manufacturing guidelines was selected.

In order to reduce impedance mismatches and current path discontinuities in the transition between PHH and transmission line, the smallest possible via diameter, which is 400 µm was chosen. By setting the viapad width of 125 µm restring to a uniform and smallest possible value across all layers, several aspects are taken into account: Firstly, like mentioned above, the transition to the microstrip line is more advantageous since the latter is narrower than the viapad itself. On the other hand, it results in the via having a symmetrical structure, which leads to fewer discontinuities and achieves greater stability in the event of later production.

The remaining parameter that needs to be considered in this approach is the antipad diameter. An antipad stands for the distance between the pad and the pad surrounding ground plane in an inner layer. In detail the hereinafter mentioned diameter dimensions the outer diameter in the ground plane, while the inner dimeter is given by the via pad (see fig. 1). There are four inner layers whereby it is assumed that the two middle ones are also to be treated uniformly, which was checked with a short validation. This leaves the antipads on layer 2, layer 3 and layer 5, whose variation in diameters should be investigated. In the following, the antipad is described by its radius, starting from the center of the vias they surround.

The simulation result for the antipad radius combinations optimized by themselves and together are given as S21 in Table I; some specific are plotted in Fig. 3.

TABLE I. S21 FOR SPECIFIC ANTIPAD RADII

Antipadradius [µm]			S21 [dB]	
Layer 2	Layer 3 & 4	Layer 5	20 GHz	40 GHz
675	750	900	-0.38	-1.52
675	675	675	-0.46	-1.21
675	550	550	-0.64	-1.15
675	425	425	-1.25	-3.05
550	675	675	-0.4	-1.78
550	550	550	-0.576	-1.36
425	425	425	-1.06	-3.72

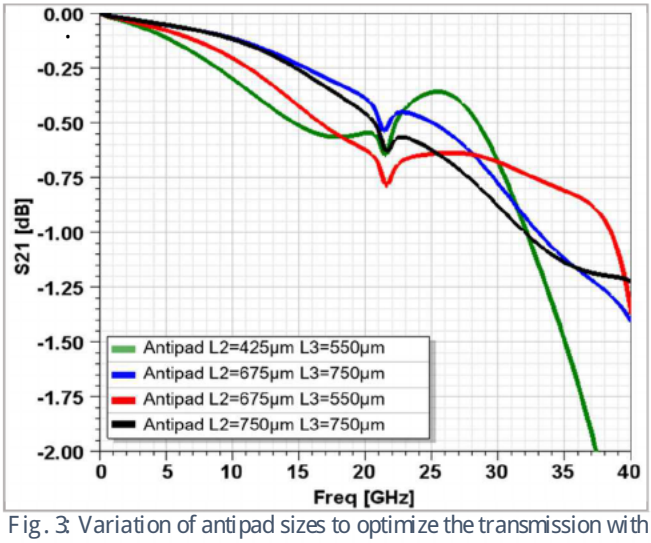

Fig. 3: Variation of antipad sizes to optimize the transmission with antipad diameter in layer 5 of 675 µm

Due to the considerations mentioned above and the simulation assisted optimization of the antipads a remarkable improvement of the transmission performance represented by S21 could be achieved. With optimized parameters the limit value of at least -3 dB can be maintained over the entire frequency range. The best values are ranging at -0.5 dB at 20 GHz and -1.2 GHz at the upper frequency range.

The sharp drop of S21 at around 21.3 GHz is an indicator that at some point in the system starts to resonate. It reveals one crucial point in this construction: The area in between both boards. Their only junction are the three soldering areas where the PHHs from the upper board are connected to the pads of the lower board. The two outer PHHs are connected to GND and providing the return current path. The area between the two boards acts like parallel plate capacitors, while the solder connection represents an inductance. At resonance frequency, return current is floating via displacement current through this gap and incite standing waves at resonance frequency. Depending on the height, surface condition and the lateral expansion, the impedance can be changed und thereby shifting the resonance frequency.

Parallel plate modes need to be avoided or reduced at the target frequency since they can cause a strong radiation of the PCB which would lead to serious EMI problems and a strong degradation of the transmission signal at this specific frequency as it is been shown in Fig. 4.

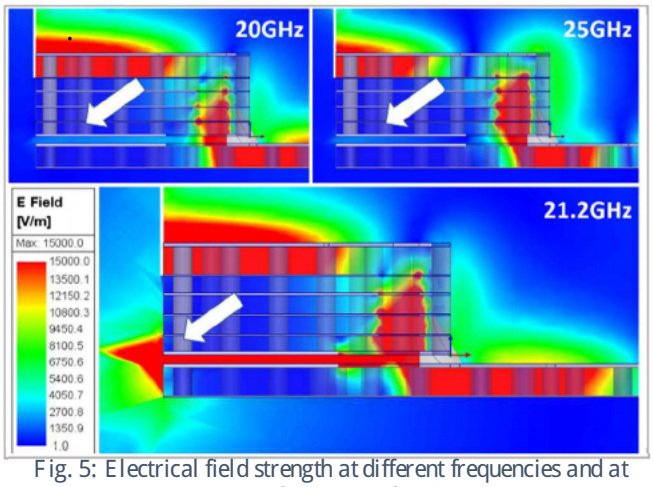

Fig. 5: Electrical field strength at different frequencies and at resonance frequency of 21.2 GHz

The parallel plate modes can be influenced by adding additional GND connections between both boards near the signal path to reduce the return current discontinuities. For PHH technolog this is only possible by adding additional connections in this area at the lower board. Due to its lack of feasibility with a focus on keeping the design as simple as possible, this approach is just mentioned here but not pursued further. Changing the size of the parallel plate section is another possibility to influence the resonances. By changing their overlapping areas, we can can reduce the strength of the signal degradation or shifting the resonance frequencies into more uncritical areas (Fig. 5), which becomes relevant in development practice when just specific frequencies are used. In practice a decrease of the overlapping area can be reached by a cavity underneath the RF board.

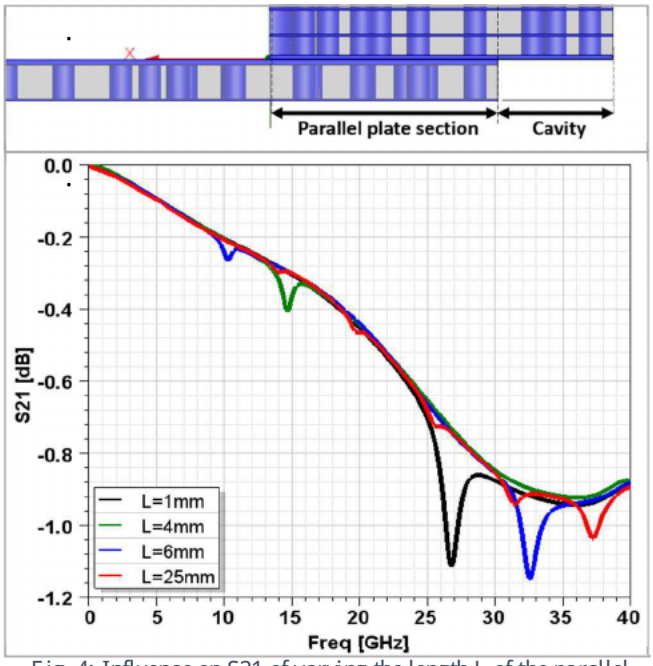

Fig. 4: Influence on S21 of varying the length L of the parallel plate section

C. Consideration of unintendet parameter variations

Fig.6 shows a typical via interconnect with surrounding copper and substrate layers. The drilling process and subsequent plating leads typically to non-exact via diameters. The offset of via to the previously manufactured pads in the individual layers can be up to 50 µm. Additional smearing effects and copper erosion caused by the milling process in order to create the PHH are difficult to represent in a simplified model and can therefore not be considered in the simulations. Additional factors such as the etching factor and the inherent tolerances of the lithography process can

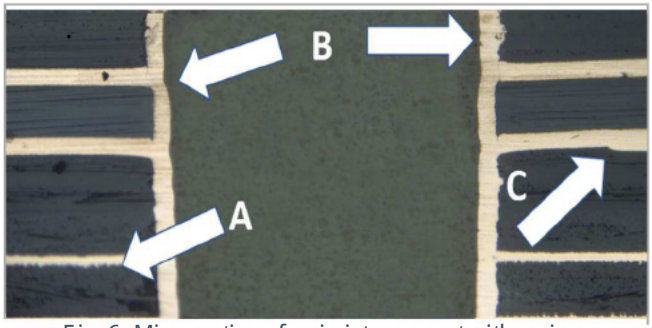

Fig. 6: Microsection of a via interconnect with various manufacturing effects. A: Increased roughness in a single layer B: Discontinuities in via cylinder C: Discontinuities in copper layer

contribute to the degradation of the originally designed structures and the resulting PCB samples. These cumulative effects have the potential to collectively influence the final performance of PCB samples beyond the confines of idealized simulations.

Surface roughness emerged as a relevant factor [8], initially ignored in the model for simplicity. Subsequent investigations revealed a certain impact, shown in a comparative simulation of a 6.8 mm long coplanar microstrip line - representing the overall transmission line length in the PHH model - simulated with different surface roughness models: Huray Surface Roughness Model (Nodule

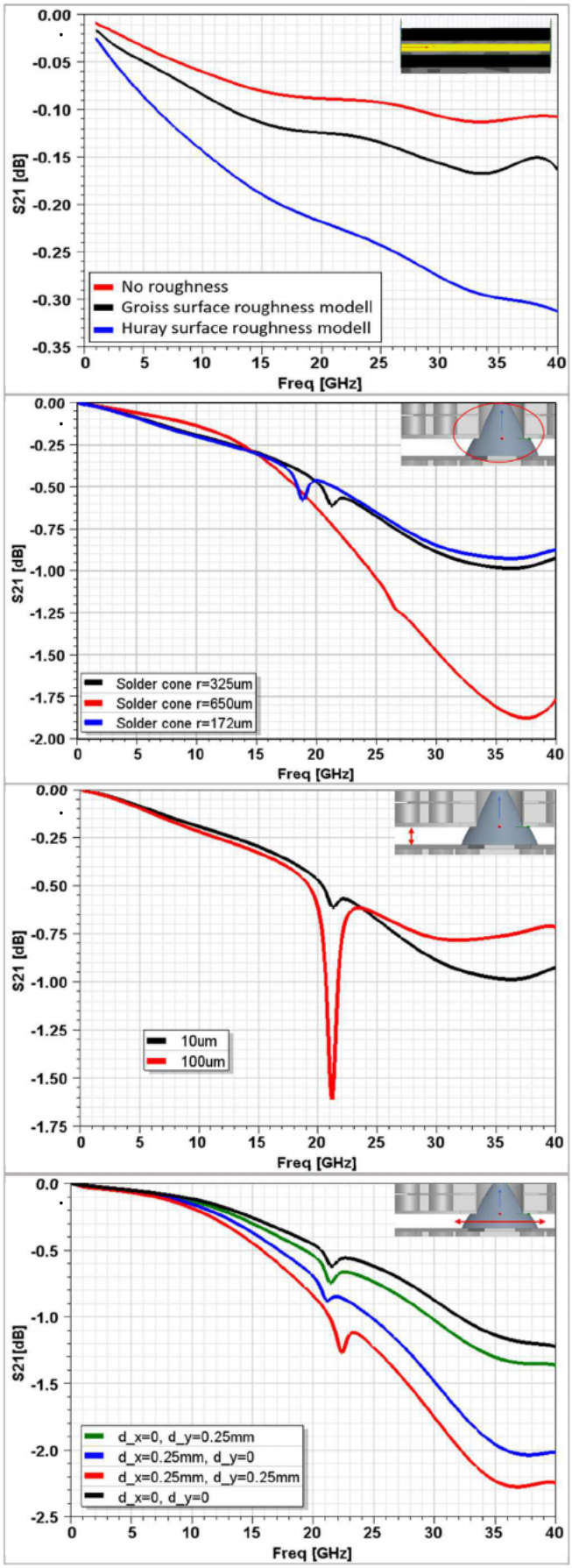

Fig. 7: Simulation results of manufacturing tolerance parameters. a) surface roughness of a microstrip line b) solder mass c) airgap d) misalignment between boards

Radius=2 ı m, Hail-Huray-Surface-Ratio =2.9) and the Groiss Surface Roughness Model (Surface roughness=2 ı m). Clearly, roughness has a impact on transmission losses of around 0.1 to 0.2 dB in the simulated frequency range, confirming its importance (Fig. 7a).

The assembly process will lead in the reality to problems with accurate component alignment, solder distribution and overall solder quality. To quantify the influences of the solder mass distribution, a simulation was done with different sized solder cones. The influence of this can be shown by varying the diameter of solder cone. In the frequency range considered here, a doubling of the losses can be observed over most of the range, with an absolute increase in transmission loss of about 1 dB at the upper end of the frequency range for a bigger solder mass distribution. Decreasing the solder mass size has es smaller effect on the transmission characteristics though we observed a small performance increase in the lower half of the frequency range and a better one in the upper half (Fig. 7b).

We have identified the gap between the two PCBs as another possible cause of a change in transmission behavior, which can occur if the PCBs are not placed exactly on top of each other, for example due to warping, coatings on the PCBs in other areas or an inaccurate soldering process. Therefore, a simulation was conducted to investigate the influence of changing the airgap (Fig. 7c). In the lower frequency range, minimal differences are observed. However, in the vicinity of the resonance frequency described earlier, a noticeable deterioration of the transmission quality occurs.

At the higher end of the considered frequency range, the changed parallel plate capacitance resulting from the larger gap actually improves the transmission behavior by up to 0.25 dB in comparison to the smaller gap.

Further investigations were carried out to evaluate the influence of misalignment of the two boards, a typical source of error caused by manufacturing tolerances from manual assembly. A simulation setup was created in which the lower PCB was either shifted laterally (y-direction), forward or backward (x-direction), or a combination of both. The displacement value was assumed to be 250 ı m. The simulation results indicate a clear influence on the transmission behavior. A shift in the y-direction has a stronger influence than x-direction, since discontinuities in signal propagation direction having a stronger effect. A slight shift in the resonant frequencies can also be seen (Fig. 7d), caused by the changed current path and impedance in the area of the return vias and the transition between both boards. In the upper range of the frequencies considered here, there is a significant degradation of the transmission performance of up to 1.1 dB additional losses for a simultaneous misalignment in both directions.

These investigations show that in some scenario˘s significant deviations from the idealized simulation model are to be expected in a realistic setup. The large number of parameters and possible sources of error and their mutual amplification and compensation do not allow an exact simulation of the test samples and mean that only an expected range of transmission losses can be given. It could be shown that this influence is clearly noticeable, but through a proper optimization of the PHH model based on the design parameters considered above, compliance with the limits of -3dB for S21 is achievable despite negative influences that cannot be influenced by the design.

III. Measurment and discussion

In order to prove the applicability of the PHH we have also conducted measurements in the considered frequency range. Therefor a board set up was created, which included a selection of PCBs with different structures to cover the range of variation that includes several variations of the pad/antipad ratios as well as variations in line width and different solder mask configurations (Fig. 8).

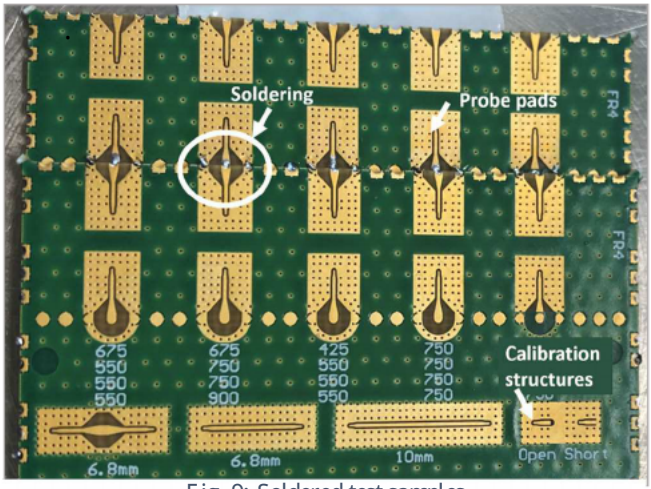

Fig. 9: Soldered test samples

It consists of the layer stack up described in the previous chapters with Megtron7 on top and 4 FR4 substrate layers. In addition, structures were applied for calibration and comparative measurements. They were manufactured in a standard process, also to ensure their practicality for possible future applications. The samples were subsequently soldered manually with a standard soldering station.

High-resolution S-Parameter measurements were carried out using the Keysight PNA-X Series Network Analyzer instrument with the Millimeter Test Set and the LRRM Calibration to test the actual S parameters of the PHH, utilizing 250ı m GSG probes. The frequency range considered was 1 to 40 GHz, with a monitored IF Bandwidth 30 Hz (Fig. 9).

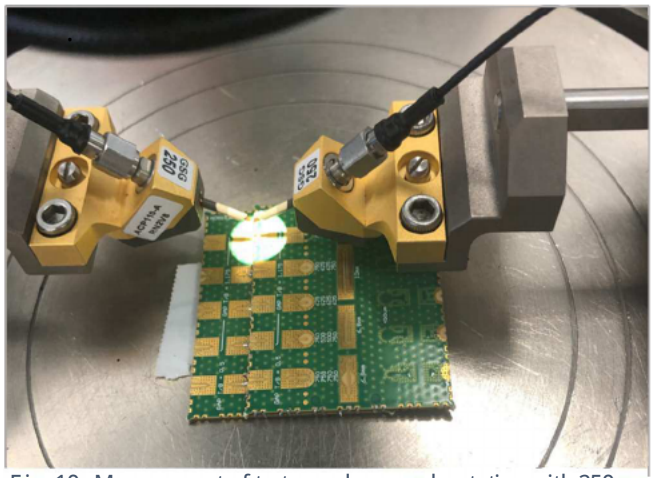

Fig. 10: Measurement of test sample on probe station with 250um GSG probes

To quantify the quality of the PCB and the test setup we measured the 6.8 mm microstrip line on the test sample, which corresponds to the total length of the test set-up of the test structures excluding the PHH. For the Megtron 7 we are ranging at 0.1 to 1.4 dB transmission losses (S21) and a maximum of -10 dB reflection (S11) at 33.4 GHz (Fig. 10).

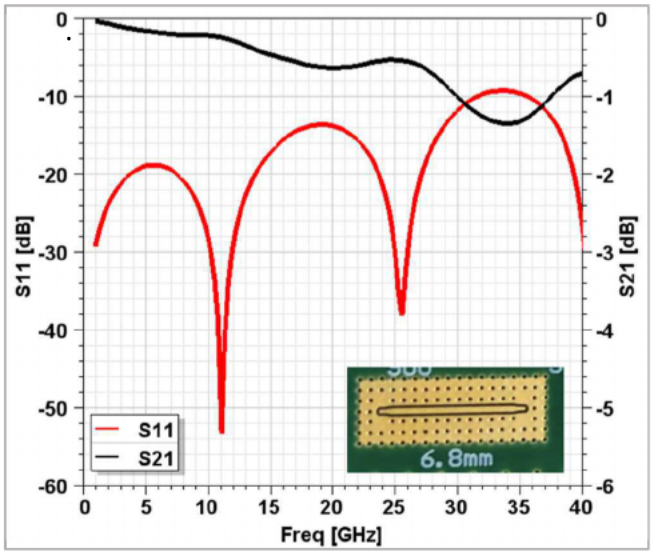

Fig. 8: S11 and S21 parameters of the transmission line

Subsequently the PHH structures were measured. Here we distinct between optimized und unoptimized structures to reach a comparability of the various design parameter and their improvements, based on the findings from the simulation analysis. Optimized means, according to simulation results, a improved viapad-antipad ratio to provide a proper distribution of the electrical field and currents in the PCB. Be varying the radii of the antipads in different layers, the improvement in the transmission results could be increased, so different variations of combinations of antipads were used, following referred as `antipads equal_ and `antipads vary_ configuration.

The measurement of the PHH structures themselves gives a good approximation to the performance in the observed frequency range according to the simulation results, so the S21 ranges about -1 dB at 20 GHz and -1.5 to -2 GHz at the upper side of the range for the optimized structure and is therefore significantly better than the target limit of -3dB as it is been shown in Fig. 11. The reflection, represented by the S11, ranks below the limit value for the optimized structure with equal antipads, in this case 625ı m. Comparing this with the measurement on the pure microstrip line of the same length, it can be shown that the signal degradation due to the PHH can be significantly reduced through an appropriate design of it. The conducted measurements show clearly, which improvement can be done by optimizing the design parameter of PHH, even more if the single antipads were optimized. However, even the unoptimized structures in terms of antipad radii are showing acceptable values for a frequency range up to 30 GHz.

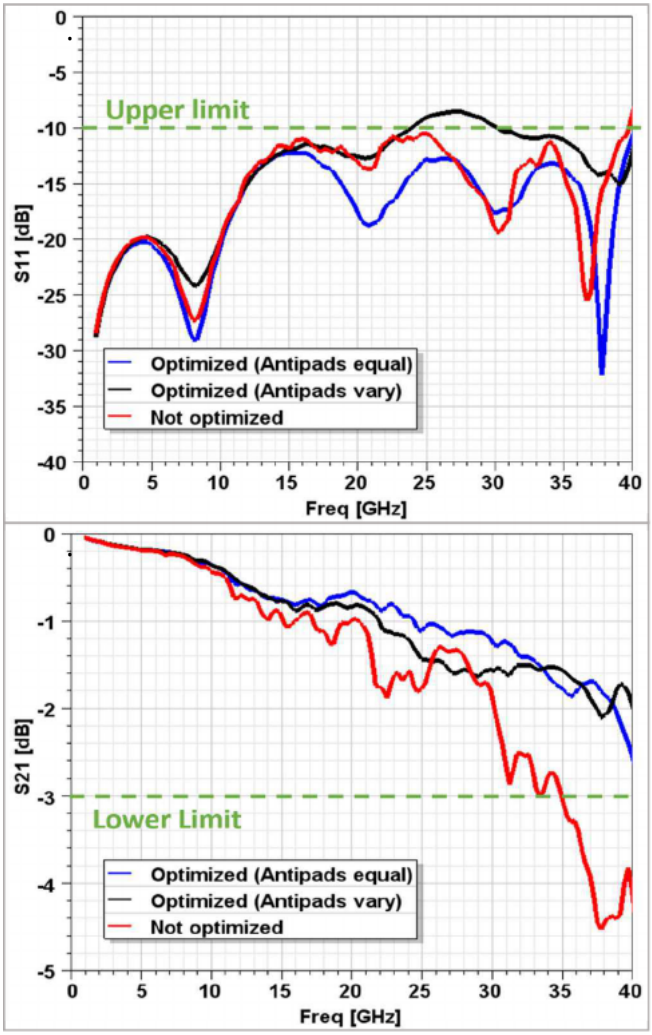

Fig. 11: Measurement of a) S11 (reflection) and b) S21 (transmission) of the optimized and not optimized PHH test samples

IV. Conclusion

In this study it could be demonstrated that the integration of Castellated Holes as RF interconnections for board-to-board transmission element up to 40 GHz is a viable option. The simulations on an idealized model show a good performance with losses of around 1.5 dB at 40 GHz which is comparable to other connection methods like BGA board-to-board soldering or the usage of connectors. Furthermore, measurements confirm that a S21 of around -1 dB at 20 GHz respectively 2 dB at 40 GHz are feasible with the optimizations described here. The insertion, represented by S11 could be significantly reduced to values below -10dB compared to not optimized structures. With this results a good alternative for board-to-board connections could be evaluated, which provide a powerful feature for modular design of RF applications in terms of cost efficiency and design effort. Further design improvements to increase the efficiency were suggested but need further research as well as examinations in order to widening the frequency range.

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