Assembly of Ultra-thin MEMS Device on Driver Chip Using Anisotropic Conductive Film

Hoang-Vu Nguyen
Department of Microsystems
University of South-Eastern Norway
Borre, Norway
hoang.v.nguyen@usn.no

Knut Eilif Aasmundtveit
Department of Microsystems
University of South-Eastern Norway
Borre, Norway
Knut.Aasmundtveit@usn.no

***Abstract*—Assembly solution for large-area, ultra-thin, MEMS-based transducer array dies on driver chips has been investigated using dummy Si dies and substrates. The dummy dies have a thickness of 50 µm, a bonding area on the order of 100 mm^2 populated with more than a thousand through-silicon vias connecting corresponding metal pads and redistribution layer (RDL) on both sides. The dummy substrates have conventional thickness as well as necessary RDL and pads for bonding and monitoring electrical resistance and stray capacitance of interconnects. Flip-chip interconnection technology based on anisotropic conductive film (ACF) was selected for bonding and characterization. Handling and ACF bonding of ultra-thin dies to rigid substrates were eased by means of glass carriers attached to the inactive side of the dies. Proper bonding parameters were identified, providing sufficiently low interconnect resistance with satisfactory yield. Stray capacitance of interconnects was found in acceptable range, though lower stray capacitance should be further pursued. The results from this work have demonstrated the feasibility of using ACF for assembling large-area, ultra-thin dies on rigid substrates.**

Keywords—ultra-thin dies, MEMS, assembly, ACA, ACF

I. Introduction

The demand for ultra-thin dies in applications such as stacked 3-dimensional (3D) packages, integrated circuit (IC) card, flexible hybrid electronics has been increasing considerably in the recent decade [1, 2]. Such ultra-thin dies, with a thickness of 50 µm and below, include IC chips and micro electro-mechanical systems (MEMS) sensors. The assembly of such dies on substrates is challenging in terms of handling, high-yield bonding, and reliable integration [3-5]. While soldering combined with underfilling has been the main solution for stacking 3D packages [1], anisotropic conductive adhesives, either in form of film (ACF) or paste (ACP), are common for assembling thin dies on polymer-based substrates in flexible electronics [2, 3, 6].

The present work investigates the assembly of MEMS-based capacitive micromachined ultrasound transducers (CMUT) for medical imaging applications. Such transducers are normally arranged in a 2D array with an extremely high number of elements (typically several thousand) on a large-area Si die in order to obtain high-resolution 3D images in real time. Since each transducer element needs a dedicated electrical connection to driver electronics, fanning out a high number of connections to the peripheral area of a sensor die for conventional wire bonds becomes impractical. Therefore, CMUT array with through-silicon vias (TSVs) connected to interconnection bumps/pads on the other side of a die for flip-chip integration is a proper solution [7-9]. Such sensor dies normally have a thickness below 50 µm, to ensure short-distance electrical connections for sufficiently low stray capacitance and enhanced temporal resolution. Stray capacitance caused by individual interconnects, which is in parallel with transducer element capacitance, must be reduced as much as possible to achieve good receive sensitivity and preserve wide bandwidth, particularly for 2D array elements with very low device capacitance [9, 10].

A sensor die with a CMUT array needs to be integrated with a driver chip (ASIC – Application Specific Integrated Circuit) via short-distance interconnections. Flip-chip bonding a sensor die to an ASIC chip with extremely high number of I/Os is thus a proper solution. Since there are similarities between ultra-thin CMUT dies and Si interposers, the results obtained in this work could also be applied for bonding IC chips to Si interposers. Possible flip-chip bonding techniques include solder reflow, metal-metal thermocompression bonding, and anisotropic conductive film (ACF). ACF is of particular interest because it provides electrical connection, mechanical strength and sealing/underfilling in a quick bonding process. In addition, ACF bonds could be obtained at moderate bonding temperatures and pressures. The technology has also demonstrated high bond yield and reliable interconnects in relevant applications, such as chip-on-glass, chip-to-chip [11-14].

This work addresses ACF bonding process of large-area, ultra-thin transducer array dies to ASIC chips. Processes providing high bonding yield, sufficiently low electrical resistance and low stray capacitance for individual interconnects are of interests. Bonding and characterization are performed using dummy Si dies and substrates mimicking the transducer dies and ASIC chips. The dummy dies have ultra-low thickness, and TSVs connecting corresponding metal pads and redistribution layer (RDL) on both sides. The dummy substrates have conventional thickness as well as necessary RDL and pads for bonding and monitoring electrical resistance and stray capacitance of interconnects. While electrical resistance could be measured using conventional methods, stray capacitance of individual interconnects is defined as the capacitance between an ACF interconnect with its corresponding TSV and bulk Si.

II. Experimental

A. Test samples

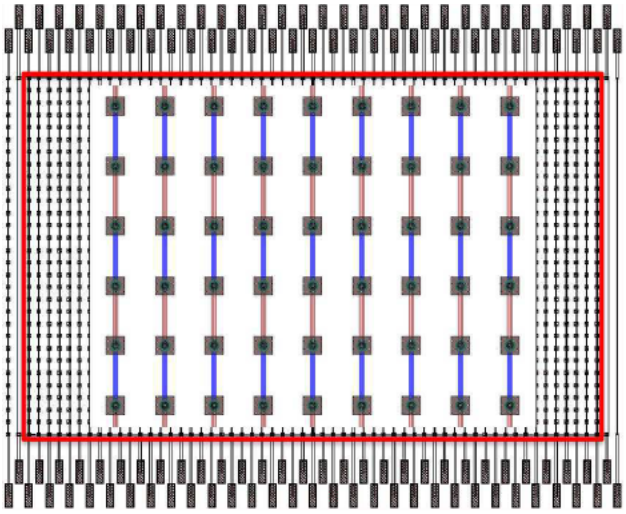
Dummy transducer array dies were fabricated on highly doped Si wafers with SiO_2 as isolation layer on surface, targeting an active area on the order of 100 mm^2 and a thickness of 50 µm. One side of the dies are populated with Ni/Au-electroplated bumps, each electrically connects to Al

Funding agency: Research Council of Norway through the project "Frontend and transducer technology for next generation cardiovascular ultrasound probes" (project number: 317769)

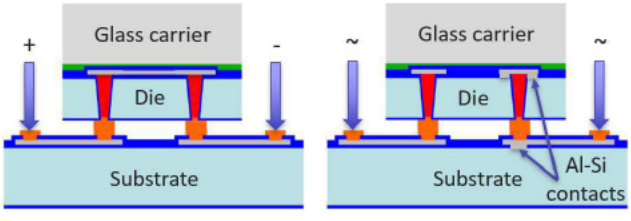
RDL on the other side by means of a Cu-filled TSV. The bumps are 50 µm in diameter, 15 µm high, and distributed in form of m-by-n matrix with bump pitch in the range of 200–400 µm. Direct contacts between Al pads and bulk Si were realized at dedicated locations on the RDL side to enable stray capacitance measurements. Due to the ultra-low thickness, all dies were attached to individual glass carriers by means of a transparent adhesive, which would be detached after bonding.

Dummy substrates were fabricated on highly doped Si wafers with a thickness about 750 µm. SiO_2 was also used as isolation layer on the substrates' surface. Bond pads are composed of Ni/Au electroplated to dimensions of 80 µm x 80 µm x 15 µm, and distributed correspondingly to the bumps on dummy dies. In addition, the substrates also have probing pads for measurements of electrical resistance and capacitance. Direct contacts between Al pads and bulk Si were also found at dedicated locations on substrates to enable stray capacitance measurements.

Test samples comprise a dummy die bonded to a dummy substrate. The dies and substrates were designed and configured to form 57 daisy chains, each with 30 interconnects. Fig. 1 shows (a) the layout design of corresponding dies and substrates, as well as illustration of measurement concepts for (b) electrical resistance and (c) stray capacitance.



(a) Layout of a die (marked with a red rectangle) overlapping a substrate. Each column is a daisy chain of interconnects. The inset shows a zoom-in of circular die bumps and square substrate pads, in addition to Al RDL on both parts.



(b) Concept for measuring electrical resistance of daisy-chained interconnects

(c) Concept for determining stray capacitance between interconnects and bulk Si

Dimensions are not to the scale.

Fig. 1. Designs of dies and substrates for measurements of electrical resistance and stray capacitance of interconnects

B. *Bonding and characterization*

A commercial ACF product from H&S HighTech Corporation was used in this work. The ACF is single-layer film with a thickness of 35 µm and contains Ø5 µm Ni/Au coated monodisperse polymer spheres. ACF bonding of a dummy die to a dummy substrate was carried out using a flip-chip bonder Finetech FinePlacer pico. Bondline temperature was characterized using flat thermocouples inserted between a die and a substrate during a bonding process without ACF applied. A conventional ACF bonding process, with two main steps: i) pre-tack ACF on a substrate's surface, and ii) final bonding of a die to a substrate, was applied. Bonding pressure was the main varying parameter whereas bonding temperature and bonding time were selected as 180 °C and 30 seconds, according to recommendations of the ACF supplier.

Bonded samples were characterized by means of electrical resistance of daisy chains and bonding yield. The daisy-chain resistance was measured using two-point probe method with a Fluke 73 digital multimeter. The resistance of probe wires and needles was found negligible compared to the measured resistance of each daisy chain. For each bonded sample, there are a total of 57 daisy chains being measured. Bonding yield of each group of samples bonded at different pressures was determined by dividing the number of interconnects with sufficient conductance by the total interconnects of all samples in that group. As the highest resolution of probing is 30 interconnects in a daisy chain, all interconnects were claimed open if an open circuit happened to the chain.

Stray capacitance of individual daisy chains was obtained by measuring impedance of the entire chains. The impedance measurements were performed using a Keysight impedance analyzer E4990A, with one probe connecting to the entire chain and the other probe connecting to bulk Si thanks to the direct Al-Si contacts. Since the resistance of highly doped bulk Si is negligible as compared to the measured impedance, stray capacitance of individual daisy chains could be calculated from the impedance measurement results. Stray capacitance of individual ACF interconnects and its corresponding TSV was then estimated based on the values obtained for the daisy chains.

III. Results

Test samples were bonded with bonding pressures varied from 2 MPa to 5 MPa. At each bonding pressure value, 5 samples were manufactured. The visual inspection of all bonded samples revealed no cracks on the ultra-thin dies after bonding. Fig. 2 shows a typical sample after ACF final bonding.

Fig. 3 shows effect of bonding pressure on electrical resistance of individual daisy chains, each comprising 30 interconnects. Considering even distribution of bonding pressure, and hence electrical resistance of individual interconnects in a daisy chain, the results in Fig. 3 also indicates impact of the bonding pressure on ACF interconnect resistance. The daisy-chain resistance decreases gradually with increasing bonding pressure from 2 MPa to 3 MPa. When bonding pressure is over 3 MPa, its impact on daisy-chain resistance is minor. Furthermore, the deviation of daisy-chain resistance increases considerably at bonding pressures higher than 3 MPa.

Bonding yield corresponding to different bonding pressures is shown in Table I. Better bonding yield is obtained

when bonding pressure is increased over 2 MPa. However, the yield remains stable at about 85–87% for bonding pressures in the range of 3–5 MPa. Daisy chains with failed interconnects were observed at random locations from samples to samples. No systematic failures were recognized.

Impedance measurements were applied for a limited number of individual daisy chains on samples bonded at 3 MPa. Note that only daisy chains with proper electrical connection of all interconnects were of interests. The results showed relatively stable capacitive reactance of individual daisy chains of about 5.8 kΩ at 1 MHz. This corresponds to a capacitance of about 27.4 pF.

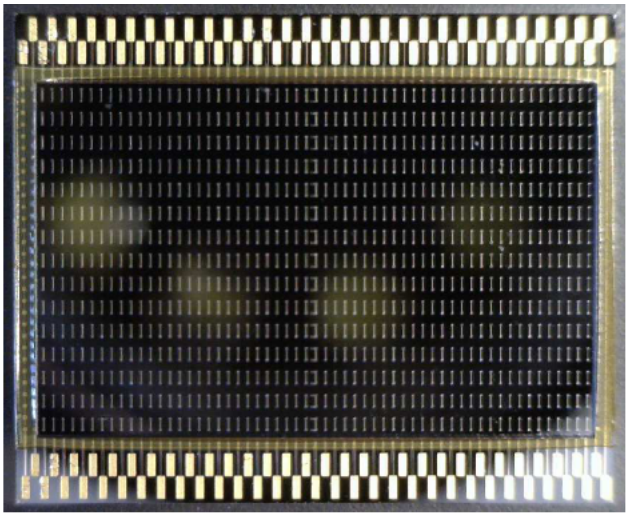


Fig. 2. Example of a test sample bonded at 3 MPa

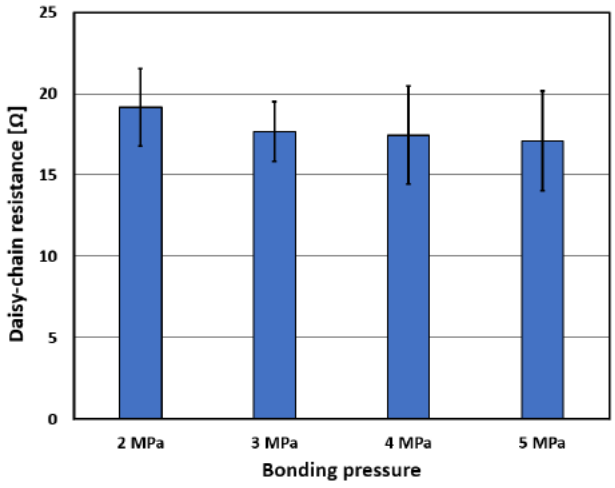


Fig. 3. Effect of bonding pressure on electrical resistance of individual daisy chains, each comprising 30 ACF interconnects

TABLE I. BONDING YIELD OF SAMPLES BONDED AT DIFFERENT BONDING PRESSURES

	Bonding pressure			
	2 MPa	**3 MPa**	**4 MPa**	**5 MPa**
Bonding yield	73.7 %	85.1 %	87.3 %	86.8 %

IV. DISCUSSION

Electrical resistance of daisy chains presented in Fig. 3 includes resistance of Al RDL and Cu-filled TSVs that belong to individual chains. The resistance of all Al RDL in a chain was measured in practice by means of dummy chains designed for this purpose. The measurement results agree very well with the estimated values based on dimensions of Al tracks. By deducting the Al-RDL resistance, the correlation between electrical resistance of individual interconnects and bonding pressure were obtained, as shown in Fig. 4. Note that the resistance values in Fig. 4 are contributed from ACF interconnects and its corresponding Cu-filled TSV. By using TSV dimensions and electrical resistivity of pure Cu, the electrical resistance of individual TSVs was estimated in the range of 5–17 mΩ, being insignificant as compared to the resistance values presented in Fig. 4. These values thus represent ACF interconnect resistance.

Bonding yield shown in Table I is considered conservative. It is because all 30 interconnects in a daisy chain were considered as open circuit even if only 1 interconnect in that chain failed. In addition, failures in a daisy chain might stem from individual ACF interconnects and/or TSVs. The ACF bonding yield in practice is thus expected to be far better than the values presented in this work.

Failures were observed at random locations from samples to samples. This indicates a proper setup of bonding equipment. Failures seem to stem from the ACF bonding process as well as the fabrication of TSVs. Further work on failure analyses, such as cross-sectional microscopy, is crucial to identify the root causes of failed interconnects in bonded samples.

The interconnect resistance in Fig. 4 and bonding yield in Table I indicate 3 MPa as a proper bonding pressure within the pressure range tested in this work, providing sufficiently low interconnect resistance with moderate deviation as well as satisfactory bonding yield. ACF interconnect resistance obtained at this pressure value is in the range of 110–240 mΩ, in accordance with results from previous studies of ACF assemblies for chip-on-glass, chip-to-chip, chip-on-flex, chip-on-board, and several MEMS applications [12-16].

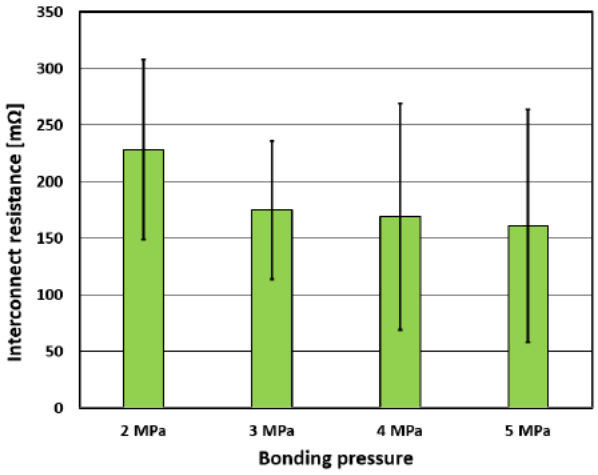


Fig. 4. Interconnect resistance versus bonding pressure

Capacitance of daisy chains with full connection was found to be about 27.4 pF. Since this result was obtained from measured impedance of a limited number of daisy chains on samples bonded at 3 MPa, the following interpretation is considered preliminary. Based on the dimensions of Al RDL as well as thickness and dielectric constant of SiO_2 layer, the capacitance of all Al RDL is estimated to be about 11.2 pF. Hence, the capacitance of 30 interconnects and TSVs in a chain is about 16.2 pF. That means stray capacitance of individual ACF interconnects and its corresponding TSV is about 0.5 pF. Whether such a stray capacitance is acceptable depends on the capacitance of individual CMUT elements used and its driver electronics. Previous studies specified element capacitance about 1 pF [10] or acceptable stray capacitance from electrical connections up to 1.7 pF [9]. This indicates that the interconnect stray capacitance obtained in this work might be acceptable. However, lower stray capacitance should be further pursued.

The assembly process employed in this work has demonstrated the ease of handling ultra-thin dies by means of glass carriers. No cracks were observed, even for samples bonded with as high as 5 MPa. Compared with handling of bare ultra-thin dies, which are common in assembly of flexible hybrid electronics [2, 3, 17, 18], the use of glass carrier indeed facilitated handling and ACF bonding of ultra-thin dies to rigid Si substrates. This solution also offered risk mitigation for squeezed-out ACF that might adhere to, and hence damage bonding tool during assembly process. No special treatment and additional steps are needed for protecting tool surface under ACF bonding. However, the use of glass carriers demands one extra step and instrument for removing the temporary adhesive used between the carriers and the ultra-thin dies after bonding. The observations in this work are in line with previous results reported by Huang and Lu [19], where ACA bonding of ultra-thin dies using rigid carriers provided considerably improved electrical performance and reliability of the assemblies, compared to the same process applied for bare ultra-thin dies.

V. Conclusion

ACF bonding process of large-area, ultra-thin Si dies to Si substrates was characterized. The dies have a thickness of 50 µm and a bonding area on the order of 100 mm^2 populated with more than a thousand TSVs connecting corresponding metal pads and RDL on both sides. The substrates have thickness of 750 µm as well as necessary RDL and pads for bonding and measuring electrical resistance and stray capacitance to bulk Si of interconnects.

Use of glass carriers attached to the inactive side of dies ensured proper handling and reliable ACF bonding of ultra-thin dies to rigid substrates. No cracks on dies were found on bonded samples, even with a bonding pressure as high as 5 MPa. No risk of bonding tool being damaged due to ACF squeezed out under bonding.

While bonding temperature and bonding time are kept fixed at 180 °C and 30 seconds, bonding pressures from 3 MPa and above are recommended. However, 3 MPa seems to be the proper bonding pressure in this work, providing sufficiently low interconnect resistance with moderate deviation (~110–240 mΩ) as well as satisfactory bonding yield. Stray capacitance of individual ACF interconnects and its corresponding TSV to bulk Si was found about 0.5 pF, which might be in acceptable range for MEMS-based ultrasound transducer applications, though lower stray capacitance should be further pursued.

ACF flip-chip technology was found feasible for assembling large-area, ultra-thin dies on rigid substrates. This applies for not only bonding MEMS-based ultrasound transducer array dies to ASIC chips, but also bonding IC chips to rigid interposers.

Acknowledgment

The authors thank Hoang Duy Le and Lars Hoff, both with University of South-Eastern Norway, for their assistance in impedance measurements. The Research Council of Norway is gratefully acknowledged also for the support to the Norwegian Micro- and Nano Fabrication Facility (NorFab III, project number: 295864).

References

[1] D. Liu and S. Park, "Three-Dimensional and 2.5 Dimensional Interconnection Technology: State of the Art " *Journal of Electronic Packaging,* vol. 136, no. 1, p. 014001, 2014.

[2] S. Gupta, W. T. Navaraj, L. Lorenzelli, and R. Dahiya, "Ultra-thin chips for high-performance flexible electronics," *npj Flexible Electronics* vol. 2, pp. 1-17, 2018.

[3] M. H. Malik, G. Grosso, H. Zangl, A. Binder, and A. Roshanghias, "Flip Chip integration of ultra-thinned dies in low-cost flexible printed electronics; the effects of die thickness, encapsulation and conductive adhesives," *Microelectronics Reliability,* vol. 123, pp. 1-7, 2021.

[4] J. J. M. Zaal, W. D. v. Driel, and G. Q. Zhang, "Challenges in the Assembly and Handling of Thin Film Capped MEMS Devices," *Sensors,* vol. 10, no. 4, pp. 3989-4001, 2010.

[5] W. Sun, W. H. Zhu, F. X. Che, C. K. Wang, A. Y. S. Sun, and H. B. Tan, "Ultra-thin Die Characterization for Stack-die Packaging," in *the 57th Electronic Components and Technology Conference (ECTC)*, Sparks, NV, USA, 2007, pp. 1390-1396.

[6] C. Kallmayer *et al.*, "Stretchable Electronics for Large Area Sensor Skin," in *IMAPS Nordic's Annual Microelectronics and Packaging Conference and Exhibition (NordPac)*, Oslo, Norway, 2023, pp. 1-6.

[7] K. Brenner, A. S. Ergun, K. Firouzi, M. F. Rasmussen, Q. Stedman, and B. P. Khuri–Yakub, "Advances in Capacitive Micromachined Ultrasonic Transducers," *Micromachines,* vol. 10, no. 2, pp. 1-27, 2019.

[8] A. S. Savoia *et al.*, "A 3D Packaging Technology for Acoustically Optimized Integration of 2D CMUT Arrays and Front End Circuits," in *IEEE International Ultrasonics Symposium (IUS)*, Washington, DC, USA, 2017.

[9] I. O. Wygant *et al.*, "An Integrated Circuit With Transmit Beamforming Flip-Chip Bonded to a 2-D CMUT Array for 3-D Ultrasound Imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control,* vol. 56, no. 10, pp. 2145-2156, 2009.

[10] Ö. Oralkan *et al.*, "Volumetric Ultrasound Imaging Using 2-D CMUT Arrays," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control,* vol. 50, no. 11, pp. 1581-1594, 2003.

[11] M. J. Yim, C.-K. Chung, and K. W. Paik, "Effect of Conductive Particle Properties on the Reliability of Anisotropic Conductive Film for Chip-on-Glass Applications," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 30, no. 4, pp. 306-312, 2007.

[12] M. J. Yim, J. Hwang, and K. W. Paik, "Anisotropic Conductive Films (ACFs) for Ultra-fine pitch Chip-On-Glass (COG) Applications," *International Journal of Adhesion and Adhesives,* vol. 27, no. 1, pp. 77-84, 2007.

[13] H.-V. Nguyen *et al.*, "Anisotropic Conductive Film Interconnects for Fine-pitch MEMS," in *the 4th Electronics System Integration Technology Conferences (ESTC)*, Amsterdam, Netherlands, 2012, pp. 1-6.

[14] A. Larsson, F. Oldervoll, T. A. T. Seip, H.-V. Nguyen, H. Kristiansen, and Ø. Sløgedal, "Anisotropic Conductive Film for Flip-Chip Interconnection of A High I/O Silicon Based Finger Print Sensor," in *the 22nd Micromechanics and Micro systems Europe Workshop*, Tønsberg, Norway, 2011, pp. 186-189.

[15] H.-V. Nguyen, T. Eggen, and K. E. Aasmundtveit, "Assembly of Transducer Array Using Anisotropic Conductive Film for Medical Imaging Applications," in *the 20th European Microelectronics and Packaging Conference (EMPC)*, Friedrichshafen, Germany, 2015, pp. 1-6.

[16] H.-V. Nguyen, T. Eggen, B. Sten-Nilsen, K. Imenes, and K. E. Aasmundtveit, "Assembly of Multiple Chips on Flexible Substrate Using Anisotropic Conductive Film for Medical Imaging Applications," in *the 64th Electronic Components and Technology Conference (ECTC)*, Orlando, Florida, USA, 2014: IEEE, pp. 498-503.

[17] J. v. d. Brand, R. Kusters, M. Cauwe, D. v. d. Ende, and M. Erinc, "Flipchip bonding of thin Si dies onto PET foils: Possibilities and applications," in *the 18th European Microelectronics & Packaging Conference (EMPC)*, Brighton, UK, 2011, pp. 1-6.

[18] J.-H. Kim, T.-I. Lee, T.-S. Kim, and K.-W. Paik, "Effects of ACFs Modulus and Adhesion Strength on the Bending Reliability of CIF (Chip-in-Flex) Packages at Humid Environment," in *the 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2018.

[19] Y.-W. Huang and S.-T. Lu, "Development and Reliability of Ultra-Thin Chip on Plastic Bonding for Flexible Liquid Crystal Displays," in *the 60th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2010, pp. 575-580.