

Interconnect Stress Testing as a tool for assessment of reliability of modern PCB's.

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Abstract (Word count: 327)

1. Background

The of miniaturization can be seen in electronics for some time already. The pinout of active components grows enabling them to have additional functions. The trend in usage of System in a Package (SiP) solutions is also evident thus routing of the active and passive elements became also challenging. To overcome this challenge boards with High Density Interconnection (HDI) where not only through hole, but also different kinds of microvias e.g. blind, buried, stacked, staggered via are used. The standard procedure to test reliability of boards and assemblies is very resource-hungry especially in time and money, as the tests have to be carried out in climatic chambers which lasts for weeks, followed by additional destructive testing like cross-sections. On the other hand IST (Interconnect Stress Testing) is a quick test, that enables to have assessment of the used technology especially the quality of the through holes of all types. Although the coupons are destroyed during the test, it is not necessary to test the manufactured circuits. This saves both materials and time. The technology optimizations and the key findings will be presented within the paper.

2. Method

The IST is a technique where a current is passed through specially designed PCB where "power" and "sensing" traces overlay. The passage of the current leads to heating of the board which is monitored through sensing side where resistance change is recorded. The described methodology is based on IPC test method where own device was built and software was written to enable testing. IST test coupons is a specialized tool that is assumed to act as "representatives" of printed circuit boards produced. Such coupons are placed in the production panels, the same on which the ultimately manufactured boards are located. This allows one to easily control the production process almost in real time. If any discrepancies are diagnosed on the test coupon, a given batch of products can be eliminated from further production or subjected to a more thorough than standard inspection to determine whether the product is still suitable for repair and restoration of its 100% functionality, or whether it must be definitively rejected. The proposed diagnostic technique includes implemented operational aspects already at the production stage, which allows for verification of the quality of printed circuit boards produced not only in terms of compliance with the design, but also in relation to the possible occurrence of hidden defects and material compatibility. Different sets of technological parameters were altered during the production of the PCBs. Exemplary PCB layout used for tests is presented in Figure 1.

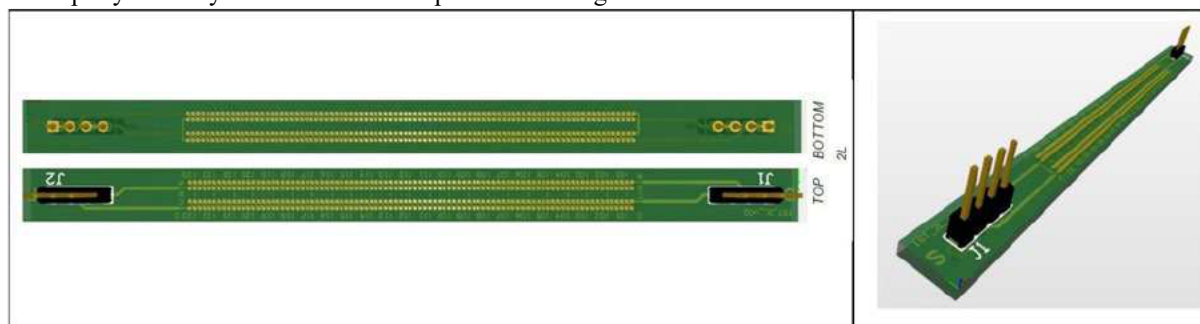


Figure 1. Top and bottom view of an exemplary test board (left), 3D model of the tested board (right).

IST works by taking the test sample through a quick thermal cycle between ambient temperature and 150°C followed by forced air cooling back to ambient temperature. As the coupon thermal cycles, changes in circuit

resistance are monitored. An increase of 10% is considered as a failure and testing is aborted. So IST stops testing (stress) at the exact moment of failure. Testing temperatures can be raised to 260°C (for polyimide boards). The test is dependent on the coupon design, which reflects the board's attributes, including critical hole size, copper weight, number of layers, connection types, etc. The coupon is designed with two discrete circuits - POWER and SENSE. The power circuit is used to heat the coupon and check the integrity of the post. The sensing circuit is measured to monitor resistance changes in the PTH or PTV (through shell). The sensor circuit is not receiving significant power. The power circuit heats the coupon to 150°C using DC current. At the same time the resistance of the sense circuit is monitored. Typically, the test is run until resistance in either circuit increases by greater than 10% or till a certain number of cycles.

These tests determine the physical resistance of representative samples of printed circuit boards to cyclic heating to high temperatures. Temperature changes are intended to create thermomechanical stresses on the sample. Generally, during the test, the sample is heated by a current flowing through it to bring the temperature of the copper to a certain value. Turning the electric current on and off at precisely defined intervals causes thermal cycles between the ambient temperature and the designated test temperature. The laminate and surrounding materials are heated to varying degrees depending on their thermal conductivity. Thermal cycling is designed to accelerate the detection of hidden anomalies. The number of cycles to failure allows for a quantitative assessment of the "technology quality" and predicts the durability of the electronic packages produced. It is expected that for consumer electronics devices, test packages should withstand at least 100 IST cycles. The IST test is also used to assess the quality of manufactured printed circuits intended for operation in space conditions. For some applications, there are requirements for strength of 1500 cycles and an allowable change in the electrical resistance of the sensory circuit not more than 5% of the output value.

The standard diagnostics of potential hidden defects, which mainly appear only during operation, requires the use of long-term, often months-long, fatigue tests. The proposed method of verifying the quality of printed circuit boards radically reduces this time to less than 2 days. Cyclically forced changes in the temperature of the test coupon, through thermal expansion of the construction materials used, cause cyclical changes in the geometric dimensions of the holes, and these in turn cause cyclical stretching and compression of the copper layer covering the walls of the holes. This phenomenon has the greatest impact along the axis of the holes, causing cyclic stretching and compression of the copper plated walls of the holes, due to CTE mismatch. The observed significant changes in the electrical resistance of interlayer connections may be caused by the low quality of metallization of the walls of the holes. This is particularly noticeable in the case of coupons with relatively small diameter holes, i.e. a large aspect ratio. This may indicate serious problems related to the penetration and exchange of metallising chemical baths inside holes with a large aspect ratio.

3. Results

Based on the literature data and the results of research work, the following design assumptions for the test boards were formulated:

1. Two separate POWER and SENSE circuits.
2. Comparable electrical resistance of circuits in the range - $0.3 \div 1.2 \Omega$.
3. Pins: two times four pins arranged in a row with a spacing of 2.54 mm for soldering GOLDPIN type connectors. The pins for the POWER and SENSE circuits can be located on opposite or one side of the test coupon.
4. Test coupon should contain current and signal traces with holes, in accordance with the production design:
 - Through Holes,
 - Blind Vias,
 - Buried Vias.
5. The size of the holes - adequate to the diameter of the holes on the production boards.
6. Number of layers / thickness of the laminate - adequate to the construction of production boards.
7. Test coupon dimensions: The tester can test coupons up to 121 x 26 mm. In addition, it is important that the GOLDPIN type connectors are not mounted close to the edge of the test coupon.

In the test system, it is necessary to provide a small clearance (min. 1-2 mm) for linear elongations of the laminate related to its thermal expansion. During the test, cyclic changes in the temperature of the test coupon are caused in the range from room temperature, approx. 25 °C, to 150 °C, which cause its elongation.

8. Coupons should be designed in a program that allows saving in the IPC-2581 Rev. format. B Best or

ODB++ v8, e.g. Altium Designer.

During the work, software for automatic IST measurements was developed. Proprietary software allows for accurate measurements of each production batch, each panel separately. Instructions for carrying out tests on a test stand have also been prepared, thanks to which measurements can be performed easily by a trained employee. This allows for quick verification of the quality and reliability of the PCBs made.

One of the basic needs of diagnostics conducted with this method is to multiply the number of tests performed at one time. As part of the research work, an eight-channel stand for testing IST coupons was developed, Fig. 2-3.

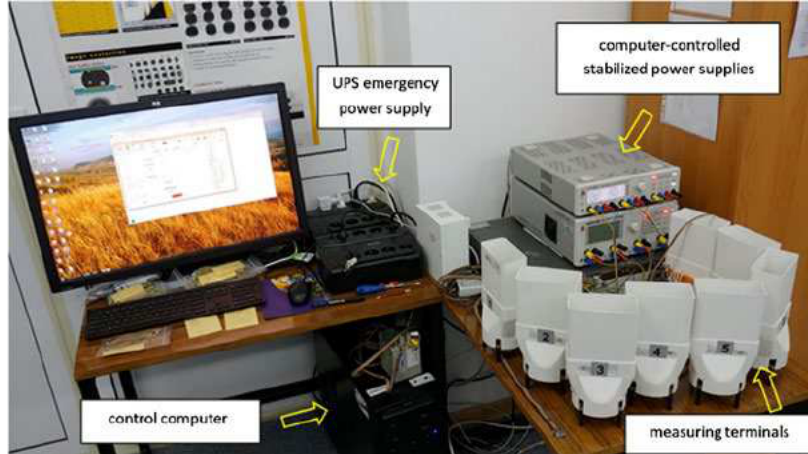


Fig.2. IST test stand.

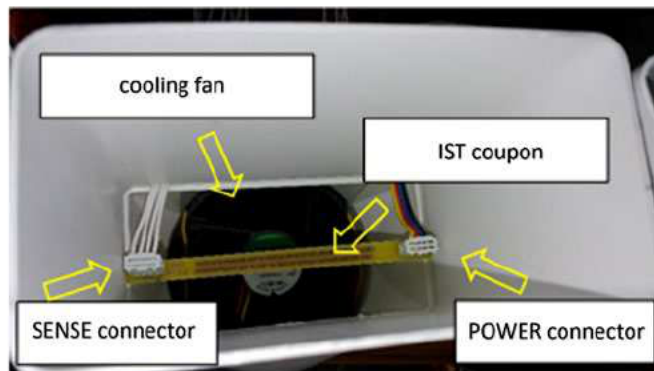


Fig. 3. IST test coupon placed inside the measuring terminal (top view).

The system can displays graphs of resistance activity in real time, showing individual thermal cycles and cumulative cycle data. Data analysis is simplified with automated graphical tools in each cycle and coupons. The data collection takes place in the set time period. The data collected during the test includes the number of cycles to failure or termination, the resistance of each circuit, the resistance at both high and low temperatures. Data evaluation can indicate failure mode and circuit integrity. The results are compared with baseline results for similar products. This gives you a quantification of how performance compares to industry, customer or internal requirements.

The diagrams in Fig. 5 and 6 show exemplary waveforms of changes in the resistance of the POWER circuit of the test coupons (designations 13 and 14) as a function of the number of exposure cycles. As can be seen from the graph in Fig. 35, the permissible resistance change ($\pm 10\%$ of the output resistance) was exceeded after a little more than 380 cycles. On the other hand, the graph in Fig. 36 shows the complete failure of the circuit after a few more than 270 cycles. Until the circuit was damaged, changes in resistance did not exceed $5\div 6\%$.

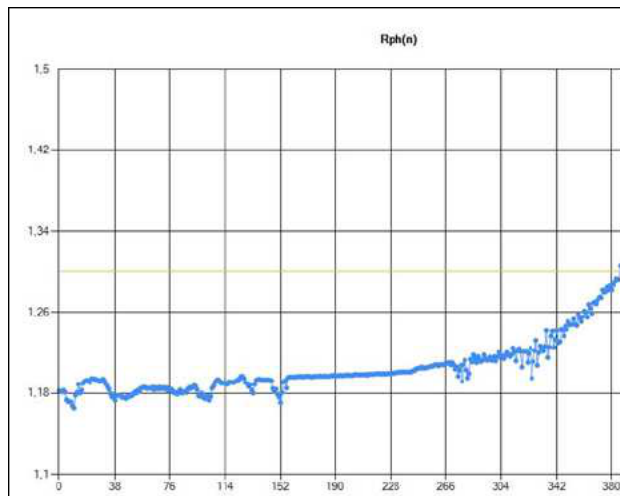


Fig. 5. Changes in the resistance of the POWER circuit of the test coupon no. 13.

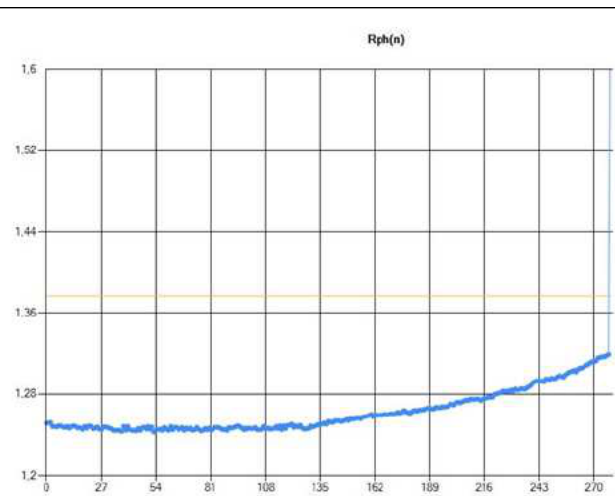


Fig. 6. Changes in the resistance of the POWER circuit of the test coupon no. 14



Fig. 7. Metallization damage in the through hole of coupon no. 13.

The failure of the metallization occurred as a result of a rapid increase in temperature.

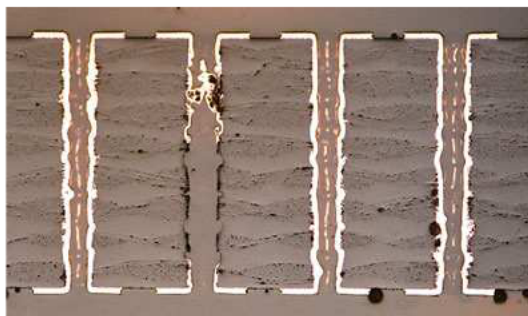


Fig. 8. Metallization crack in the through hole of coupon no. 14.

The failure of the metallization occurred as a result of barrel cracking. This is a typical defect observed for through holes, due to the higher thermal expansion of the system in the Z axis than in the XY axis.

4. Conclusion

The main reason why PCB manufacturers use IST is to save costs and time. IST costs less than full accelerated standard thermal tests while being more comprehensive. IST tests hundreds of holes and connections simultaneously, so statistically IST tests are more representative of PCB quality. The IST test ends before or after the PCB is fully damaged according to requirements. The combination of IST and thermography greatly improves the ability to find and assess failure causes. The use of thermal imaging to locate the damaged area allows for precise metallographic examination and quick determination of the cause of the failure. Other test

methods have significant limitations. Analysis based solely on metallographic microsections is laborious and requires qualified employee preparation and subjective assessment. Standard thermal tests are more expensive and time consuming and do not distinguish whether a failure occurs for PTH or interlayer connections. IST is cost effective test method that enables swift analysis of the PCB reliability. This method is successfully introduced to the scope of research in the Laboratory. It allowed to quickly assess the quality of the production panels and optimize the production process. The outcomes helped to identify failure in early fabrication stages and lead to further optimization of the PCB manufacturing process.

5. References

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