Characterizations for eWLB (Embedded Wafer Level Ball Grid Array) Antenna in Molded Package Integrations in 77GHz Automotive Applications

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***Abstract*— The worldwide IC market has had a significant growth rate in recent years, driving diversified package solutions in the segments of communication, computing, consumer, automotive, industrial, etc. Among these market segments, the automotive market is forecast to have the strongest CAGR (Compound Annual Growth Rate) of any of the end-use segments in the next 5 years, which results in more IC packages and components being designed into automotive vehicle systems such as infotainment, ADAS (Advance Driving Assistance System), instrumentation, body systems, battery control systems and so on. In these applications, the 77GHz short-range radar sensor application that can enable higher EIRP (Effective Isotropic Radiated Power) and adaptive cruise control performance has become more attractive to be commercialized. Due to the benefits of shorter interconnection length, lower conductive loss with smooth Cu surface as well as a lower dielectric constant and dielectric loss of materials in a fan-out wafer level package (FOWLP) technology, the FOWLP is proven as a suitable packaging solution to achieve the high speed and frequency requirements in 5G and mmWave applications. The eWLB Embedded Wafer Level Ball Grid Array) is a versatile FOWLP technology, providing a robust package platform in a space-efficient design with the very dense interconnection and routing of multiple dies as well as a smaller footprint and lower package profile providing a reliable package solution. Meanwhile, since the utilization of an antenna that is integrated into the packages has been studied as a low-cost solution because the packages can be tested in normal FR4 printed circuit board (PCB) instead of the RF function integrated PCB, the eWLB integrated with molded antenna chip packages (called eWLB antenna in molded package) technology is introduced in this paper. The characterizations for assembly process challenges are evaluated and illustrate the process optimizations of equipment handling, antenna molded chip package fabrication, reconstitution process control and warpage characterization of the molded wafer. In addition, the radio frequency (RF) test validation is performed to verify the performance of scattering parameter (S-parameter), radiation pattern, impedance and detection range of the antenna. In order to prove the reliable quality and yield of the evaluated eWLB antenna in molded packages, package-level reliability tests are studied. Through these results, it will show that this eWLB antenna in molded package integration is a robust and cost-effective solution for 77GHz automotive applications.**

Keywords—Fan-out wafer level package, FOWLP, eWLB, antenna in package, AiP, 77GHz, automotive.

I. Introduction

The semiconductor industry is growing faster than ever, driving the need for various advanced packaging solutions to achieve higher performance requirements in multiple market segments, such as communication, computing, consumer and automotive applications. Among these semiconductor markets, the automotive applications have been predicted to have tremendous growth with a 2022-2027 CAGR of around 7.4% according to an industry report [1]. In order to achieve the requirements of high speed, high frequency, fine routing pitch and efficiency enhancement, the FOWLP technology has been studied as the proper packaging solution not only in 5G and mmWave communication applications but also in 77GHz (and above) automotive radar applications [2-3]. The eWLB (Embedded Wafer Level Ball Grid Array) technology is one of the commercialized FOWLP technologies that utilizes the simplest process flow with chip first and face down architecture as well as lower dielectric constant and dielectric loss re-passivation materials. In addition, the smooth electroplated Cu surface with lower conductive loss and shorter interconnection length is also adopted to reduce the parasitic effect and insertion loss at mmWave high frequency in the eWLB technology [4-6].

For the purpose of satisfying the demand for a higher performance and cost-effective packaging solution for 77GHz automotive radar applications, the FOWLP technology with integrated antenna has been widely discussed. Because the use of antenna integrated with a FOWLP will result in many complicated processes and higher assembly cost, the related function tests can be performed with the normal FR4 PCB instead of the RF function integrated PCB. The PCB cost will be reduced more than several dozens of times. In this paper, the technology of eWLB integrated antenna in a molded package and the corresponding assembly characterizations as well as electrical test verifications are studied. The antenna in molded chips are designed with the backside metal antenna patterning process not having any connection to the eWLB redistribution layer (RDL) and are fabricated internally. The CMOS die is integrated with several antenna molded chips in the eWLB to form a single channel (one transmitter and one receiver, 1TX1R) and dual channel (two transmitters and two receivers, 2TX2R) packages. In order to validate the robust design and the reliable packages of this evaluated eWLB integrated antenna in the molded package, the characterizations for optimizations of equipment handling, fabrications of antenna molded chip packages, the process flows of reconstitution and warpage control as well as the package reliability tests are presented. In addition, the electrical test validation includes the evaluation of S-parameter, radiation pattern, and impedance and detection range of the antenna verification. These results are proven to meet 77GHz automotive requirements. With these results, it is believed that this present eWLB antenna in molded package integration will be a proper package solution to meet high frequency, and high reliability requirements in 77GHz automotive application and an overall cost-effective solution to minimize the assembly and test board cost.

II. Process Flows for eWLB Antenna in A Molded Package

With the benefit of eWLB technology that can integrate multi-chips, enable high speed and high-frequency requirements as well as achieve reliable performance in 5G and mmWave applications, the innovation of this study is to design antenna molded chips that can integrate into a eWLB package with the current compatible integration process flow.

A. Antenna molded chip fabrication

The antenna molded chip is designed with the backside metal antenna patterning process on the molded wafer and will be viewed as the other die that integrates with the CMOS die using a pick and place process that places them onto a carrier simultaneously. This will be followed with the compression molding process in the standard eWLB reconstitution process. These antenna molded chips are fabricated internally and there is no signal routing connection between antenna molded chips and the eWLB redistribution layer (RDL). The uses of the antenna molded chips are not only compatible to the existing eWLB process flows, but also reduce the antenna fabrication cost. The optical and cross-sectional image of an antenna molded chip is illustrate in Fig. 1.

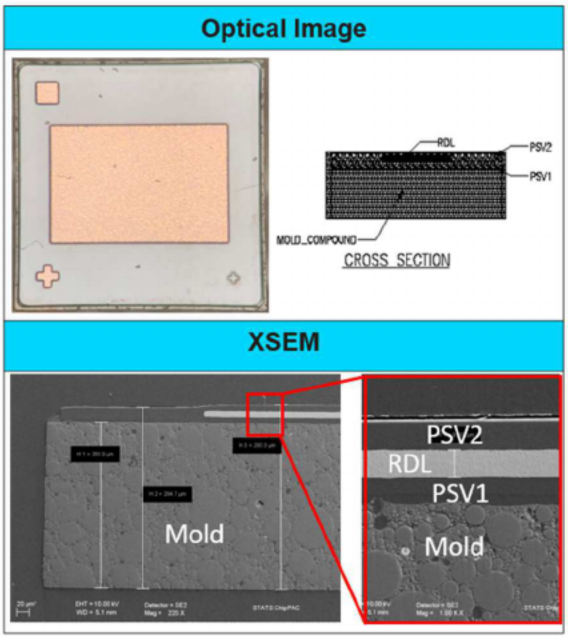


Fig. 1. The optical and cross-sectional image of an antenna molded chip.

B. Process Flow for eWLB Antenna in a Molded Package

Two devices with the utilizations of eWLB antenna in molded package integrations are studied. One is AiMP-1TX1R, the single channel (one transmitter and one receiver) design with a pair of antenna molded chips and the other is AiMP-2TX2R, the dual channel (two transmitters and two receivers) design with two pairs of antenna molded chips. The evaluated devices' specifications and final package images are illustrated in Fig. 2 and 3, respectively. The assembly processes of these evaluated eWLB antenna in molded package integrations are illustrated in Fig. 4 and described below.

Items	Specifications
Package size	10x8.5mm
Die size	~4x4mm
Die thickness	250um
Antenna molded chips size	1.75x1.75mm
Antenna molded chips #	2
Ball pitch	0.5mm
Ball diameter	0.3mm
Package thickness	<0.6mm

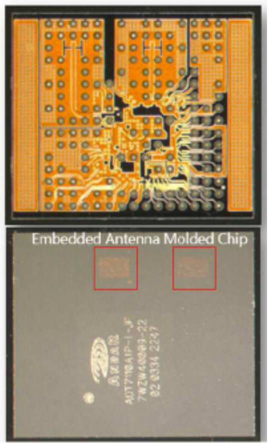


Fig. 2. AiMP-1TX1R specifications and package image.

Items	Specifications
Package size	10x8.5mm
Die size	~4x4mm
Die thickness	250um
Antenna molded chips size	1.75x1.75mm
Antenna molded chips #	4
Ball pitch	0.5mm
Ball diameter	0.3mm
Package thickness	<0.6mm

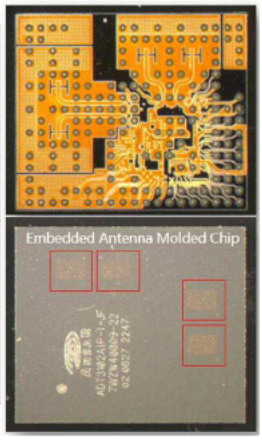


Fig. 3. AiMP-2TX2R specifications and package image.

(1) Pre-assembly processes: includes incoming wafer thinning with backside grinding as well as wafer singulation by laser grooving and mechanical sawing;

(2) Reconstitution process: starts from the processes of laminating an adhesive foil onto a carrier then placing active die face down and antenna molded chips with top side patch antenna with the pick and place tool. After the process of die pick and place, the compression molding process is implemented and then followed by a de-bonding process to remove the carrier and foil, resulting in a reconstituted wafer with the molding compound surrounding all antenna molded chips and active dies surfaces.

(3) WLP process on a reconstitution wafer: includes dielectric layer (PSV1 & PSV2) coating, exposure, development, curing and dielectric layer opening etching; seed layer sputtering, RDL and UBM (under ball metallization) plating and etching; solder ball mounting and package singulation.

(4) Backend process: includes final test, laser marking, EVI/AOI inspection, packing, etc.

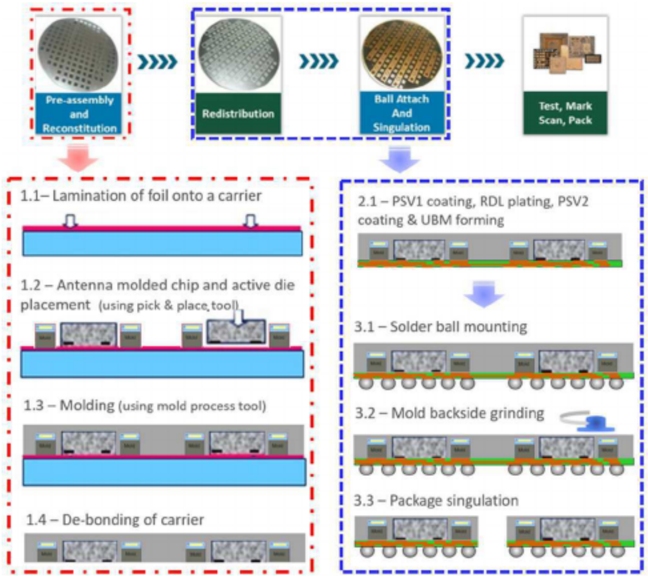


Fig. 4. Process flow of eWLB antenna in molded package integration.

III. PACKAGE ASSEMBLY CHARACTERIZATION FOR EWLB ANTENNA IN MOLDED PACKAGE

As the pre-assembly process of the incoming wafer is needed before the eWLB reconstitution process, the characterization data of the monitored items in pre-assembly (includes wafer grinding and dicing) is listed in Table I. Table II and III shows the process monitored items in the reconstitution processes with the integrations of antenna molded chips and an active die, which include PSV1 and PSV2 lithography, RDL and UBM plating as well as the related warpage control data, respectively. The warpage specification requirements is controlled within -1.5mm to 2.0mm in each process in eWLB reconstitution processes. Through these results, it is not only observed that the maximum warpage after annealing, PSV1, RDL, PSV2 and UBM plating processes are all less than 2 mm and meet the in-line specification of well warpage control but also indicates both pre-assembly and reconstitution molded wafer processes are consistently under control.

In addition, the ball shear test is also performed to verify the strength of solder ball after the solder ball mount (ball drop) process. The ball shear results for both eWLB antenna in molded package integrations, AiMP-1TX1R and AiMP-2TX2R are illustrated in Table IV, which shows that all the examined solder balls exceeded the spec. of 260gf with good strength. After the solder ball mounting process, the mold backside grinding process is utilized to achieve the targeted mold thickness with the specification requirement of 0.355 ±0.025mm after backside grinding. With this target mold thickness, it can be ensured that the overall maximum package thickness (includes solder ball stand-off height) will be less than 0.6mm. After the package singulation process, the final eWLB packages can be obtained. These characterization data are illustrated in Table V and VI, respectively, which showed all are passed specification requirements and the cross-sectional images of the final AiMP-2TX2R package is showed in Fig.5.

TABLE I. PROCESS CONTROL ITEMS IN PRE-ASSEMBLY PROCESS

Process	Monitoring Items	Criteria	Average	Stdev
Si Backgrind	Wafer Thickness	250 ± 10um	249.26	0.664
Si Dicing	Kerf Width	20 ± 12um	21.5 (X) 21.5 (Y)	0.689 (X) 0.599 (Y)
	Kerf Shift	± 5um	0.1 (X) -0.1 (Y)	0.551 (X) 0.721 (Y)

TABLE II. PROCESS CONTROL ITEMS IN RECONSTITUTION PROCESS

Process	Monitoring Items	Criteria	Average	Stdev
PSV1	Thickness	12.3 ± 2um	11.82	0.561
	Opening (CD)	22.5um ± 3um	23.84	0.562
RDL1	Thickness	8 ± 1.6um	8.17	0.111
	Opening (CD)	20um± 3um	21.07	0.531
PSV2	Thickness	13.0 ± 2um	12.90	0.670
	Opening (CD)	250um ± 6um	249.51	0.849
UBM	Thickness	12.0 ± 2.6um	11.60	0.182
	Opening (CD)	290um ± 6um	288.65	0.706

TABLE III. MAX. WARPAGE DATA FOR RECONSTITUTION MOLDED WAFER

Process	Criteria	Max. Warpage (mm)
Molding	-1.5mm ~ 2um	1.88
PSV1		-0.37
RDL1		0.53
PSV2		0.94
UBM		1.16

TABLE IV. BALL SHEAR TEST AFTER BALL DROP PROCESS

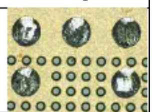
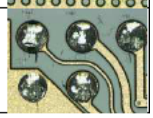
Device	Criteria	Min. (gf)	Max. (gf)	Result	Image
AiMP-1TX1R	Min. 260gf	592.7	660.9	Pass	
AiMP-2TX2R	Min. 260gf	600.2	633.7	Pass	

TABLE V. MOLD BACKSIDE GRINDING RESULT

Device	Item	Mold thickness (um)
AiMP-1TX1R	Before Backside Grinding	~610
	After Backside Grinding	355.1
AiMP-2TX2R	Before Backside Grinding	~610
	After Backside Grinding	357.8

TABLE VI. PACKAGE SINGULATION RESULT

Device	Monitoring Items	Criteria	Average	Stdev
AiMP-1TX1R	X-Dim.	10.0 ± 0.05mm	9.999	0.003
	Y-Dim.	8.5 ± 0.05mm	8.502	0.002
AiMP-2TX2R	X-Dim.	10.0 ± 0.05mm	9.997	0.003
	Y-Dim.	8.5 ± 0.05mm	8.500	0.002

IV. ELECTRICAL PERFORMANCE CHARCTERIZATIONS

To fully characterize the designed AiMP-1TX1R and AiMP-2TX2R samples, some test structures are also fabricated. For testing purposes, the S-parameter performance of the designed testing structure is characterized first. The measurement process was conducted using on-wafer G-S-G probing up to 100 GHz by means of a vector network analyzer

N5290A from Keysight and a 200-µm pitch Air Coplanar Probe (ACP) probe with 1-mm connectors from FormFactor. The on-wafer calibration was made by using a conventional short-load-open-thru (SLOT) approach to move the reference planes from the connectors of the equipment to the tips of the RF probes.

The die microphotograph, testing setup, and comparison results between the simulation and measured data are given in Fig. 6. As it can be seen from Fig. 6(c), a good agreement between simulated and measured results is obtained. More than 15-dB return loss is achieved across a bandwidth of 76-84 GHz. It indicates a good impedance matching for the designed antenna as well. The impact due to back-side metal, and BGA balls on impedance variations of the designed testing structure is marginal.

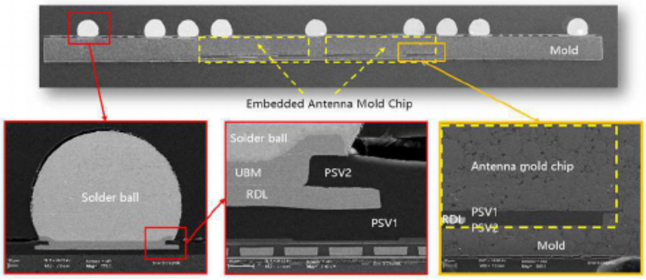
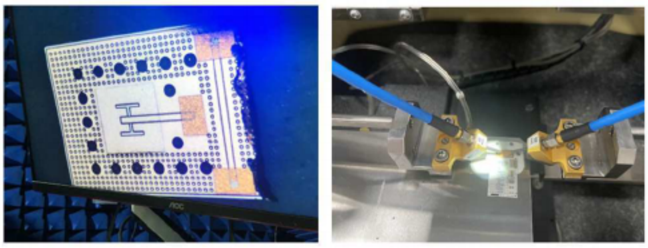
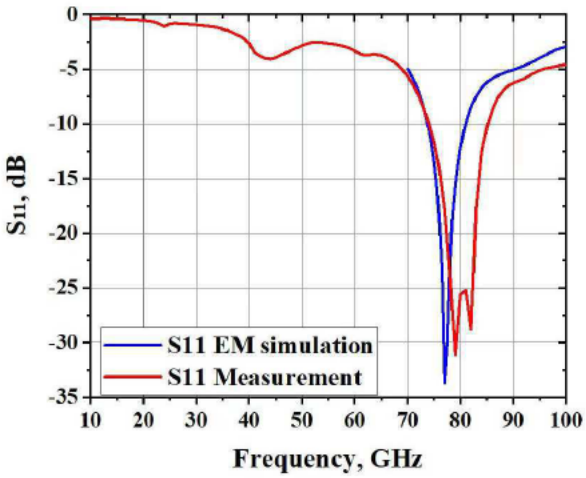


Fig. 5. Cross-sectional images for AiMP-2TX2R.



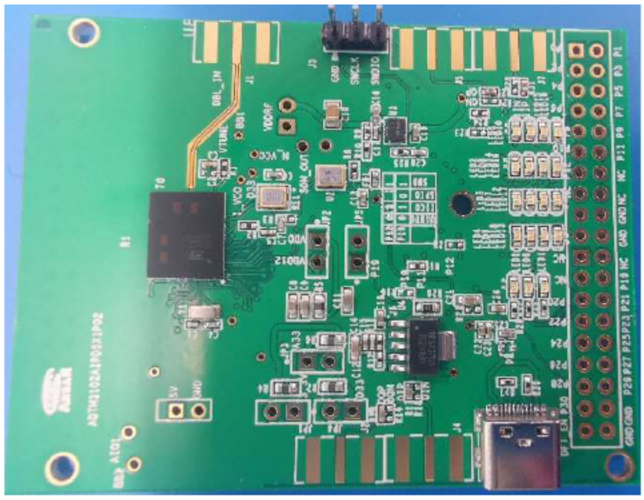
(a) (b)



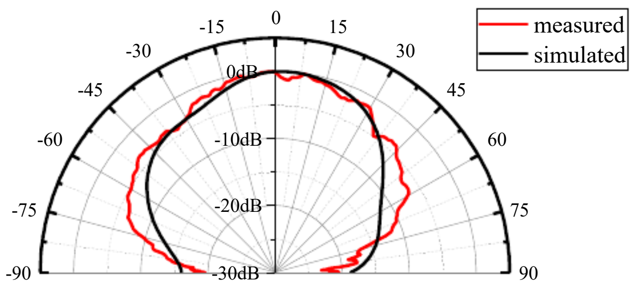
(c)

Fig. 6. Measurement results and set up for testing structures using on-wafer probing, (a) die microphotograph, (b) set up on probe station, (c) comparison results between simulation and testing.

To further verify the performance of the designed AiMP, the prototype is also tested at the PCB level, which is shown in Fig. 7(a). In Fig. 7(b), the comparison results between simulation and measurement results are illustrated. A good agreement between them is also obtained. It once again indicates that the designed AiMP is fully functional as expected.



(a)



(b)

Fig. 7. Measurement results and setup for testing the packaged antenna. (a) circuit board with the packaged chipset; (b) radiation pattern at 79 GHz.

V. RELIABILITY TEST DATA

For the purpose of demonstrating the examined reliable eWLB antenna in molded package integrations, long term reliability tests such as pre-condition of moisture sensitivity level (MSL3) with 30°C/60%RH and 192 hours condition, unbiased highly accelerated stress test (uHAST, test condition at 130°C/85%RH), pressure cooker test (PCT, test condition at 121°C/100%RH) and thermal cycling test condition B and C (TCB, -55°C to 125°C and TCC, -65°C to 150°C) with pre-condition of MSL3 as well as high temperature storage test (HTST, test condition at 150°C) were performed. The long-term package reliability results of all examined legs passed uHAST 168 hours, PCT 168 hours, TCB and TCC 1000 cycles as well as HTST 1000 hours through the T-SAM inspection. The test condition, result and sample size are listed in Table VII. Fig. 8 illustrates the T-SAM result for final reliability reading points of AiMP-1TX1R and it clearly shows that there is no abnormality and delamination observed through these images. Bases on these reliability test results, it shows not only the examined eWLB antenna in molded package integrations can achieve the robust antenna design and compatible fan-out wafer level package assembly process flows but can also meet package level reliability criterion. Therefore, it is believed that with the technology of eWLB antenna in mold package integrations established in this paper will provide a suitable packaging solution for when highly integrated, high speed, high frequency and cost-effective purposes are required in the semiconductor industry.

TABLE VII. LONG-TERM RELIABILITY TEST RESULT

READOUT POINTS	TEST CONDITIONS	SAMPLE SIZE	PRECON DITION (Y / N)	AIMP-1TX1R	AIMP-2TX2R
MSL3	30degC / 60% RH / 192hrs	44 units	Y	0/44	0/44
uHAST 168 hrs	130degC / 85% RH	11 units	Y	0/11	0/11
PCT 168 hrs	121degC / 100% RH	11 units	Y	0/11	0/11
TC(B) 1000x	-55degC / 125degC	11 units	Y	0/11	0/11
TC(C) 1000x	-65degC / 150degC	11 units	Y	0/11	0/11
HTS 1000 hrs	150degC	22 units	N	0/22	0/22

Remarks: No delamination found on all readout points for both AiMP-2TX2R & AiMP-1TX1R packages.

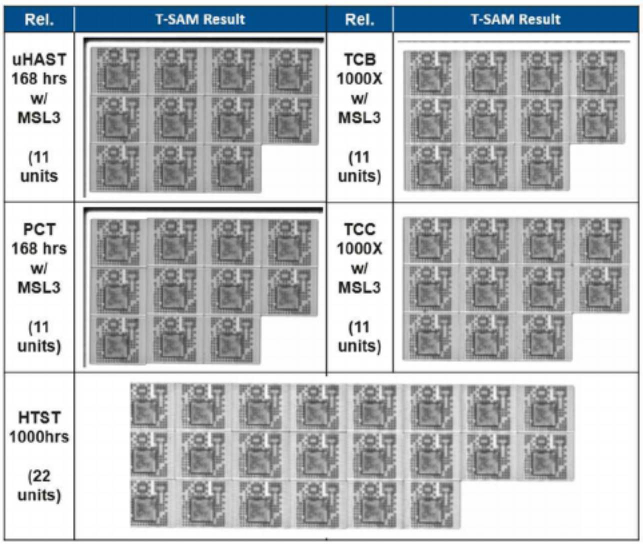


Fig. 8. T-SAM result for AiMP-1TX1R.

VI. CONCLUSIONS

The technology of eWLB antenna in molded package integrations was introduced to deliver a robust and highly integrated performance packaging solution with high speed, high frequency, reliable as well as cost-efficient requirements in 77GHz automotive applications;

(1) The eWLB antenna in molded package (eWLB AiMP) adopts the pre-fabricated antenna in molded chips to integrate with the eWLB package. As the antenna in molded chips are fabricated internally, the compatible integration process flow has been observed.

(2) Two eWLB antenna in molded package integrations are studied for process, mechanical, electrical and reliability characterizations. The examined eWLB AiMP integrations passed the process specification requirements, S-parameter, impedance, radiation pattern performance verification as well as long term reliability tests. The results show the good assembly quality and electrical performance of this robust and cost-efficient eWLB AiMP integration solution.

Bases on the investigated results above, it is believed that this eWLB AiMP integration technology can be an overall low-cost solution to minimize both assembly and test board cost as well as a proper package solution to meet high frequency and reliability requirements.

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