Investigation of Aluminum and Gold Flip-Chip Bonding for Quantum Device Integration

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***Abstract*— The majority of qubit chip integration is realized in a two-dimensional (2D) architecture. Whereas 3D architecture enables more advantages like efficient interconnect routing, allowing for more compact qubit coupling geometries, reducing form factor, and increased connectivity beyond nearest-neighbor interactions. Flip-chip (FC) assembly has been demonstrated to enable 3D architecture connecting qubit chip, interposer, and readout in a sandwich-like structure. Moreover, 3D integration allows the fabrication of hosting chip circuitry without degrading the qubit performance [1–4]. Different material considerations have to be taken into account since qubit operational frequency is in the gigahertz range and operating temperature is in the mK range to avoid thermal excitation. Materials that possess superconducting characteristics like Indium (In), Titanium Nitride (TiN), Tantalum Nitride (TaN), and Niobium (Nb) have been discussed as potential interconnect between building blocks [3, 5]. The In bumping on Aluminum (Al) redistribution layers require under-bump metallization (UBM) layers thus introducing multiple fabrication steps before the bonding process. An alternative approach would be to use the existing Al surface to electrochemically grow Al bumps and bond the chip using thermosonic bonding (TSB) at below 150°C to form a homogeneous metal-metal interface [6, 7].**

Keywords—Aluminum electrodeposition, Aluminum flip-chip bonding, Thermosonic bonding, Gold flip-chip bonding, Chip ultrasonic bonding, Thermal stress, Qubit chip integration, Finite Element analysis

I. Introduction

In ion trap-based quantum computers, the electrical, magnetic, thermal, and thermo-mechanical performance of the heterogeneously integrated package at cryogenic temperatures is crucial for the number of usable qubits per integrated area and thus ultimately determines the achievable computing power [4, 8–13]. Qubit chip integration using Flip-Chip bonding has been demonstrated to enable dense chip integration in 3D architecture [5, 14–19]. Wherein, traditional materials like copper (Cu), which is a standard metallization layer, are not superconducting due to quasiparticle excitation from heat formation thus reducing qubit performance. Also, silicon dioxide (SiO_2) and silicon nitride (SiN) dielectrics are reported to decrease the qubit lifetimes due to the qubit electric field interaction with defects [20]. Materials like Aluminum (Al), titanium nitride (TiN), and niobium (Nb), where substrate materials are silicon (Si) and sapphire (Al_2O_3), are discussed and used in the scientific community for qubit chip fabrication and integration [1, 3].

Different qubit chip integration methods can be used like wire bonding, soldering using In bumps as bumping material, or TSB using Al pillars to create a homogeneous metal-metal interconnect [1–3, 6, 7, 15, 21]. FC bumping using In and TCB have already been successfully demonstrated, however, In bumping requires UBM layers like Titanium (Ti), Platinum (Pt), Gold (Au), and Niobium nitride (NbN) to prevent the formation of Al-In intermetallic state, thereby introducing more fabrication steps and complex equipment to achieve the final layer before In electroplating process [1]. Also, considering CMOS processes the final metallization layer usually is Al, which can be utilized as a base for Al electrodeposition (ECD) [6, 7, 22, 23]. Finally, the Al-ECD-grown pillars could be bonded using the TSB method to bond the chip at below 150°C. Moreover, homogeneous metal-metal interconnects would benefit the overall system owing to reduced fabrication costs and good electrical contact between building blocks. The Au pillar chip bonding was used to compare the bond strength and cryogenic stress with Al pillar bonding.

II. Experimental

Aluminum and gold pillars were electrodeposited on 6-inch wafers with a thickness of 675 µm ± 25 µm. The substrate wafer had a similar wafer thickness with final Al and Au metallization layers.

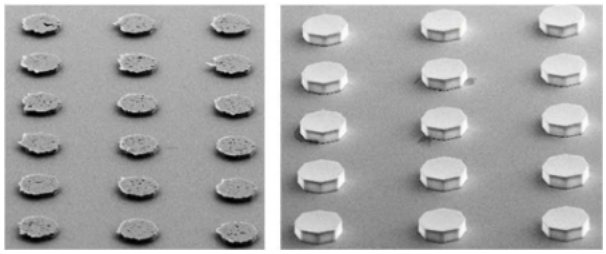

Figure 1. Aluminum (left) and Gold (right) chips with pillars

For the shear strength test, chips with electroplated Al and Au pillars were used to compare the bonding strength between the two materials. The average pillar thicknesses of Al and Au were 15.6 µm ± 0.5 µm and 15.2 ± 0.1 µm respectively (Figure 1). Each chip had 42 pillars with a pillar diameter of 100 µm and pillar distances of 120 µm in horizontal and 160 µm in vertical directions. Chips and substrates had sizes of 1.5mm x 1.5mm and 5mm x 5mm, respectively (Figure 2). The final bonding layer on the substrate was 1000 nm for Al and 250 nm for Au. The overall active bonding area of the pillars was 0.33 mm^2. The TSB of both chip materials was done using FINEPLACER® femto 2 from the company Finetech GmbH. The bonding machine is equipped with an ultrasonic module with a frequency of 42 kHz. An ultrasonic bonding tool with

a flat surface was used for the experiments. The bonding parameters were previously experimentally tested.

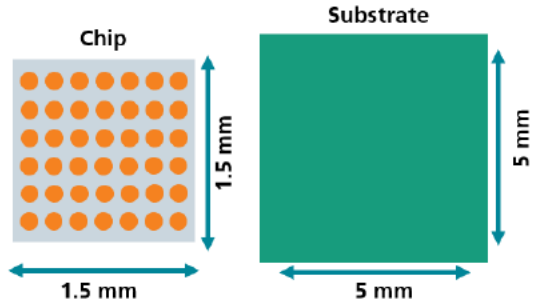

Figure 2. Flip-chip samples with chip dimensions of 1.5mm² and 42 pillars. The substrate with dimensions of 5mm² and PVD surface

A thermal stress test was conducted to measure bonded Al chip shear strength, with shear tester Condor Sigma from company XYZTEC, after immersing it in liquid nitrogen (-196°C) for the 60s and thawing it at +25°C for 30s (Figure 3). The first set of bonded Al and Au chips were sheared at room temperature (A) for comparison purposes and the second set of Al bonded chips was exposed to thermal cycling of 5x and 10x cycles (B) before the shear test.

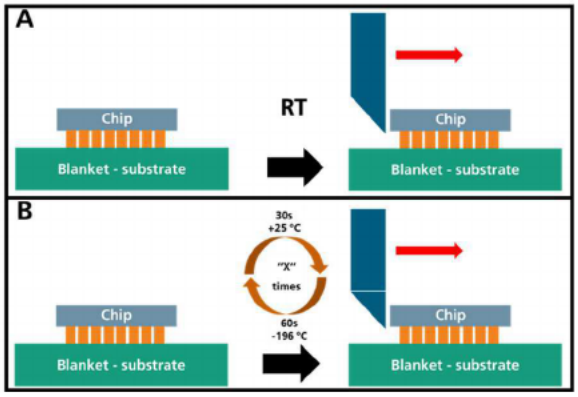

Figure 3. Bonded gold and Aluminum chip shear tests at A) Room temperature (25°C) and B) After thermal cycling

III. Results & Discussion

Results and discussion are separated into two parts – The Finite Element model (FE) and TSB using Al and Au samples.

A. Finite Element Analysis of the joint materials

The objective was to build FE models to study the thermo-mechanical performance of metallic joints on 3-layer setups (substrate, joint, chip) and to present an approach scalable to the package level. These models will further serve as a basis for future investigation of the electrical, magnetic, and thermal behavior of packages at cryogenic temperatures. The analysis was carried out using the simulation software Ansys.

The thermomechanical investigation considers a single joint since the chip and substrate are made of silicon and therefore exhibit no thermal mismatch. The metallization and joint are made of Al. The static analysis includes thermal shock cycling from 293 K down to 77 K and back to 293 K. Any visco-plastic behavior of the Al is neglected. The plastic deformation in the Al during cycling leads to fatigue crack growth. The accumulated equivalent plastic strain is quantitatively closely correlated with damage in ductile metals like Al and serves as a physical failure parameter. Hence, this quantity was determined together with the *VON MISES* stress.

The FE model consists of a single joint with dimensions similar to the FC samples used in the shear tests. Figure 4 shows the quarter model of a joint with its mesh. The volumes are divided into chip, substrate, and joint together with seed layer (metallization) on chip and substrate. The boundary conditions include the fixation of the symmetry planes as well as the fixation of a point in the center in all 3 directions. The loading is applied at a uniform temperature of 293 or 77 K respectively.

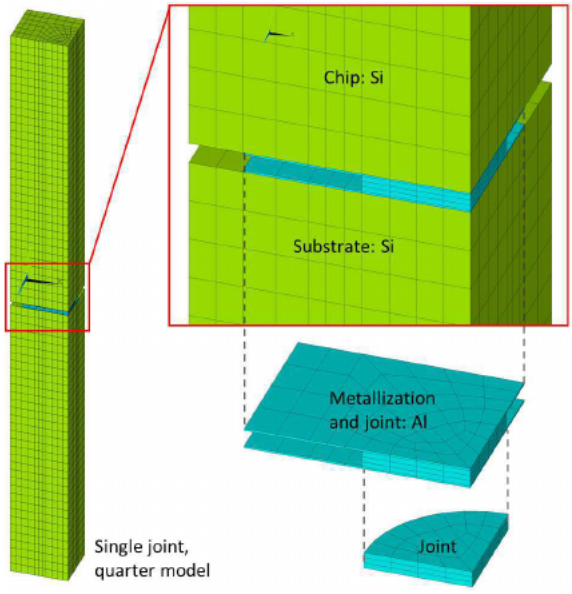

Figure 4. Quarter model of a single joint with its materials.

Temperature-dependent material data of Si and Al between 293 and 77 K is required for the modeling. The isotropic Young's modulus as well as coefficients of thermal expansions (CTE) are presented in Figure 5. The anisotropy of the mono-crystalline Si was neglected and isotropic Young's modulus and Poisson's ratio were used, computed from elastic constants considering the isostrain assumption (*VOIGT* average modulus) [24, 25].

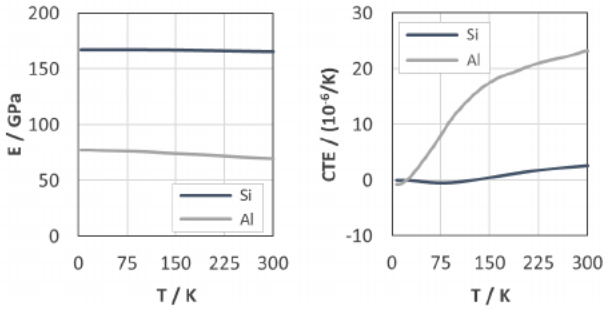

Figure 5. Anisotropic Young's modulus E (left) and coefficient of thermal expansion (right) of silicon and aluminum [24–27]

However, the actual plastic deformation of metals depends strongly on their microstructure. Therefore, that data must be obtained at a certain temperature from samples that feature the same microstructure as in the actual package. Since such equipment is not available at the author's facilities, the plastic behavior was estimated based on temperature-dependent offset yield strength (0.2% strain) and ultimate stress presented for a low alloy Al-1100 [27]. The ultimate strain

was then chosen. Assuming a material behavior according to Ramberg-Osgood, temperature-dependent stress-strain curves could thus be determined. Their multilinear approximation is given in Figure 6. The Poisson's ratio was chosen temperature independent with 0.33.

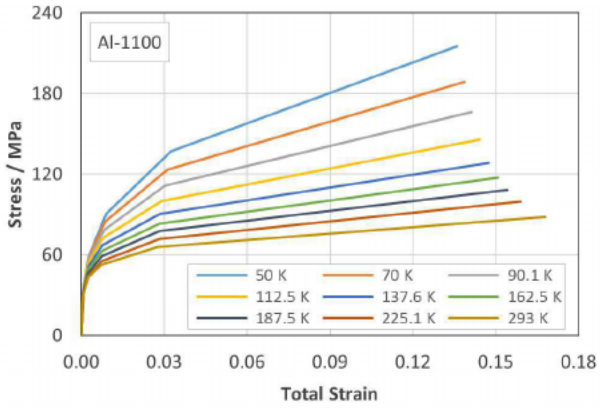

Figure 6. Estimated temperature-dependent multilinear stress-strain curves of alloy Al-1100. The model is based on yield stress and ultimate stress found in [27] assuming a material behavior according to Ramberg-Osgood.

Figure 7 shows the *VON MISES* stress after cooling down from 293 K to 77 K. The aluminum joint experiences a load of approximately 60 MPa to 80 MPa.

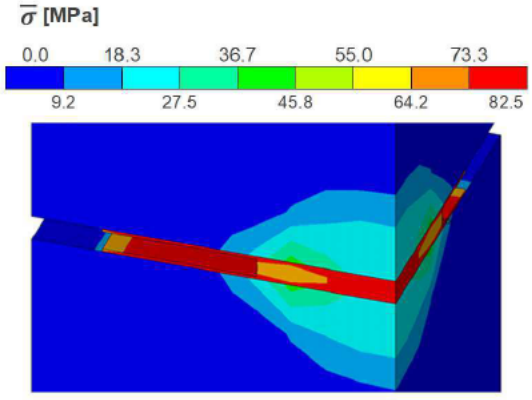

Figure 7. V ON MISES stress after cooling down to 77 K.

The accumulated equivalent plastic strain as well as the *VON MISES* stress are averaged over the center layers of the joint for analysis of the thermal cycling. Stress concentrations at edges and material interfaces are therefore not included. The equivalent plastic strain is given as accumulation per cycle. Figure 8 presents the result after the first 3 cycles.

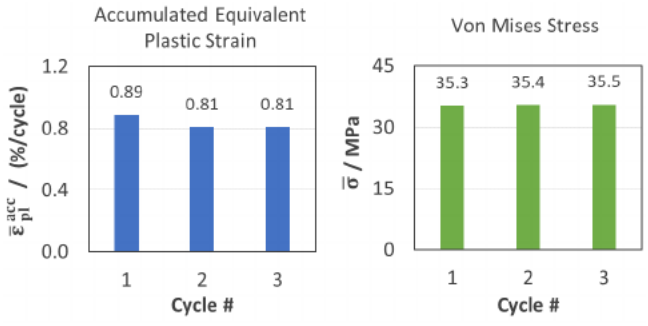

Figure 8. Accumulated equivalent plastic strain (left) and VON MISES stress (right) after the first 3 cycles.

The *VAN MISES* stress increases slightly for the first cycle due to strain hardening. It is only half as large at room temperature as at 77 K. The equivalent plastic strain accumulated per cycle settles after very few cycles to roughly 0.8%. These rather high values result from the large temperature step of 216 K and the large CTE mismatch between Si and Al, which produces a huge load of the joint. The relatively small joint height and its large diameter reinforce the behavior. Large shear components with large gradients develop towards the joint edges at Si-Al interfaces.

Caution is advised when analyzing absolute numbers since the elastic-plastic data of Al are subject to an unknown error. On one hand, tensile elongation values are estimated. And on the other hand, stress values are taken from a precipitation-hardening alloy (Al-1100) containing about 1% Si. Therefore, in the future, it is necessary to determine the material data of Al directly on the packages at different temperatures. The behavior of the bonded Al could in principle be more ductile so that the stress-strain curves are less steep. This would result in a lower *VON MISES* stress and higher plastic strain.

B. Aluminum and Gold shear strength

Chip TSB was performed at elevated temperatures of 100°C for Al-Al and 150°C for Au-Au. A bar chart shows the average shear strength of Al-Al and Au-Au samples (Figure 9). Shear strength was higher for Al-Al exhibiting values of 74 MPa ± 16 MPa compared to Au-Au with 40 MPa ± 15 MPa. The variation of bond strength can be attributed to the small pillar structure variation, which persists after Au-ECD and Al post-treatment using fly-cut planarization.

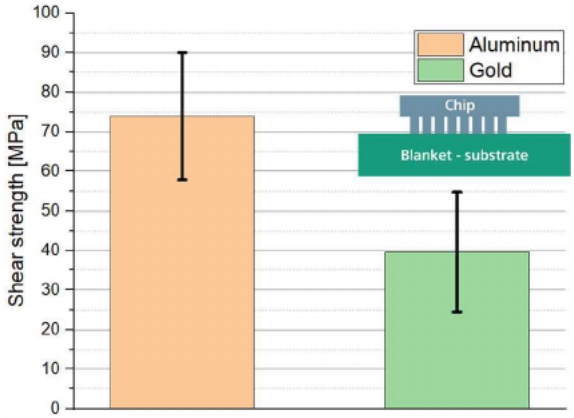

Figure 9. Comparison of Aluminum and Gold chip shear strength at room temperature

Shear tests of bonded Al samples were carried out after thermal stress tests of 5x and 10x cycles. Figure 10 shows shear strengths after 5x and 10x cycles at temperatures of +25°C and - 196°C. The average shear strength value (63 MPa ± 8 MPa) is similar to the shear strength values without the thermal cycling test in Figure 9 for Al bonded samples. The difference between 5x and 10x cycles shows that the bonded chip was not or only minimally damaged after the thermal stress test.

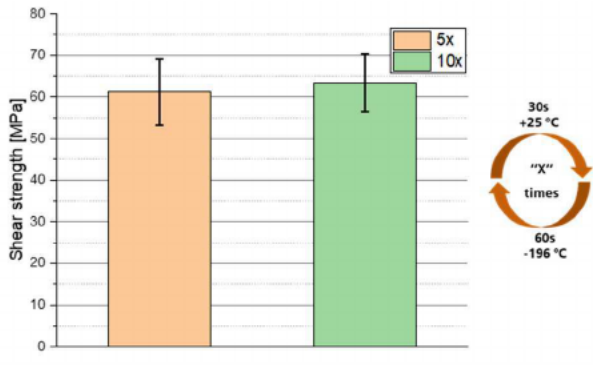

Figure 10. Shear strength of Aluminum chip after 5x and 10x cycles of +25°C and -196 °C

The cross-sectional images of Al-Al and Au-Au samples (Figure 11) show that both the pillar and substrate layer had made contact after TSB. From the measured pillar dimensions, the Au pillar remained close to its original thickness of 15.1 µm, but the Al pillar thickness decreased to 9.9 µm due to the high applied force on the chip. The width of the Au pillar was close to 100 µm, whereas the Al pillar's width increased by almost 15 µm.

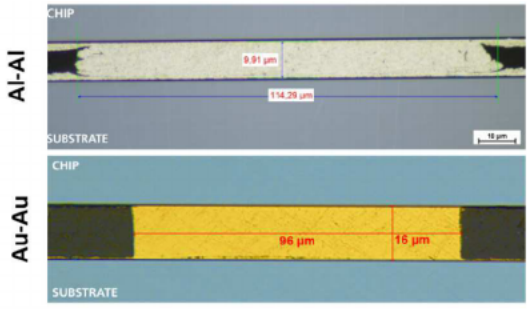

Figure 11. Cross section of gold and Aluminum chip after TSB bonding

Microscopic images (Figure 12) of different bond failures show that the metal-metal bond failed either at the chip-pillar interface (transferred pillar to the substrate) or the bond interface. Excessive damage to the Al pillar can be confirmed, showing that the pillar size changed along the pillar bonding direction. Therefore, adjustments to Al-Al bonding parameters should be made to reduce the excessive pillar damage.microscopic images of Au-Au samples confirm that the bonding mark and transferred pillars are regular in shape and correspond to initial dimensions.

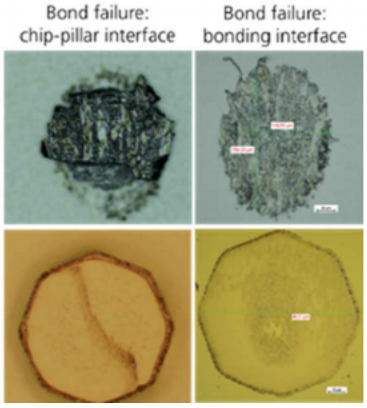

Figure 12. Light microscope image of bond failure of Aluminum and Gold chips after the shear test

IV. Conclusion

The Al-Al TSB was done at elevated temperatures showing the process's feasibility. The Al-Al samples showed higher average shear strength compared to the Au-Au samples. However, cross-sectional images showed that the Al pillar thickness changed by almost 5 µm in thickness from its initial size, which was not the case with Au pillars, where its pillar thickness did not change. It suggests that Al TSB parameters need to be adjusted to reduce the excessive deformation of the Al pillars for fine-pitch bonding applications. For further investigation, an optimized chip layout will be used to enable electrical test measurements and to examine the Al natural oxide at the interface of the bond. Additionally, different pitch sizes with varying numbers of pillars arranged in an array structure will be investigated to target fine-pitch applications.

The FE analysis provided an indication of a large load in the Al joint at 77 K. Changes in joint geometry to smaller diameters or larger heights can help to counter this large load. The FE model will serve as a starting point for analyses of possible ion trap layouts down to temperatures around 4 K. In this respect, the implementation of multiphysics in the model will help to gain system competence. A key task involves the determination of relevant temperature-dependent material data. To save computational time at the package level, simply meshed volumes with effective material properties could replace all but a few joints.

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