

Concepts for realizing High-Voltage Power Modules by Embedding of SiC Semiconductors

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Abstract— Today's power electronics modules typically consist of a ceramics substrate (DBC – Direct Bond Copper), carrying IGBTs, diodes or MOSFETs. These semiconductors are soldered or sintered to the ceramics and their top sides are interconnected by thick Al wires. An integration of further components or functions on the DBC substrate is difficult or even not possible. Therefore, driver circuits and controllers have to be mounted to a separate substrate, typically an organic Printed Circuit board (PCB). The PCB has to be connected to the DBC by wires or pins. The mechanical integration of the whole system requires a bulky housing.

Embedding of power semiconductors like SiC MOSFET allows a significant size reduction, improved electrical performance and a high degree of reliability of such modules.

In the last years, the capability of PCB embedding technology for the realization of low and high voltage power modules was demonstrated. Fraunhofer IZM together with partners from the industry demonstrated the feasibility for different applications, from single die SiC packages to high voltage automotive traction inverters.

In this paper, a general overview about innovative power module technologies will be given and the embedding of power semiconductors will be introduced in detail. It will address all most relevant point, like the demands on the semiconductor, the thermal and electrical considerations as well as the demands on the used materials

To address the integration of the required driver circuits and controllers, the idea of modularization such electronics systems will also be presented. Here already packaged components will be used and embedded into PCB layers too. As a result, a modular approach to form a complete system will be developed. Different functional layers, e.g. power switches, logic modules, will be formed and finally stacked und connected to form the system. The concept and first realized demonstrators will be discussed.

Keywords—*Embedding, PCB technology, SiC MOSFET, Power module*

I. INTRODUCTION TO INNOVATIVE POWER MODULE TECHNOLOGIES

The PCB based embedding of power semiconductors like SiC MOSFET or GaN provides several advantages. Beside the potential of miniaturization and the possibility of three-

dimensional approaches, the improvement of the electrical performance is a mayor benefit. The replacement of bond wires to contact the semiconductor with the use of direct copper connections, result in a very short connection length and with this in a significant reduction of parasitic inductance. As a result, the switching behavior can be improved and switching losses are reduced. The addressed applications can be manifold: (1) Single die packages, what we call "Prepackages", only containing one power semiconductor to form a very robust and improved package solution, that could be handled like an SMD component, (2) power modules, half bridge or complete inverter structures, for electrically improved systems, or (3) 3D modular power electronics, which provides the possibility to combine a power module with needed logic and driver functionality in a compact and robust monolithic block.

Looking on this technology, several companies are offering embedding approaches for power modules, most of them out of the PCB world. Schweizer Electronic (DE) and AT&S (AT) do have a long experience with their p² Pack [1] or ECP technology [2] respectively. In addition, other PCB manufactures gain more interest in this technology topic, like Würth electronic [3] or Unimicron Germany [4]. The basic principle of all the different ways to realize embedded component packages or modules is quite similar for all, and will be described in the following in detail.

II. EMBEDDING TECHNOLOGY

A. Variations of Power Embedding

In order to address high-voltage applications, a suitable electric isolation needs to be added to the embedded structure. On the other hand, this isolation layer also needs to ensure a sufficient thermal management, since e.g. a single SiC can generate more than 100W losses.

The method that will fit best into a PCB production environment would be an organic isolation layer [Fig. 1]. Such a film could be easily implemented into the PCB process flow. The organic material needs to provide sufficient breakdown voltage for e.g. 1.200V applications and a good thermal conductivity. However, these organic layers are limited in their thermal conductivity. Best in class provide 8 to 10 W/mK according to the datasheets. With this limitation, maximum losses and power density of modules are limited.



Fig. 1. Schematic of embedded structure with organic isolation layer

To address higher power densities the integration of ceramic substrates needs to be considered. These could be silicon nitride (Si_3N_4) AMB (active metal brazing), DBC (direct bond copper) or DPC (direct plated copper) substrates. These substrates are providing superior electrical isolation and thermal conductivity up to 90W/mK . Here the challenge is to combine the ceramic material with the PCB process sequence. In order to overcome this challenge, the ceramic substrate should be kept as small as possible and will be embedded into the PCB structure similar like the power component itself.



Fig. 2. Schematic of embedded structure with ceramic isolation layer

In Fig. 2 a schematic example for the use of an embedded ceramic is shown. In this case, the ceramic substrate is embedded into a base PCB substrate and the SiC die is assembled to this substrate and is embedded using several layers of epoxy prepreg material. Warpage control of the resulting substrate after embedding is a critical point and needs to be balanced, and is mainly determined by the size and density of the ceramic in the substrate.

For both variations, the by the power component generated heat, must be removed effectively from the bottom side of the chip. That is why a sufficient heat spreading, e.g. by thick copper layer, is important to realize an effective transfer at the heat sink or cooler.

B. Semiconductor

Typical values of SiC MOSFETs used in recent projects are an area of around 25mm^2 , thickness between $100\mu\text{m}$ and $400\mu\text{m}$ and maximum blocking voltage of 1.200V with currents up to 100A . In order to electrically and thermally design correct, the conductive losses needs to be known. These are determined by the on-state resistance (R_{DSon}). With modern generation SiC MOSFETs, R_{DSon} can be as low as around $12\text{m}\Omega$. More importantly is the temperature behaviour of R_{DSon} , since SiC will be operated with high junction temperatures of e.g. 175°C . At this operation state R_{DSon} can easily double or triple, which need to be considered for a proper thermal layout.

In order to be compatible with the embedding process, the components need to have a specified contact metallization. SiC power semiconductors have back and front contacts, typically the drain contact is the back-side, whereas gate and source are on the top side of the chip. The back contacts of most power semiconductors have by default a silver finish, which provides an optimal match with the Ag-sintering process, used for die attach. The top contacts (gate, source) of power semiconductors are typically delivered with a 1 to $3\mu\text{m}$

thick aluminum metallization. This metallization is not compatible with the micro via drilling process using UV or IR laser: The micro vias are cut through $5\mu\text{m}$ copper (on top) and the 50 to $80\mu\text{m}$ cured prepreg (glass fiber epoxy compound). During the laser drilling around 1 to $2\mu\text{m}$ of the contact metallization can be removed by the laser ablation process. Additionally, cleaning processes, required for the copper metallization, can remove up to $1\mu\text{m}$ of copper. Therefore the contact pad of the embedded component needs to provide a compatible metallization. Hence, a 10 - $12\mu\text{m}$ thick electroplated copper metallization is applied, ideally in a wafer level process. This 10 to $12\mu\text{m}$ copper pad metallization provides a sufficiently thick pad for a reliable micro via drilling and metallization process.

C. Embedding materials

For the embedding process for high voltage applications, two classes of materials need to be considered: (1) The embedding material itself and (2) thermally higher conductive isolators enabling the thermal management.

As the embedding material epoxy prepreg or copper clad (CCL) materials are used. Prepreg is the PCB initial material. It consists of a glass cloth of different types, different thickness of the glass cloth and the glass fiber itself, which is impregnated with a certain resin system. This resin is still not fully cured, but in a partially cured stage (B-stage). In this stage, the resin is still able to melt and flow while applying temperature and pressure and with that, filling any gaps within the circuit board and around the power component, which has to be embedded. Certain properties are mandatory, which are the following:

- **High thermal stability:** Since SiC MOSFETs will be operated at high junction temperatures, the embedding material needs to be capable of operating at these temperatures. Standard FR4 materials do provide glass transition temperatures (T_g) between 120 and 170°C . At this temperature, the polymer system changes from a hard (glassy) state to a soft state. That is why this temperature should not be exceeded in operation.
- **Sufficient Breakdown voltage:** Currently 850V inverter modules are of high interest, typically 1.200V SiC MOSFET will be used for this application. With these given numbers, the used embedding material should provide breakdown voltages of at least 2 to 3 times of these values.
- **Coefficient of thermal expansion (CTE):** The CTE should be well balanced to the different materials, which will be present in the embedded structure. Thermo-mechanical modelling will help to determine a well-fitting material selection.

Typically used materials for the embedding of power semiconductors do provide T_g up to 280°C and higher, as well as CTE between 5 and 9ppm/K . A careful testing of breakdown voltages is of high importance, since data sheet values may indicate only limited numbers, which will not give sufficient information for the material in operation. Finally yet importantly, all selected materials will need to be suitable to be processed in standard PCB equipment.

As already described thermal management and electrical isolation can be realized by ceramic substrates or organic highly thermal conductive layers. Here again, the breakdown

voltage and processability needs to be considered for their selection.

D. Process flow

The complete process flow for the embedding of power electronic devices like IGBT, MOSFET, SiC transistors or others is based on printed circuit board technology in combination with a suitable die attach method. Also, the material properties of the used FR4 materials are of paramount importance. Like already described, beside suitable thermo-mechanical characteristics, they need to provide the ability to withstand higher operational temperatures, because of the losses and resulting temperatures of the embedded power semiconductors.

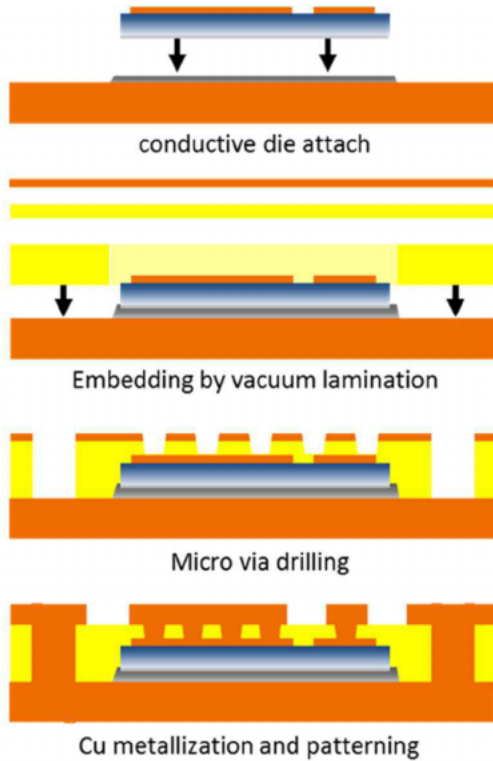


Fig. 3. PCB based embedding of power devices

The general process flow is shown in Fig. 3. On a suitable substrate the power components are assembled using a conductive die attach. This substrate could be a simple copper foil or leadframe, a high current PCB or even a base substrate with integrated electrical isolation like a ceramic substrate. The preferred method for mounting the semiconductors would be a low pressure and low temperature Ag sintering process. This method provides some advantages: First, it is capable to assemble the dies on a large panel format, enabling a highly parallel processing. In addition, the die bond accuracy, which is important for the following process steps, mainly depends on the accuracy of the die bond process, since, other than for a soldering process, the dies stay most accurate at their position during the sintering process. Additionally the Ag sinter layer provides an excellent thermal ($\geq 100\text{W/mK}$) and electrical contact ($\leq 0,008\text{m}\Omega\text{cm}$) to the substrate. If applicable, an Ag sinter glue could be used also. This would be possible if electrical and thermal demands are fitting with the characteristics of these glues. The main benefit of these glue, which consist of a metal-organic Ag system and a resin system for mechanical reinforcement, is, that they do not need

pressure to be processed, and sinter/curing temperatures are not exceeding 200°C .

The embedding itself is done by vacuum lamination of FR4 prepreg (glass fiber with B-stage epoxy resin) layers. Structured prepreg layers are used to compensate the height of die attach and die, and full layers provide the required isolation to the electrical layer above the die. Additionally a copper foil is applied which is needed for the metallization process. The embedding itself takes place by lamination of the stack in a standard multi-layer lamination press.

Laser via drilling is used to create contacts to the embedded die, which needs to be controlled and parameterized carefully, in order not to damage the chip. Blind via to the thick copper substrate or thicker copper layer are typically made by mechanical drilling. Subsequently the micro via are filled in a copper plating process, followed by the structuring of the electrical layer by lithography and etching of the copper.

The appearance of the printed circuit board with embedded components is the same as a conventional circuit board. Hence, in subsequent processes either additional signal layers can be processed, solder mask and surface finish can be applied, in order to mount further components on top of the embedded module, or additional heat spreaders or embedded modules of different types can be added onto the module [5].

III. APPLICATIONS

A. Single Die Packages – Prepackages

The most simple embedded power semiconductor structure is a package, which contains only one die. Here, the target is to create a robust housing for further production steps to form e.g. a half bridge structure, which uses the advantages of the embedding technology, nearly adding no thermal impedance and no inductance. Such packages are already on the market for some years, and gained more and more interest within project for module applications over the last time. One widely known example is GaNSystems GaN prepackage, Fig. 4. These packages are available in 100V and 650V classes and are manufactured in PCB embedding technology.



Fig. 4. GaNSystems embedded HEMT

At Fraunhofer IZM different types of SiC prepackages were developed (Fig. 5). One example for modularization of these packages is given in [6]. These prepackages are manufactured using the described process flow.

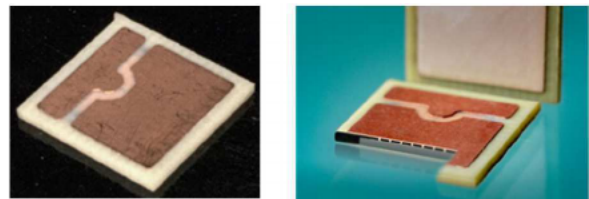


Fig. 5. SiC prepackages

On a thin copper foil the SiC MOSFET was assembled using a silver sinter die attach. A simple and robust package was formed by means of embedding technology, carrying gate and source contact on top and drain contact on the bottom side.

For the development of new power electronics concepts, prepackages with their own safety isolation become of interest. Therefore, a ceramic substrate will be integrated into the embedded like schematically shown in Fig. 6.



Fig. 6. Schematic of embedded (SiC) prepackage with integrated safety isolation

The process sequence will remain the same, with the difference, that in addition to the semiconductor, the ceramic substrate will be assembled to the base copper. As the ceramic substrate, a DPC with a $320\mu\text{m}$ Si_3N_4 ceramic and $100\mu\text{m}$ copper on each side is used in this example. In Fig. 7, a cross section of the resulting package is shown. These prepackages are designed for 850V applications using 1.200V SiC MOSFET. In the following modularization these prepackages can be handled like a SMD component.

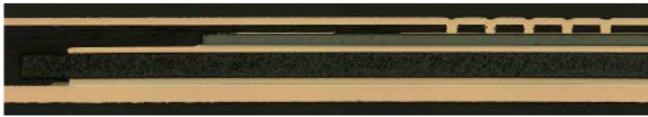


Fig. 7. Prepackage with embedded SiC MOSFET and Ceramic isolation

B. SiC Inverter with organic isolation

An early project for the realization of a SiC inverter with up to 100kW switching power targeted the use of an organic isolation layer. Instead of a ceramic substrate, a polymeric material with a thermal conductivity of around 3W/mK was used. The schematic of the module is shown in Fig. 8

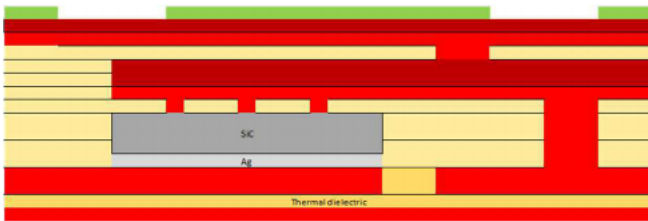


Fig. 8. Schematic SiC inverter with organic isolation

Within this module two times four SiC MOSFET (HS/LS) per phase were embedded. The switching current for each semiconductor is 50A. The resulting module combines the improved electrical characteristics, short electrical connections resulting in low inductance and lower switching losses, with the possibility to mount additional components, primary DC link capacitors, shunts, gate driver and connectors, directly and close to the switching cell. The final half bridge module is shown in Fig. 9.



Fig. 9. SiC halfbridge module with assembled components

C. SiC Inverter module with driver and logic integration

In the German funded project „SiCModul“, a new concept for power module fabrication was developed. The idea was to integrate safety insulation by a ceramic substrate and to manufacture two separate layers, power core and logic board, and join them together to finalize the module.

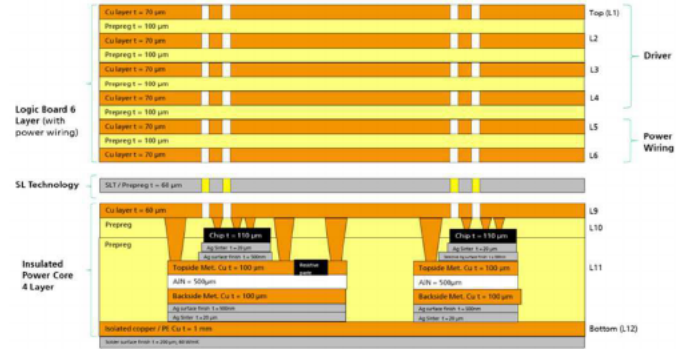


Fig. 10. Concept of SiC inverter with driver and logic integration

These power modules are fabricated based on the layer structure shown in Fig. 10. The fabrication was divided into two parts: the logic PCB and the power PCB with the embedded SiC MOSFET. The logic PCB consists of a 6-layer structure, with through holes, micro via and thick copper of $70\mu\text{m}$ in each layer. On the bottom side, partial silver plating was performed in the areas where the joining by sinter lamination technology (SLT) between logic and power PCB is made later.

The idea of sinter lamination technology (SLT) is to simultaneously produce an electrical (or thermal) contact, and to fill the cavities between the contacts with resin of the prepreg (PCB starting material) in one process step. In this process, a silver sintering paste is applied to one of the respective joining partners, usually by stencil or screen printing. To fill the cavities, prepreg layers are produced which contain openings at the positions where Ag is to be sintered. The entire stack of joining partners with Ag sinter paste and prepregs is then placed oriented to each other. The joining process takes place in a multilayer laminating press. In the first phase, Ag sintering takes place, as well as flowing and thus filling of the cavities. In the second phase, the epoxy resin of the prepregs is completely thermally cross-linked. After this lamination process, the joining of the individual layers is completed.

For the power PCB, 1mm thick copper is used as substrate. A DPC ceramic and the SiC MOSFET are mounted on this by means of Ag sintering and subsequently embedded and electrically wired using PCB embedding technology. The assembly is carried out in two steps. The DPC ceramic is mounted on the prepared 1mm copper substrate. This is done by stencil printing of the Ag sintering paste, placement of the DPC using automatic placement machines and subsequent sintering process (Fig. 11a). In the second step, the Ag sintering paste is applied to the sintered DPC using stencil printing, and the SiC MOSFET is assembled and then sintered (Fig. 11b, c).

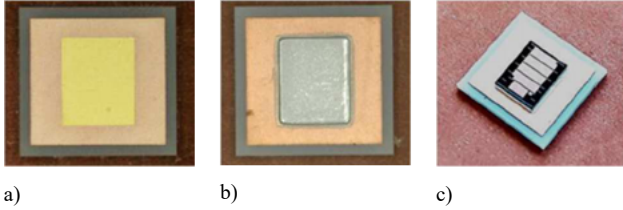


Fig. 11. Ag Sinter sequence DPC and SiC on 1mm copper

After that, the assembled substrate is ready for the embedding process. DPC and SiC MOSFET embedding is done by placing patterned prepreg layers containing the outline of the DPC and chip, and a full area prepreg layer for insulation and copper foil. This is followed by lamination in a PCB multilayer lamination press. Laser micro vias are fabricated to make the electrical contacts to the embedded SiC MOSFET, which are subsequently copper metallized. The copper layer is patterned subtractive by the fabrication of a photoresist mask and subsequent wet chemical etching. Finally, partial deposition of immersion silver (imAg) is performed on the areas where the Ag sintered connections to the logic PCB are made. After this, the power PCB is also available for joining with the logic PCB.

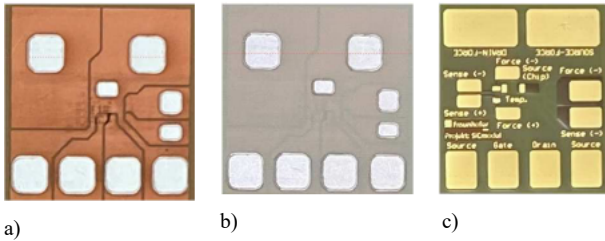


Fig. 12. Joining of Power coer and logic board by SLT

The joining of the two individual layers is done as shown pictorially in Fig. 12. First, the power PCB is placed on a press plate with pins at defined positions, which serve to align the individual layers to each other (Fig. 12a). Then a filler prepreg with cutouts in the areas to be sintered is applied (Fig. 12b). This serves to fill the cavities and to bond the two PCBs. Finally, the logic PCB (Fig. 12c), additional separation, and pressing materials are applied. The entire press stack is then loaded into the multilayer lamination press and pressed under temperature and pressure control.

The resulting module is shown in the cross sectional view in Fig. 13

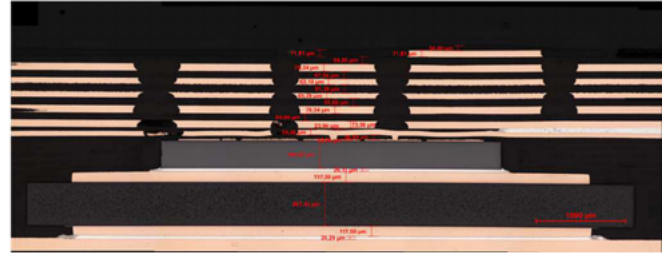


Fig. 13. Cross section of power module

D. GaN HEMT Modular Driver and Logic Integration

A new concept for the driver and logic integration into a compact power module was addressed in the German project “3D Leistungselektronik” (3D power electronics). The basic idea is to divide the complete module into different functional layers and finally join them to create a kind of monolithic block. The functional layers should be (1) the motherboard, (2) the driver module and (3) the power module, all together mounted to a heatsink. The schematic of the concept is illustrated in Fig. 14.

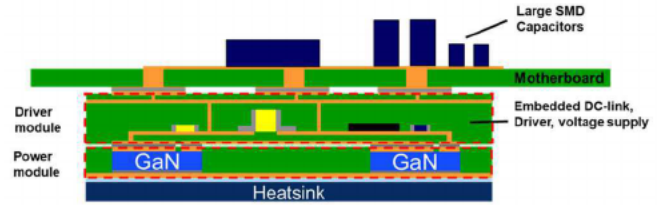


Fig. 14. Schematic of the 3D power system

For the driver module, also an embedding technology is used. Instead of bare dies already packaged SMD components, active and passive, are used. On a multi-layer core, SMD components are assembled by soldering (Fig. 15), and in the following embedded using epoxy prepreg layers. For the power modules, GaN prepackages are used. The electrical isolation is realized by a DPC ceramic. Prepackage and DPC are assembled using Ag silver sintering (Fig. 16), and are embedded by the use of prepreps in PCB embedding technology.

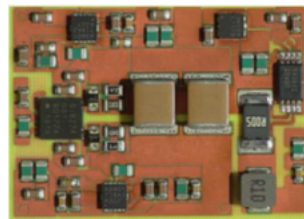


Fig. 15. SMD assembly for logic module

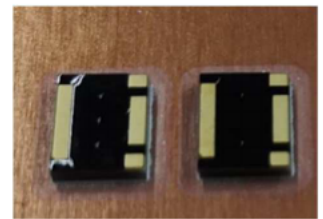


Fig. 16. GaN prepackages assembled to DPC and substrate

In Fig. 17 a cross section of the logic module is shown, with the different SMD parts visible.



Fig. 17. Cross section of embedded logic module

To join the driver and logic module, sinter-lamination technology (SLT) is used once again. In a similar way as already described, the different layers will be stacked and laminated in a multi-layer lamination press. Fig. 18 illustrates

a cross section through the complete stack, showing the GaN prepackages and the highest SMD component in the driver module.

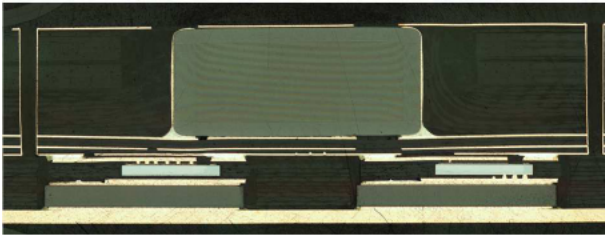


Fig. 18. Cross section of the Logic-Power module

The resulting Logic-Power module, with x/y dimension of only 3.5cm by 2.5cm and 4.5mm thickness, provides a monolithic and highly miniaturized component (Fig. 19).

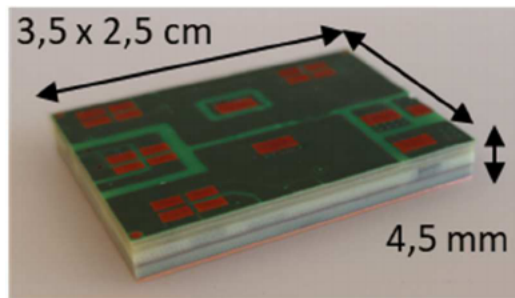


Fig. 19. Final Logic-Power module

As the final step, the complete system is assembled by soldering the Logic-Power module face down on the backside of the motherboard (Fig. 20). The backside of the power module provides the interface for the heatsink assembly.

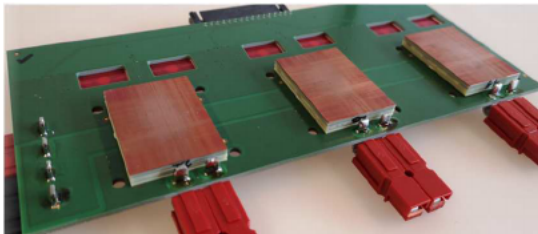


Fig. 20. Logic-Power modules soldered to bottom side of motherboard

On the top side of the motherboard, the larger SMD components, which cannot be embedded, are assembled as well as control components and connectors. The resulting complete three-phase power module is shown in Fig. 21.

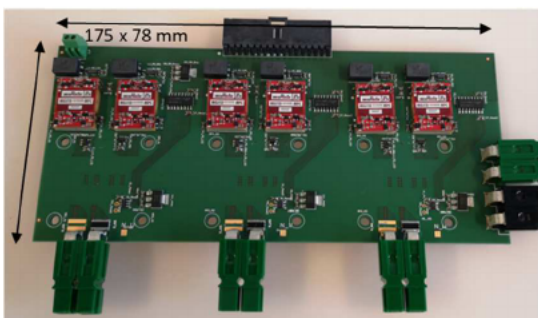


Fig. 21. Complete module with all top side motherboard assemblies

With the intended concept for a new kind of power modules, it was possible to demonstrate a way to realize a compact and highly miniaturized module in a robust monolithic block, carried on a motherboard. With the integration of the electrical isolation within this module, a best possible thermal path could be realized. In addition, a very robust and highly reliable construction was addressed. To join the different functional layers the novel sinter-lamination technology was applied. It is intended to develop this concept further to provide a platform for scalable configurations. Although GaN HEMTs were used in this project, the concept can equally be applied to SiC MOSFET applications.

IV. SUMMERY

Embedding of power electronic components provides a large benefit in terms of reliability, volume reduction and electrical performance. Direct copper connection and the resulting short connection length lead to a significant reduction of parasitic inductance, resulting in improved switching behavior and switching losses. Proper thermal and electrical design is a key enabler for such high performance power modules.

Meanwhile, there are many different ways to realize innovative power semiconductor packages and modules, based on PCB embedding technologies, developed. Which technology fits best often is defined by the demands of the application.

A new topic is 3D modular power electronics. This technology approach can provide compact embedded power electronics systems, and can be realized by use of established processes. It is also intended to provide a scalable platform for different configurations.

V. ACKNOWLEDGMENT

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