Novel low temperature and low pressure sintering of ADAS radar sensor antenna stack

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Abstract— A low temperature and low pressure sintering of antenna stacks with the promising prospect of achieving a single step bonding process of multi-layer wave guide antennas for automotive radar sensors is demonstrated. Silver nanoparticles (Ag-NP) paste with the ability to sinter at 200°C in air allows for easy integration into standard surface mount device reflow process. The paste drying and sintering process of the Ag-NP paste is first optimized using dummy test chips to reduce the typical voiding and channeling in the interconnect when sintered without pressure. In especially, a slow ramp rate with an integrated pre-drying step is applied after placement of the test chips into the wet paste. Afterwards, the process is transferred to the antenna. However, pre-existing bending in the large antenna layers challenges the sintering process without pressure, e.g. larger amounts of paste need to be applied for compensation of the bending. Therefore, the use of a low bonding force in observed to improve the quality of the sintered interfaces. Near bulk like Ag sintered interconnects were realized.

Keywords — sintering, ADAS, nano Ag sintering, low pressure, low temperature, antenna stack, radar

I. INTRODUCTION

Autonomous driving is a megatrend of today and advanced driver assistance system (ADAS) sensors play a critical role enabling this megatrend, being the fastest growing segment in automotive today. Cameras, radio detection and ranging (RADAR) and light detection and ranging (LiDAR) are the sensors enabling the environmental perception of future autonomous cars. Radar is considered indispensable since it can work under any weather conditions due to its unique ability to penetrate smoke, fog, dust, rain and/or snow. It also has a strong anti-interference characteristic and high accuracy of speed and distance measurement [1].

In the standard automotive ADAS applications, radars can be characterized into three main categories: (1) short range radar (SRR), medium range radar (MRR) and long-range radar (LRR). SRR is typically used in applications such as parking assist and has a detection range of ~ 30m and a wide field of view (FOV). MRR has a similar FOV to SRR, but a higher detection range of upto 130m and are typically used for applications such as blind spot detection, lane keeping assist and lane changing alert. LRR are used in applications with a range > 180m but have a comparatively small FOV of ± 20°. These are typically used in applications such as adaptive cruise control, collision avoidance systems and automated emergency braking [1].

Considering the stringent safety and reliability requirements, it is essential to design and develop robust sensors while at the same time ensuring low cost, excellent process traceability and improved reliability and performance. In addition, reduction of complex assembly processes is also desired. Therefore, novel materials and efficient and effective processes need to be designed and developed.

A key aspect of the radar architecture is the radio frequency antenna. For automotive radar sensors microstrip patch antennas were dominating, due to their compact size, low profile, and directional radiation pattern. Enabled by improvements of accuracy of injection molding, plastic waveguide antennas were introduced [2] and getting more and more popular. After molding, the individual plastic layers of the antenna are metallized and soldered on top of each other. The fully assembled antennas are tested and finally attached to the printed circuit bord (PCB). The antenna considered in the paper, consists of a multi-layer wave guide antenna. Due to the plastic material (ABS) of the antenna, it is challenging to realize an appropriate solder hierarchy, i.e., solder the single layers of the antennas on to each other using a solder with higher melting point than standard SAC solder used for board level attachment. Therefore, the antenna stack layers are first soldered using a low temperature solder and then the stack is soldered on to the populated PCB to undergo a second reflow process where the surface mount devices (SMDs) are soldered on to the PCB. The second reflow process can cause remelting the low temperature solder that bonds the antenna stacks together and risks reduction of antenna performance due to reposition or misalignment of the stacks.

Low temperature sintering is, therefore, an attractive alternative. The present paper deals with the development of a novel low temperature & low-pressure sintering process for injection molded antenna stacks. A sintering process using a low temperature and in air sinterable Ag sinter paste is investigated, providing the possibility of easy integration into a standard SMD soldering line. The goal is to realize a pressureless sinter process wherein the individual antenna stack layers are sintered under pressureless conditions in air and at temperature substantially below the peak soldering temperature of 255°C.

II. Materials and Methods

A. Sinter pastes and device under test

Two different commercially available Ag sinter pastes were considered for the study. A pure nanoparticle (NP) based Ag paste and a nanoparticle and salt (NP+S) based Ag paste were initially evaluated to ascertain their performance. Both pastes are specified for pressureless sintering. They can be stencil printed or dispensed. While the pure NP based Ag paste was capable of sintering at temperature as low as 175°C under air, the NP+S paste has a minimum sintering temperature of 250°C.

The antenna stacks have an overall surface area of 1000mm² and Ag coating on the ABS plastic as shown in Fig 1. The pastes is dispensed as 1mm wide track with a measured thickness of approximately 80 µm onto the bottom stack layer and the top layer is assembled onto it manually using the alignment holes as provided in the design.

For the development of the sinter process, first, small 1mmx1mm test chips with a 120 µm thickness were used. Afterwards the process was applied for the assembly of the antenna stacks.

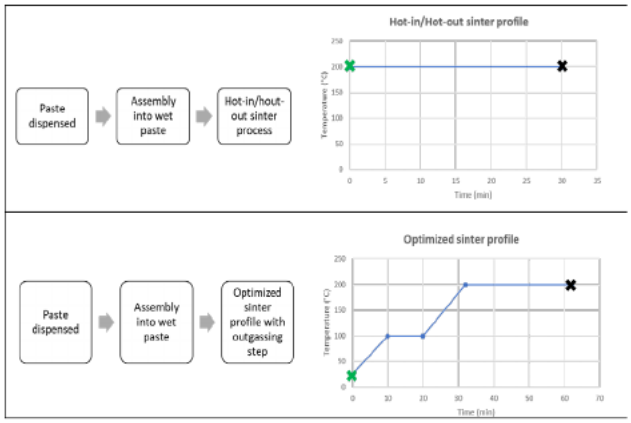

Fig. 1 Sinter process: The green marks indicate the point of placement of the chips and the black marks indicate when the assembly is removed from the oven after sintering. For NP the sinter temperature is 200C and for NP+S 250C.

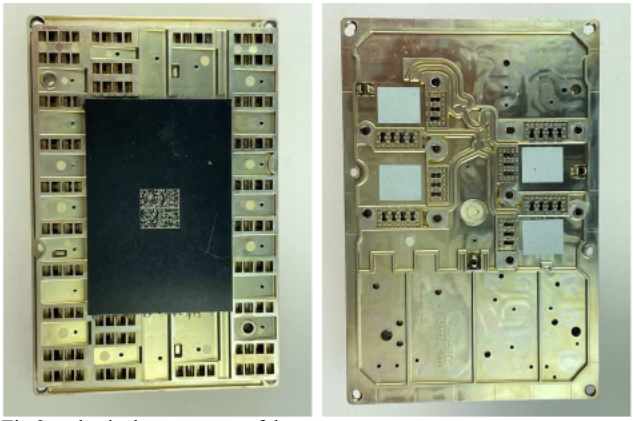

Fig 2 – physical appearance of the antenna.

B. Sinter pastes and device under test

The sinter process is depicted in Fig. 2. For sintering without pressure, the chip is placed into the wet sinter paste. The hot-in/hot out process describes the process in which the device is placed into the hot oven. Therefore, the heating up to sintering temperature is fast but depends on the thermal mass of the product.

C. Sample preparation & characterization techniques

For the initial process investigation 1mm² test chips with a thickness of 120 µm and an Au metallization surface finish were used as standard test vehicles. Aluminum insulated metal substrates, also with Au surface finish were used. The commercial Ag pastes was carried out by stencil printing using a PBT-Uniprint-PMGo3v semi-automatic printer and a 75 µm stencil. The sintering was performed without applying pressure. in air in using a Memmert convection oven with 100% fan speed.

For the assembly of the antenna stacks the pastes were dispensed using a Musashi dispenser with a dispensing pressure of 20kPa and nozzle diameter of 0.15mm. Considering the limitations of the temperature as discussed above, solely the NP Ag sinter paste was considered for the sintering of the antenna stacks. Sintering was performed without and with small pressure in the Memmet convection oven. To apply pressure, a tape was attached tightly at four positions around the stack to equalize bending and hold the antenna stacks in place.

Optical microscopy imaging was performed on a Keyence Digital Microscope. Profilometry is performed using a Nanofocus profilometer. Scanning Electron Microscopy (SEM) analysis was performed using a ZEISS EVO MA15 microscope.

III. Results and Discussions

A. Development pressureless sinter process

As mentioned earlier, the initial tests to understand the voiding behavior of the pastes was carried out with 1mm² test chips (120 µm thickness). The test chips were placed into the wet paste and the hot-in/hot-out process was applied. As can be seen in Fig. 2, the hot-in/hot-out sintering process resulted in a high rate of defects in both the NP and the NP+S pastes. However, the defects manifested differently between the pastes. While in case of the NP paste a high degree of voiding and channeling defects were seen. This is also evident from the SEM imaging of the cross-section of the sintered interconnects as shown by the red arrows in Fig. *3*. The channels are observed to follow the entire thickness of the interconnect i.e., from the substrate to the chip interface. The hypothesis for explanation of this phenomenon is that during too fast evaporation of organics sinter particle lose contact and the material shrinkage leads to the formation of these channels. One possible process step to reduce these effects is by introducing a pre-drying and/or a slow ramp step [3],[4] which is discussed later. It is important to note that without a pre-drying step or a slow ramp rate to sintering temperature and by following a hot-in/hot-out process, even within a small chip area of 1mm², large number of defects are observed. The waveguide sealing ring, has a similar width of 1

mm. Therefore, the voiding and channeling is expected to be similar.

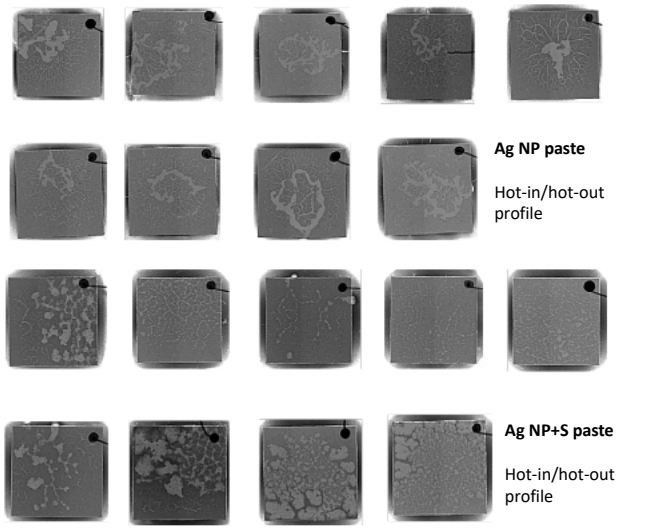

Fig. 3 – X-Ray analysis of the NP and NP+S paste after hot-in/hot-out sintering process following die-placement in wet paste with 0.1N placement force.

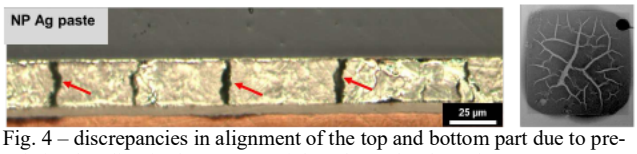

Fig. 4 – discrepancies in alignment of the top and bottom part due to pre-existing bending in the test material as shown by the red arrows.

The inhomogeneities in case of the NP+S paste were large voids that appear to be highly localized as shown by the red arrows in Fig. *4*, indicative of the inhomogeneous dispersion of the Ag salt in the paste and the localized decomposition of the same. Therefore, contrary to the NP paste where a very dense interconnect is observed between the vertical channels, in case of the NP+S paste the sintered microstructure shows poor sintering between the particles. This has also been reported to lead to poor performance under thermal shock conditions [5].

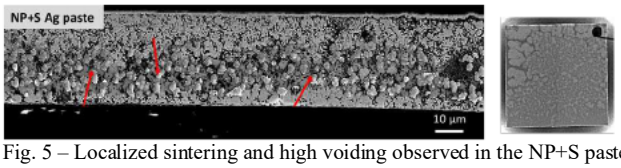

Fig. 5 – Localized sintering and high voiding observed in the NP+S paste following the hot-in/hot-out sintering process, consistent with features observed under X-ray analysis.

To improv the sintering results, a two-step sintering process was evaluated by introducing an intermediate step at 100°C and a slow ramp to the sintering temperature. The NP and NP+S pastes was sintered at 200°C and 250°C in air respectively.

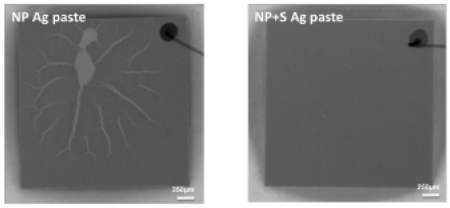

Fig. 6 – X-ray analysis of the sintered interconnects after introducing the two-step sintering process after placing the chip in the wet-paste.

As can be observed from Fig. *5*, the introduction of the two-step sintering process drastically reduced the defects in the NP+S paste and considerably reduced the voiding in the NP paste. It must be noted that unlike a pressure-sintering process where the paste is printed, pre-dried and the chip is placed in the pre-dried paste, in this pressureless sinter process, the chip was placed in the wet paste at room temperature with only 0.1N placement force, but instead of a hot-in/hot-out process as earlier followed, the two-step sintering process was introduced to allow for the efficient outgassing of the binder. This is similar to a pre-drying step in a pressure sinter process, but here with the test chip already placed in the wet paste. This step ensures a slow and improved degassing of the organics in the paste. Then, the sintering temperature of 200°C for NP and 250°C for NP+S is reached at a ramp rate of ~8°C per min and an isothermal sintering step at 200°C for 30min is applied. Finally, the samples are removed from the hot-oven.

B. Bonding of antenna stacks

Following the preliminary analysis with the two Ag sinter pastes, the NP Ag paste was chosen for further analysis despite the risk of the development of vertical channels as observed in the preliminary study with the 1mm² test chips. This is because, the paste is capable of sintering in air at 200°C. Further, although in this study, the NP Ag paste was dispensed, a dipping/stamping process can also be realized with this paste. However, that would limit the bond line thickness (BLT) and is part of a larger ongoing study to understand the impact of the BLT on the performance of the antenna stack and the reliability.

The NP+S paste required a minimum sintering temperature of 250°C which is critical for the antenna stack material which is desired to withstand a maximum of 250°C and only for short durations (typically durations as defined for peak soldering temperatures in standard SMD solder profiles). Further, the paste required a minimum sintering time of 30 min and therefore under the present design restrictions, such a process is not desirable.

The NP Ag paste is composed of NPs of ~80nm and requires deep freeze (-40°C) storage. Therefore, it is allowed to thaw at room temperature for 1 hour before dispensing. The paste is dispensed by a Musashi dispenser with parameters as described earlier by inputting a CAD file to the printer which replicates the wave guide antenna structure on the stack.

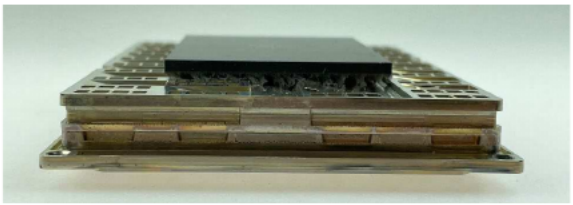

Fig. 7 – Optical image of the assembled antenna stack with a standard soldering process.

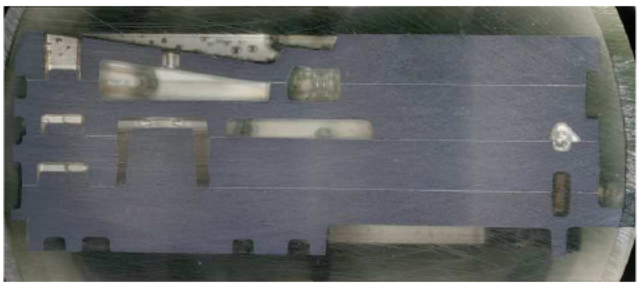

Fig. 8 – optical image of the cross-section of the soldered antenna stack, showing the multi-layer structure.

The profilometer analysis of the dispensed trace showed a thickness of ~80µm after dispensing. Warpage is a well-known and commonly observed phenomenon in microelectronics packaging for PCB substrates. In the sinter process no liquid phase forms. Therefore, contact between the sinter particles and the metallized antenna stacks is more critical compared to soldering. Unlike under pressure sintering, where bending of the chip or the substrate can be compensated to a certain extent by the application of the external pressure, within a pressureless sintering process, any pre-existing bending can compromise the contact between the bonding interfaces and thereby lead to poor sinter contacts. The antenna stacks used in this study showed pre-existing bending between the stacks.

A pressureless sintering step was followed after printing the NP Ag paste onto the individual layers of the antenna stack and assembling the stacks over each other manually. Therefore, the squeeze out of the paste during assembly could not be avoided. A slow ramp two step sintering process with the first step at 100°C reached at 7°C/min, followed by sintering at 200°C in air for 30min with a ramp rate of 8°C/min from the intermediate step of 100°C to the isothermal sintering step of 200°C.

The SEM analysis of the sintered interconnect (Fig. *8*), cross-sectioned along the yellow dotted line as shown in Fig. *6*, however shows poor sintering along both the edges and the presence of large voids between the stacks.

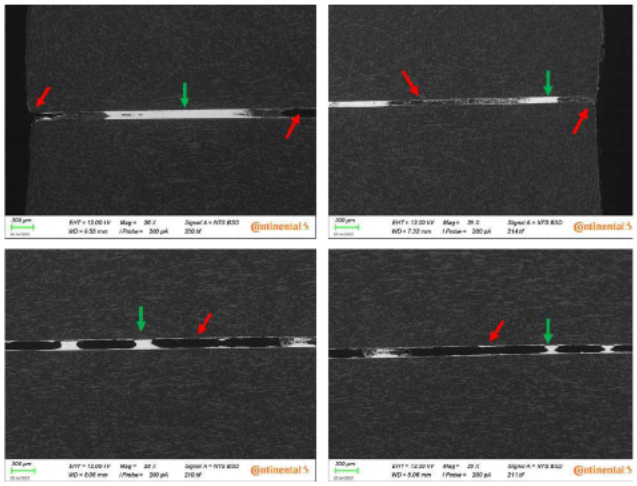

Fig. 9 – SEM analysis of the cross-sections showing sporadically well sintered areas (green arrows) among large voids (red arrows) after pressureless sintering for 30min in air at 200°C.

Therefore, to further improve the process, a small force of 8N is applied across the entire antenna stack, by placing a bare Cu block on the antenna stack. The SEM analysis of the sintered interconnect shows a more homogeneous and well sintered interconnect compared to the pressureless sintered sample. As can be observed from Fig. *11*, well sintered interconnects are realized also along the edges in comparison to Fig. *10*.

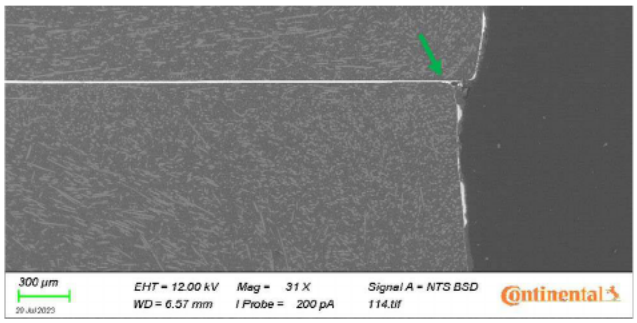

Fig. 10 – SEM analysis of the cross-sections showing well sintered areas interconnect after sintering for 30min in air at 200°C while applying a force of 8N over the entire area of the antenna stack.

Further analysis, as depicted in Fig. *12*, that bond line thickness (BLT) across the sample is not uniform. Also, the presence of the defects similar to those observed earlier for the test chips, i.e. vertical cracks that exist along the entire thickness of the interconnect, between the interfaces.

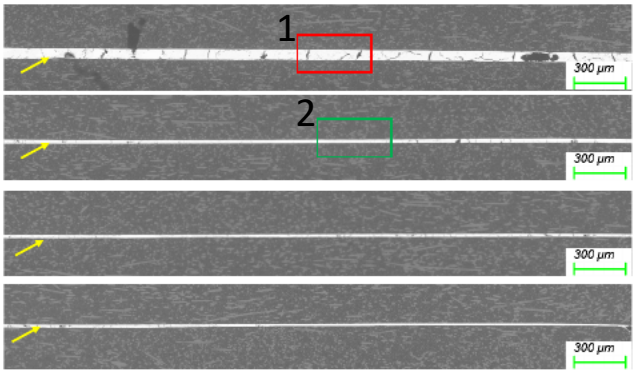

Fig. 11 – SEM analysis of cross-sections of multiple areas along the edge shown in Fig.6, showing sintered microstructure after sintering for 30min in air at 200°C while applying a force of 8N over the entire area of the antenna stack.

As can be seen in Fig. *13*, the defects are cracks. Similar observations were made in the preliminary studies with the test chips (Fig. 3). However, near bulk like interconnects are observed around these defects and in other areas (Fig. 11 image 2), indicating the potential of the NP Ag paste of realizing bulk Ag interconnects even under low pressure bonding conditions. It must be noted such bulk like sintered areas were also observed under pressureless conditions as seen in Fig. 8, but were sporadic in nature owing to the pre-existing warpage in the antenna stack layers. Therefore, if this issue can be addressed, the NP Ag paste has the potential to realize good sintered microstructure even under pressureless conditions. While it is desirable to eliminate the vertical cracks in the sintered microstructure, its impact on the reliability is unknown at the moment and needs further detailed analysis. In general, due to the shrinkage during sintering, it might not be completely possible to eliminate these vertical cracks. Therefore, as in case of soldering where in a standard SMD soldering profile no vacuum steps are included and instead an acceptable void rate is determined for specific solder materials and applications, the acceptable defect rate for sintered interconnects must also be defined. Thereby, a balance between process times and acceptable defects can be determined.

Fig. 12 – Magnified SEM images of the areas 1 & 2 shown in Fig.10.

IV. CONCLUSIONS

Low pressure and eventually pressureless sintering with NP Ag sinter paste offers a promising alternative to soldering of antenna stacks in ADAS Radar sensors, eliminating the risk of remelting of the solder.

The possibility to sinter in air and at a temperature of 200°C allows the sintering of the antenna stacks without damaging the plastic material by high process temperature. Furthermore, there is no risk of remelting the solder in the followed SMD reflow process to attach the antenna to the PCB.

Therefore, low pressure, and low temperature sintering in air with NP Ag paste is shown to be a promising approach to bonding antenna stacks together and eventually to the PCB in a single step without affecting the standard soldered SMD components. Near bulk like sintered microstructure can be realized and a potential towards miniaturization can be evaluated.

For a required high yield process, like in case of soldering, the acceptable defect rate for sintered interconnects must be determined, specifically the impact of vertical cracks as

observed in this case with the NP Ag paste, on the reliability must be ascertained.

In addition, potentially, the sinter process could be integrated into the existing SMD soldering process: The antenna layer are not bonded in a separated process but stacked onto the PCB. Within the SMD process also the sintering would be performed. However, to implement such a process the sinter time would need to be reduced. Furthermore, warpage in the antenna stacks is a challenge to realize well sintered interconnects and must be addressed.

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