Reliability of Copper Sintered Interconnects under Extreme Thermal Shock Conditions

Sri Krishna Bhogaraju[1]*, Francesco Ugolini[2], Federico Belponer[2], Alessio Greci[2] and Gordon Elger[1]

[1]*Institute of Innovative Mobility, Technische Hochschule Ingolstadt, Esplanade 10, 85049, Ingolstadt, Germany

[2]AMX Automatrix srl, Località Bolina, 1D/1E, 25085 Gavardo BS, Italy

*Email: srikrishna.bhogaraju@thi.de Tel: +49-841-9348-6449/6416

Abstract— Copper flakes-based sinter paste showed high reliability under thermal shock conditions. A dense and homogeneous interconnect was realized while sintering for 5 min at 275°C under 15 MPa bonding pressure, with the flakes showing the unique behavior of stacking over each other to realize a dense and homogeneous interconnect. Porosity under 10% could be achieved. The paste could be sintered under a constant nitrogen flow and did not need a fully inert atmosphere during sintering. Under high stress thermal shock cycling of +175/-65°C, the sintered interconnects showed a drop of 25% in the shear strength values after 1000 TST, consistent with observations made with Ag sintering. Thermal conductivity more than 200 W/mK and electrical conductivity of 20 Ms/m is achieved using the Cu sinter paste.

Keywords — sintering; copper flakes; reliability; SiC, die-attach

I. INTRODUCTION

New power electronics applications, mainly driven by the rapid pace of electrification in the automobile industry has necessitated the need for novel, sustainable materials with improved reliability [1], [2]. Conventional lead free-based solders have a low melting point (220-230 °C), thereby limiting the reliable temperature use to below 150 °C.

Among the alternatives, solid state sintering has shown a high rate of adaptability by the industry. Ag sintering under pressure is industrialized and has proven to be a reliable interconnect material [3]–[6]. But, Ag is expensive and prone to electromigration [7]. Cu offers the next best alternative to Ag and has been the focus of research and development.

However, Cu is prone to oxidation. Organic capping agents, sintering under formic acid enriched nitrogen/forming gas or pure H_2, or the use of a binder with the in-situ capability to reduce copper oxides are some of the common approaches to tackle the issue of oxidation. For Cu sintering to be easily adopted by the industry, it is essential to design a paste capable of operating in the similar process window as is established for Ag sintering in the industry today. Therefore, for the overall cost of ownership to be attractive, not only should the material cost be low, the handling and operating costs of the Cu sinter material should also be comparable, if not better than commercial Ag sinter materials.

Ag sintering under pressure is an industrialized process in the power electronics packaging industry with numerous publications on the reliability of Ag sintered interconnects for die-attach applications. Flakes based Ag sinter pastes have been subject to harsh thermal cycling of -50/+250 °C with a dwell time of 30min. While initially sintered interconnects showed a high shear strength of 45 MPa, it degraded drastically to 11 MPa after 750 cycles. The degradation is attributed to a combination of degradation of the sintered microstructure and the delamination between the die and the sputtering layer [8]. Typically, a crack propagates from the edges to the center of the die. However, recent publications in the field of Ag sintering, comparing nanoparticle based Ag sinter paste and bimodal (nano + microparticle) Ag sinter pastes have shown that delamination in the bimodal paste was faster than in case of the nanoparticle based paste when performing TST at -40/+150°C. Two different failure mechanisms were also reported, namely, edge crack mode and void growth mode [9]. Recent studies on Cu nanoparticle sintering have studied the effect of oxidation on the strength of the sintered interconnect after thermal ageing in air [10]. It is reported that the oxidation initially leads to the increase in the density of the sintered microstructure as well as the shear strength by filling the pores, eventually however leading to a drop in shear strength due to coarsening by the growth of copper oxides around the sintered nanoparticles. Grain boundaries are observed to act as nucleating sites for oxide, leading to formation of nanovoids. However, by achieving a dense and homogeneously sintered microstructure (~10% porosity), the oxidation is reported to be significantly limited [10]. Therefore, working with flake type particles offers a substantial advantage in realizing a dense sintered microstructure, which is discussed later in the paper.

II. MATERIALS AND METHODS

A. Sinter paste & characterization

Microscale copper particles-based paste, commercially available as Cuprum 81 from CuNex GmbH, capable of sintering at 275°C under constant nitrogen flow was evaluated. The unique chemistry of the paste allowed for sintering under N_2 flux, eliminating the need for a vacuum step prior to introducing N_2 into the sintering chamber. Therefore, an inert atmosphere during sintering was not necessary. Non-functional SiC devices with Ag end metallization and a footprint of 24mm² were used as test devices in the study. These were sintered onto Si_3N_4 based AMB substrates, also with Ag end metallization. A two-step sintering process is designed. The paste was printed using a 75 μm stencil on a Uniprint PBT Go3v semi-automatic

stencil printer using a squeeze pressure of 20 N, printing speed of 13mm/s and a stencil separation speed of 2.3mm/s. A double stroke printing was performed. After printing, the paste is pre-dried in air at 100°C for 5 min. Finally, sintering was carried out by the application of 15 MPa bonding pressure at 275 °C for 5 min on a AMX P100 sinter press at the application lab of AMX Automatrix in Gavardo (BS), Italy (Fig. 1).

Cross sections were prepared with a JEOL SM-09010 Ar-Ion beam miller. Optical microscopy imaging was performed on a Keyence Digital Microscope. Profilometery is performed using a Nanofocus profilometer. Scanning acoustic microscopy (SAM) imaging was performed on a Nordscan Sonoscan D9600 with 50MHz transducer. Shear tests were performed on a XYZ-Condor Sigma Lite shear tester under a shear speed of 250 μm/s and a shear height of 20 μm. Scanning Electron Microscopy (SEM) analysis was performed using a Zeiss Auriga 40 Crossbeam microscope. The thermal conductivity of the sintered samples was measured by In-Plane Thermal Material Analyzer (LaTIMA) and the electrical conductivity was measured using the electrical conductivity analyzer (ECLA). Both LaTIMA and ECLA measurements were performed by Berliner Nanotest und Design GmbH [11]. Profilometer measurements of the printed samples was completed using the Nanofocus profilometer. Thermal shock test (TST) was performed on a Thermotec shock chamber with a profile +175/-65°C, air-air with a dwell time of 30 min.
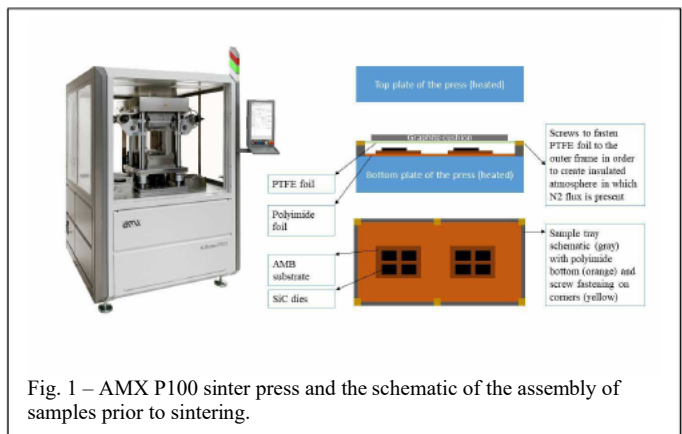

Fig. 1 – AMX P100 sinter press and the schematic of the assembly of samples prior to sintering.
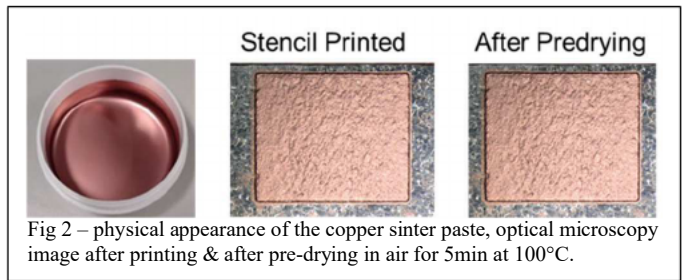
III. RESULTS AND DISCUSSIONS

Fig 2 – physical appearance of the copper sinter paste, optical microscopy image after printing & after pre-drying in air for 5min at 100°C.

The paste shows very good form adherence and printability as shown in Fig 3. No bleed out is observed. Hot-die placement as is the case with many Ag sinter pastes was not required. Die placement could be performed at room temperature with a placement force of 0.1N. The paste retained its tackiness even after pre-drying. Therefore, the SiC die could be placed without the need for any tacking agent to hold it in place.

The freshly printed paste had a measured height of 64 ± 3 μm. After pre-drying, the height of the printed paste was 51 ± 3. The measurements were averaged across 16 samples. After sintering, the bondline thickness (BLT) measured on the cross-sectioned samples across 4 different dies and 10 positions for each die (40 positions in total), averaged to be 12 ± 2 μm.

In conclusion, the paste showed a reduction of ~20% in print height after pre-drying and a reduction of 82% from the original printed paste to the final sintered BLT. This is attributed to the stacking nature of the flakes. As seen in Fig 3, a clear indication of this phenomenon is observed under low bonding pressure sintering (5 MPa), indicating the flake type morphology and the ability of the flakes to orient parallel to the interfaces. With the application of a higher bonding force, a dense and homogeneous interconnect with uniformly distributed porosity is obtained as seen in Fig. 4.
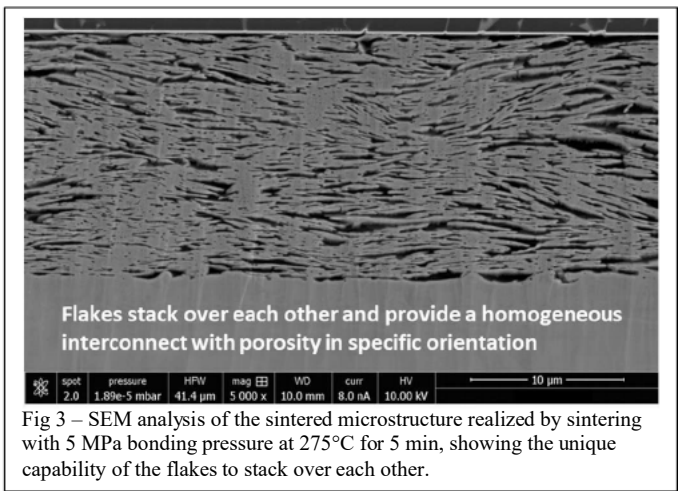

Fig 3 – SEM analysis of the sintered microstructure realized by sintering with 5 MPa bonding pressure at 275°C for 5 min, showing the unique capability of the flakes to stack over each other.

To understand the thermal and electrical properties of the sintered microstructure, stripes measuring 5mm x 50 mm, were manually stencil printed onto stainless tell substrates using a 150 μm stencil. These stripes were sintered at 275°C for 5 min, resulting in a dense sintered microstructure (Fig. 5). Three sample stripes were measured by LaTIMA and ECLA. The average width and thickness of the samples are measured to be 5.23 ± 0.15 and 50 ± 4 μm respectively, resulting in a thermal conductivity of 205 ± 27 W/mK and an electrical conductivity of 20.45 ± 1.76 MS/m.
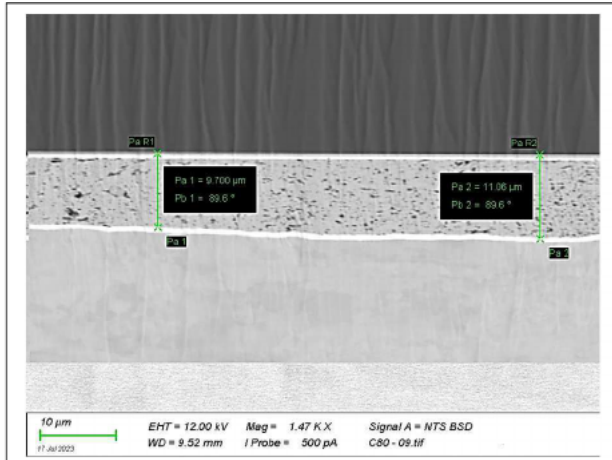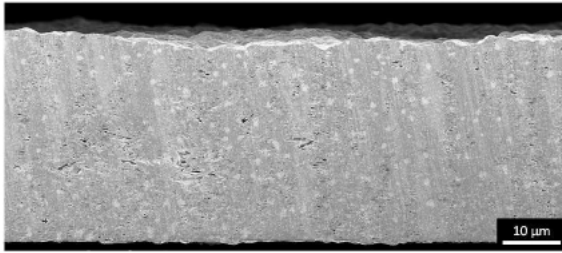
2

Fig. 4 – SEM analysis of the sintered microstructure.

Fig. 5 – SEM analysis of the stripes used for LaTIMA and ECLA analysis.

Fig 6 – (above) original SEM image of the sintered microstructure, scale bar referring to 5 µm and (below) ImageJ threshold image used to calculate porosity of the interconnect. The red highlights showing the pores.

Fig. 7 – Backside SAM analysis of the sintered interconnect after TST at +175/-65°C, air to air, 30min dwell time. Red arrow shows the crack.

The porosity of the sintered interconnect as measured using the open-source ImageJ software resulted in a porosity of 8.6% (area %), a pore circularity of 0.9 ± 0.2 (a value of 1 indicating the pores are circular) and pores with an average width of 0.23 ± 0.1 µm and height of 0.22 ± 0.09 µm. The measurements indicated that the interconnect is largely dominated by nearly circular pores, apart from some long, interconnected pores as highlighted by the yellow marking in Fig 6. All values were measured across 4800 elements in a SEM cross-section of the sintered interconnect as shown in Fig 6.

The shear test results between the as-sintered samples and ones after 1000 TST are compared. As sintered interconnects showed a shear strength of 60.5 ± 9.5 MPa which reduced to 45.4 ± 5.3 MPa after 1000 TST, indicating ~ 25% drop in shear strength, but still considerably higher than the reported values for Ag sintering [4][12]. It must also be noted that SiC is a very stiff material, with Young's modulus that is approximately 3 times that of Si [13]. Therefore, under high thermo-mechanical stress conditions, while Si shows some flexure, reducing the total strain in the die-attach layer, SiC due to its high stiffness results in the die-attach layer carrying the bulk of the strain from the test conditions. Therefore, it is important for the die-attach material to be able to carry the high strain.
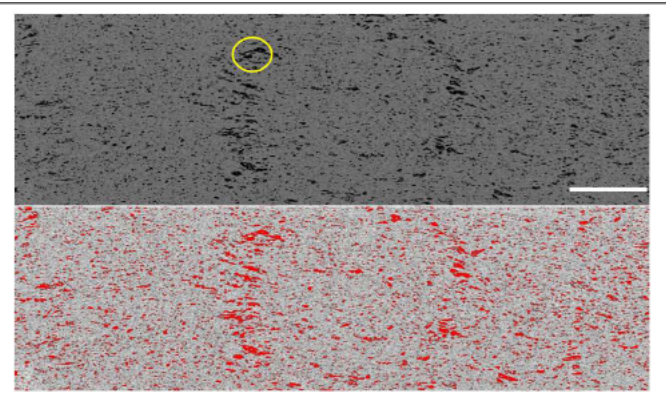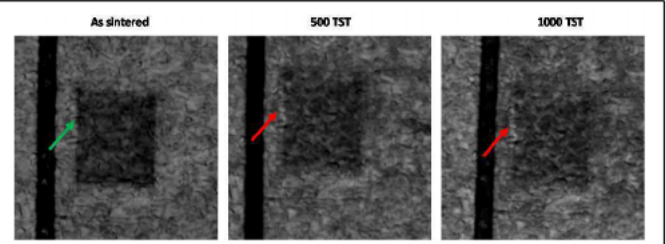
SAM analysis (backside scan) of the sintered interconnects is as shown in Fig. 7. A 50MHz transducer was used for the imaging. The TST was performed on the substrates as sintered, without encapsulating them. As is evident from the image, the first delamination was observed after 500 cycles along the left edge of the chip as shown by the red arrow. However, it is observed that this defect did not propagate or grow substantially in the next 500 cycles as can be seen in the 1000 TST image. But, although scanned under the same settings, the image quality is considerably compromised between the scans compared to the as sintered interconnect. The degradation within the AMB substrate as well as the impact of oxidation on AMB substrate impact the SAM scans. Further, as is evident from the images, the reflection of the substrate features (uniform white texture) could not be eliminated. A top side scan through the structure of the SiC chip did not yield the desired results due to the structuring on top of the chip and the corresponding reflections as can be seen in Fig. 8. Further, the dummy SiC devices used in this study had a polyimide coating on the top surface which degraded partially during sintering at 275°C for 5 min and also during thermal shock tests, further compromising the SAM top scan possibilities. Therefore, top scan SAM imaging was not pursued further.
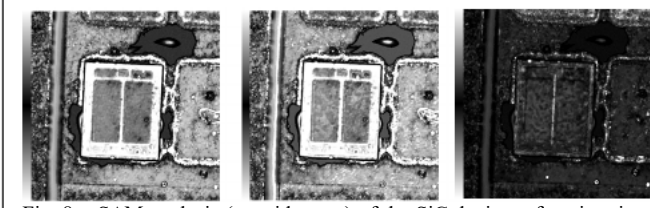
3

Fig. 8 – SAM analysis (top side scan) of the SiC devices after sintering, showing the impact of the structuring on the top surface of the chip and "stain" like features/spotting attributed to degradation of polyimide layer on die surface.

The subsequent cross-sectioning and SEM analysis of the sample showed interesting defect phenomena. The SEM image is shown in Fig. *9*. The delamination at the chip edge and the crack further into the interconnect is observed on the edge as marked with the red arrow (top image in Fig. *9*). On the opposite edge, consistent with the SAM image does not show any crack or delamination as shown by the green arrow. However, the SAM images do not reveal the defects at the substrate interface as observed in the bottom image of Fig. *9*, shown by the red arrow. Although the large void exists, the microstructure above the void is dense and uniformly sintered. With no such defect observed under the SAM, it could be a possibility that this is a defect during the sample preparation. However, the defect with the substrate metallization is clearly observed.
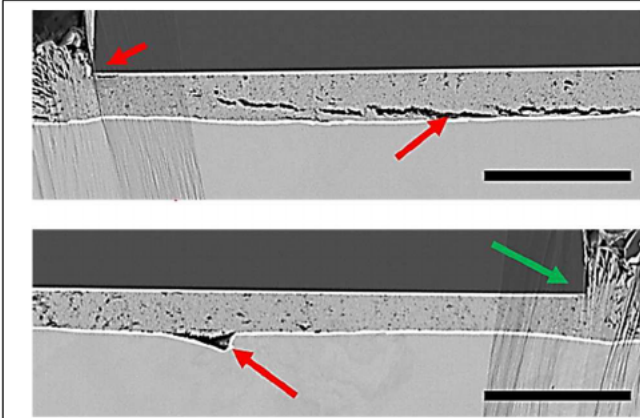

Fig. 9 – SEM analysis of Ar-ion beam milled cross-section of the sample after 1000 TST. Red arrows indicate the defects. Scale bar refers to 50 μm.
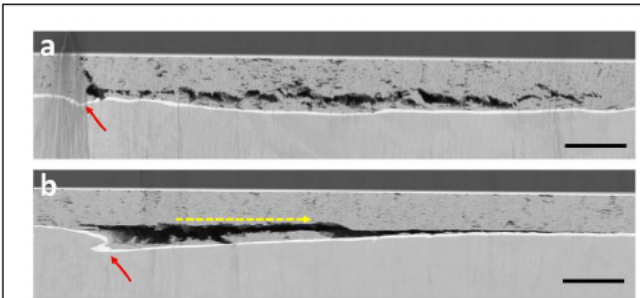

Fig. 10 – SEM images of the sintered microstructure showing substrate metallization defects and the corresponding cracks in the sintered microstructure. Scale bar refers to 20 μm.

In order to ascertain if this is a recurring effect, further samples from the same batch were cross-sections and the resulting analysis of the sintered microstructure among other samples indicated cracks to have predominantly initiated in areas where defects on substrates were also noticed. The origin of the cracks is consistent with the position of the defect on the substrate and hence localized. As a result, the typical edge to center crack propagation is not observed as reported earlier [14]. This can be possibly explained by the phenomena that the sintered interconnect is characterized by long pores which are nearly parallel to the interfaces as shown earlier in Fig 3. Therefore, the stress concentration formulation that gives the maximum stress at crack tip can be applied in terms of the long pores in case of the stacked Cu flakes Fig. *11*. This implies, the longer the pore and sharper the pore tip radius, higher the stress concentration. Therefore, the stress concentration at these locations is of several magnitude higher than the applied stress, thereby causing delamination by crack initiation and propagation. Therefore, while the stacking of the flakes over each other is beneficial for sintering, it is important to ensure a low porosity interconnect on sintering, i.e., a densely packed structure to avoid the above-mentioned phenomena.
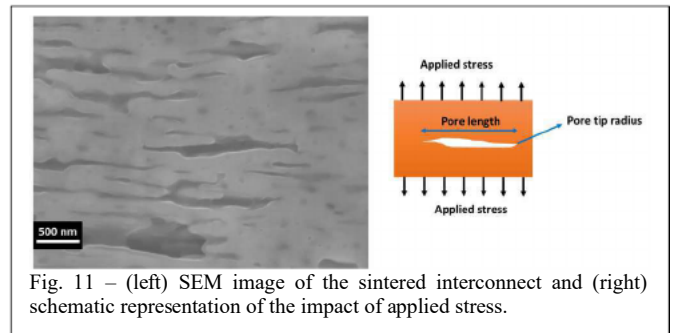

Fig. 11 – (left) SEM image of the sintered interconnect and (right) schematic representation of the impact of applied stress.

IV. CONCLUSIONS

Cu flakes-based sinter pastes provide a promising approach to die-attach bonding of SiC devices. The paste shows good workability, stencil printing and no bleed out. The compatibility to Ag metallization is also proven. The performance of the copper sinter paste is comparable with state of the art in Ag sintering. A thermal conductivity > 200 W/mK could be achieved, with as sintered interconnected resulting in shear strength over 60 MPa and an interconnect with < 10% porosity. Even after 1000 TST under harsh testing conditions of +175/-65°C, non-encapsulated, an average shear strength of 45 MPa is recorded. The unique stacking behavior of the flakes resulted in a dense and homogeneous interconnect with porosity < 10% (area %). Typical delamination failures as known from Ag sintering were not observed. Even with a thin BLT of ~12 μm, the sintered microstructure could withstand the extreme thermal shock conditions with SiC devices bonded onto AMB substrates. Localized cracks were observed which initiated at surface anomalies observed on the substrate. However, the typical failure mode with cracks initiation in the corners, leading to the center and complete delamination is not observed. In conclusion, the flakes-based paste offers a promising and reliable approach to die-attach bonding.

REFERENCES

[1]   J. Fabian, M. Hirz, and K. Krischan, "State of the Art and Future

4

Trends of Electric Drives and Power Electronics for Automotive Engineering," *SAE Int. J. Passeng. Cars - Electron. Electr. Syst.*, vol. 7, no. 1, pp. 293–303, 2014, doi: 10.4271/2014-01-1888.

[2] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 12, pp. 9226–9235, 2015, doi: 10.1007/s10854-015-3459-4.

[3] M. Schaal, M. Klingler, and B. Wunderle, "Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing," *2018 7th Electron. Syst. Technol. Conf.*, pp. 1–18.

[4] S. A. Paknejad and S. H. Mannan, "Review of silver nanoparticle based die attach materials for high power/temperature applications," *Microelectron. Reliab.*, vol. 70, pp. 1–11, Mar. 2017, doi: 10.1016/j.microrel.2017.01.010.

[5] Y. Tan, X. Li, G. Chen, Q. Gao, G.-Q. Lu, and X. Chen, "Effects of thermal aging on long-term reliability and failure modes of nano-silver sintered lap-shear joint," *Int. J. Adhes. Adhes.*, p. 102488, Nov. 2019, doi: 10.1016/j.ijadhadh.2019.102488.

[6] F. Qin *et al.*, "Crack Effect on the Equivalent Thermal Conductivity of Porously Sintered Silver," *J. Electron. Mater.*, vol. 49, no. 10, pp. 5994–6008, 2020, doi: 10.1007/s11664-020-08325-1.

[7] J. Dryzek, "Migration of vacancies in deformed silver studied by positron annihilation," *Mater. Sci. Forum*, vol. 255–257, pp. 533–535, 1997, doi: 10.4028/www.scientific.net/msf.255-257.533.

[8] Z. Zhang, C. Chen, A. Suetake, M.-C. Hsieh, and K. Suganuma, "Reliability of Ag Sinter-Joining Die Attach Under Harsh Thermal Cycling and Power Cycling Tests," *J. Electron. Mater.*, vol. 50, no. 12, pp. 6597–6606, Dec. 2021, doi: 10.1007/s11664-021-09221-y.

[9] K. Wakamoto, T. Otsuka, K. Nakahara, and T. Namazu, "Degradation Mechanism of Pressure-Assisted Sintered Silver by Thermal Shock Test," *Energies*, vol. 14, no. 17, p. 5532, Sep. 2021, doi: 10.3390/en14175532.

[10] Y. Zuo, A. Robador, M. Wickham, and S. H. Mannan, "Unraveling the complex oxidation effect in sintered Cu nanoparticle interconnects during high temperature aging," *Corros. Sci.*, vol. 209, no. July, p. 110713, Dec. 2022, doi: 10.1016/j.corsci.2022.110713.

[11] M. A. Ras *et al.*, "'LaTIMA' an innovative test stand for thermal and electrical characterization of highly conductive metals, die attach, and substrate materials," in *2015 21st International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, Sep. 2015, pp. 1–6. doi: 10.1109/THERMINIC.2015.7389630.

[12] T. F. Chen and K. S. Siow, "Comparing the mechanical and thermal-electrical properties of sintered copper (Cu) and sintered silver (Ag) joints," *J. Alloys Compd.*, vol. 866, p. 158783, Jun. 2021, doi: 10.1016/j.jallcom.2021.158783.

[13] K. Järrendahl and R. F. Davis, "Chapter 1 Materials Properties and Characterization of SiC," in *Semiconductors and Semimetals*, vol. 52, no. C, 1998, pp. 1–20. doi: 10.1016/S0080-8784(08)62843-4.

[14] S. K. Bhogaraju, M. Schmid, H. R. Kotadia, F. Conti, and G. Elger, "Highly reliable die-attach bonding with etched brass flakes," in *2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC)*, Sep. 2021, pp. 1–6. doi: 10.23919/EMPC53418.2021.9584967.

5