Study of spatial distortion in InP nanophotonic membranes on different carrier substrates

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***Abstract*—Electron Beam Lithography (EBL) metrology and least-square estimation of wafer-scale distortions is used to determine InP membrane deformation as a result of bonding to different substrate materials. First, the accuracy of EBL as a metrology tool for this particular application was assessed. Next, modelling of distortions was tested on unbonded InP wafers as a reference for extracting post-bonding distortions. Then we investigated the effect of substrate material choice on InP membrane deformation after bonding. We found residual expansion factors of 4.53±1, 312.4±1, and 317±1 ppm of the InP membrane bonded to InP, Si, and 3C-SiC carriers, respectively. For the SiO_2 carrier, the 3inch InP membrane split into smaller membranes to reduce the stress, highlighting the importance of substrate choice.**

Keywords—Adhesive bonding, metrology, 3D integration, overlay lithography, heterogeneous integration

I. Introduction

Nanophotonics has emerged as a groundbreaking field that enables the generation and guiding of light in sub-micron sized planar structures, with applications ranging from telecommunications to biomedical sensing [1]. A promising approach to nanophotonic design is the utilization of InP membranes that are bonded onto a substrate, like Silicon (Si), using some dielectric low refractive index material, such as SiO_2 or benzocyclobutene (BCB) [1]. This method is also purposed for vertical integration of photonics with electronic drivers for applications requiring high bandwidth or high integration density [2]. While membrane technology shows potential for the miniaturization of photonic integrated circuits (PICs), the fabrication of membrane devices poses challenges as a result of a complex process flow, involving double-side membrane processing before and after bonding. In particular, it becomes a challenge to perform wafer-scale alignment for overlay lithography before and after bonding due to non-uniform distortion of the membrane [3].

To gain quantitative insight into membrane distortions, one method employed is EBL metrology [3], [4]. This technique involves the utilization of a set of EBL markers that are patterned on the wafer as the initial step of the fabrication process to allow for overlay alignment. These are subsequently read by EBL after each process step such as adhesive bonding or hard mask deposition. Such processing steps can introduce distortions in the form of expansion, non-orthogonality, and higher-order distortions [5], [6]. By comparing the positions of markers found by EBL before and after processing, it is possible to determine the magnitude and direction of distortions and decompose it into systematic and non-systematic errors. This reveals how different physical processes influence the membrane expansion [5]. This method could be used as an in-line metrology tool during fabrication of nanophotonics, and it also allows for guiding future work to improve overlay lithography using industrial tools for membrane photonics [4], [7].

In this paper, we analyzed the influence of the EBL tool's beam current and beam drift on the writing and reading positional accuracy of markers. We used a 6-parameter model to fit the distortions and quantify systematic and non-systematic errors. This model corrects for in-plane translation, rotation, asymmetric scaling, and non-orthogonality on the wafer scale. We first validated the possibility to use the model with InP wafers before bonding. Then we applied the model to investigate how bonding parameters can influence membrane distortion.

For the effect of adhesive bonding on membrane distortion, the bonding is carried out at 280°C. So we investigated bonding a 300nm-thick InP membrane to different substrates to vary the coefficient of thermal expansion (CTE) mismatch between the membrane and the carrier substrate. We fixed the BCB thickness at 2µm and chose InP, Si, 3C-SiC (SiC), and Pyrex glass (SiO_2) carrier substrates to achieve a wide range of CTE mismatch of 0 to 4.27×10^{-6}/°C, as will be discussed later on. We observed that the CTE mismatch, *i.e.* choice of substrate, plays a crucial role on membrane expansion, namely scaling. Moreover, our findings suggest that such deformations are dynamic and can be further reduced by extra fabrication steps or tailored bonding parameters.

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II. Experimental Details

The study was conducted on 3" wafers. A simplified process flow is shown in Fig.1. Herein, we used a dedicated epitaxial stack on InP wafers and bonded it to different substrates to assess the effect of substrate carrier type on membrane distortion. The chosen substrates are: InP with identical CTE to the membrane of 4.75×10^{-6}/°C [8], Si and 3C-SiC with CTE of 2.55×10^{-6}/°C [9] and 2.77×10^{-6}/°C [10], and finally Pyrex glass with low CTE of 0.48×10^{-6}/°C [11]. To fabricate overlay markers, we grew a basic epitaxial stack on InP consisting of 300 nm InGaAs etch stop layer and 300 nm InP used as the membrane for device fabrication.

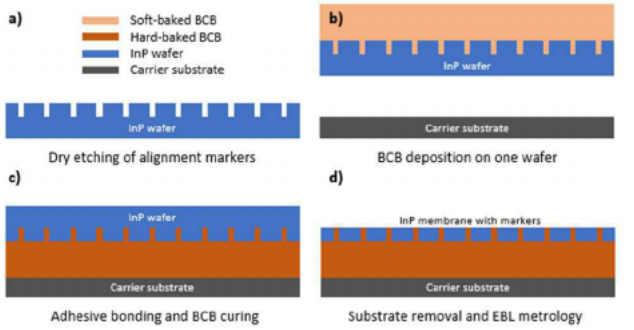

Fig. 1. Simplified illustration of the general process flow used in this study

We begin marker fabrication by depositing a SiN hard mask and patterning it with EBL using a positive resist. The pattern is then transferred to the hard mask with RIE etching, and subsequently to the InP wafer using ICP RIE plasma ensuring an etch depth of 450nm (Fig.1.a). Next in Fig.1.b, We prepare the InP wafer by depositing SiO_2. We then load it into EBL and read the markers. After that, we coat a thin layer of AP3000 for better adhesion to BCB and follow it with coating a 2 µm-thick BCB and evaporation of solvents. The carrier substrate is also prepared by depositing the same thickness of SiO_2 followed by coating with AP3000. The substrates are then aligned using the orientation of the major flats and locked in a cassette holder, which we load into EVG bonder for bonding. This operation is carried out at 280°C for 1h. We use a low ramp-up rate of 5 °C/min and 700N of force. During bonding, the temperatures of the top and bottom parts of the bonder are controlled separately within 0.1°C accuracy. Bonding results in full crosslinking of BCB, turning it to a solid dielectric layer that permanently joins the two substrates (Fig1.c). We note that the BCB thickness non-uniformity is below 5% before bonding, but it can increase after bonding because of BCB reflow before full-crosslinking [12]. After bonding, the bulk substrate and etch-stop layers are wet etched. For the InP substrate carrier case, we use protective multi-coatings to preserve the carrier during wet etching of the other InP wafer, and these are removed afterwards. After this stage, the markers are visible and ready for EBL reading from the backside(Fig1.d).

In this study, we use a Raith EBPG5150 EBL system. Both pattern writing and reading require placing the InP substrate into a 3" holder. For this, the substrate is clamped into the holder using three pins from the top side and pushed from the backside by the holder's backplate using a spring mechanism. Here, the substrate's bow is not fully neutralized. The locations of the 3 pins are shown in Fig.2.b. After loading the holder and reaching a vacuum level of ~10^{-7} mbar, marker reading or writing is carried out. We use square markers with an area of 20×20 µm^2 for marker fabrication with our system. The markers are uniformly distributed across the entire 3" wafer. We designed 3 maps on the same wafer with different marker pitches to investigate the impact of the spatial resolution on our analysis. The chosen pitches are 1.25, 2.5, and 5 mm in the (x,y) directions, where x and y are the directions perpendicular and parallel to the major flat, respectively. A beam current of 100 nA was chosen to ensure fast writing of the markers.

For marker reading, EBL logs the design and absolute positions of found markers. These are extracted and fitted using a wafer-scale 6-parameter model based on the least-squares estimation method. More details on the model are discussed next. The fitted maps can either be pre-bonding or post-bonding maps based on the desired information to be extracted. Experimentally, we explored a beam currents range of 5-190nA and investigated its effect on the residual errors. The effect of drift was also investigated as it can be a major source of reading errors [13].

For modeling our results, we used a 6-parameter model to correct for various systematic distortions of the studied maps. The model transforms given (x,y) coordinates of a map to new coordinates (x_{opt},y_{opt}) according to the following equations [5]:

$$x_{opt} = x.\cos(P_1) - y.\sin(P_1) + P_2 + x.(1+P_4) + y.\tan(P_6) \quad (1)$$

$$y_{opt} = x.\sin(P_1) + y.\cos(P_1) + P_3 + x.(1+P_5) + x.\tan(P_6) \quad (2)$$

Here, P_1 is the rotation in (rad). P_2 and P_3 are the translations in the x- and y-direction in (µm) perpendicular and parallel to the flat, respectively. P_4 and P_5 are the scaling factors in parts-per-million (ppm) in x- and y-directions, respectively. P_6 is the non-orthogonality factor in (rad).

Optimal values of P_1-P_6 are obtained using a least-squares estimation method to match (x_{opt},y_{opt}) with a given (x_0,y_0). The given coordinates can be the design coordinates or coordinates read by EBL at a certain stage during fabrication. In the post-bonding case, the coordinates are flipped in the y-direction to match pre-bond observed coordinates, *i.e.* we match (x,-y) with pre-bond (x_0,y_0). For optimal results, we use a null initial guess for all parameters and then fit the data with a suitable algorithm for minimization. Throughout this study, we use the standard deviation (StDev) of residual errors (x_{opt}- x_0, y_{opt}-y_0) to assess the quality of the acquired results. Hence, to benchmark results, we first calculated with Eq.1 and Eq.2 how the StDev grows when each of the variables P_1-P_6 is varied individually. For this, we used wafer-scale marker positions that are identical to the ones used in our experiments dedicated to this study. We matched our modelling estimation errors using this information with experimental data revealing experimental systematic errors from EBL, namely from beam drift. Given that translation and rotation depend on the initial wafer position and are related to wafer placement in the EBL holder, we do not include P_1- P_3 in our results. For P_4 and P_5 the errors are within ±1ppm, and for P_6 it is within $\pm2\times10^{-6}$rad.

III. RESULTS AND DISCUSSION

A. *Evaluation of the effect of EBL settings and model accuracy on residual errors*

In this section, we investigate the effect of chosen EBL settings during marker reading/writing on the standard deviation. We also test our model on unbonded wafers. The goal is to decouple systematic and non-systematic errors before bonding to ensure the accuracy of results in this paper. In metrology, the main non-systematic EBL errors arise from beam drift and the used beam current. Beam drift is caused by temperature fluctuations <0.1°C of the chamber, and it affects both marker fabrication and reading [13]. It can particularly affect results for large writing areas or as a result of temperature instability of the holder, for instance during loading. Beam drift is corrected periodically by EBL each 1h in this study, and these corrections if present are extracted and subtracted from results in this paper for better modelling accuracy. Also, increasing the beam current leads to a higher beam diameter, which affects marker reading time, image contrast, and edge sharpness, thereby affecting the registered marker positions.

First, we assessed the effect of beam drift and current on marker fabrication and reading without using the model. For that, we used 100 wafer-scale markers spanning the full wafers. These required a fabrication time of 10 minutes to expose. An identical map with a 675µm x-shift was also fabricated and designed to take 60 minutes to expose. The maps were then read multiple times with multiple beam currents without loading/unloading the holder from the main chamber. Next, marker positions were extracted from different reading times and subtracted from each other. We calculated the StDev from the residuals and the results are shown in Fig.2.a. The residuals map extracted using 5nA beam is shown in Fig2.b. The standard deviation is below 5nm for beam currents below 100 nA and around 8.5 nm for a beam current of 190 nA. This could be caused by the increase in beam diameter that lowers the accuracy of observed marker positions, especially since the effect of charging is likely mitigated by the high pitch between markers. The increase in markers' exposure time from 10 to 60 minutes during fabrication does not increase the StDev above 1nm. The map in Fig.2.b shows the movement as vector directions and lengths. The displacement appear to be locally defined, with no clear global wafer-level trends.

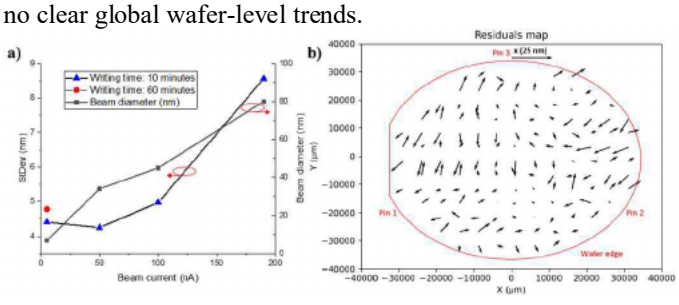

Fig. 2. a) Standard deviation of residuals and beam diameter *vs* beam current. b) Residuals map showing the positional differences between markers read at two different times highlighting the effect of drift.

Next, we assessed the accuracy of our 6-paramter model based on these findings. Here, we compared the observed marker positions with the designed positions and extracted the six distortion parameters based on Eq.1 and Eq.2. The fitted map using 5nA beam and averaged for >10 datapoints per marker is shown in Fig.3. The inset of Fig.3 shows bell plots of residuals from averaged data *vs* different beam currents. Here, we observe that using smaller beam currents yield slightly higher accuracy based on lower residuals. However, the overall standard deviation values are similar. Moreover, the obtained values for P_4-P_5 for different currents are all within ±1 ppm. For non-orthogonality all obtained values of P_6 are below 1.10^{-6} Rad lower than the error range, indicating that the effect of non-orthogonality is minimal. Based on this, and to ensure the highest accuracy of our marker reading, we use 5nA beam and averaged data per marker in the rest of the study.

For the map in Fig.3, the largest vectors lie on the edges of the wafer. We note that the pattern near pin 1 is consistent in all of our extracted maps, suggesting that such deformations are affected by the metal pins used to secure the wafer on the holder. Since the wafer was not yet bonded, the overall observed distortions might come from the effect of removing the SiN hard mask used initially to fabricate the markers. Indeed, residual errors in the order of tens of nm can be the result of localized wafer shape changes induced by residual stress from thin films [14]. Such distortions would require both localized and wafer-scale correction models to account for the full distortion, for instance with a 10-parameter model based on the used lithography tool, depending on the neutralization of the wafer bow by the holder [14]. It also might be possible to better model the patterns near the edge with only wafer-scale corrections by using higher-order corrections like cubic distortion. However, as will be shown in the next sections, the post-bonding distortions are mainly dominated by scale (P_4 and P_5), so we do not pursue this option.

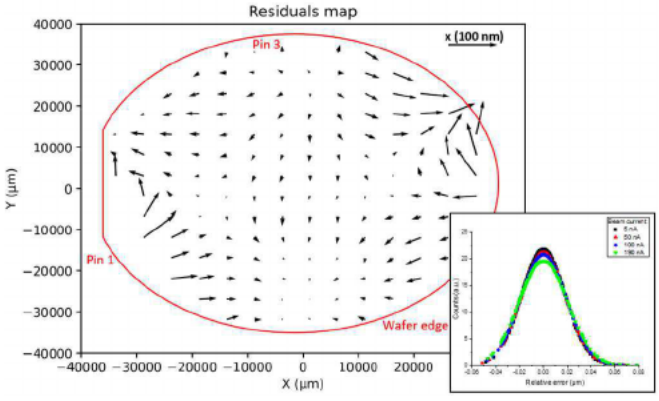

Fig. 3. Residuals map showing the difference between design and observed marker coordinates after correction of the data with fitted model parameters. Inset: bell plots of residuals from fitted maps for different beam currents

B. *Effect of substrate choice on post-bonding membrane distortion:*

The choice of the substrate directly affects the CTE mismatch between the InP wafer and the carrier substrate during bonding. It also affects the InP membrane after substrate removal in a similar manner. For isotropic materials in CTE, the equation to describe ideal values for scaling based on CTE is given as follows:

$$P = \Delta T . \Delta \alpha \qquad (3)$$

Where P is the scaling coefficient, ΔT is the difference between bonding and room temperatures, and Δα is the CTE mismatch. Using Eq.3, we first calculated the theoretical thermal expansion values of the InP membrane on different substrates for bonding temperatures of 250 and 280°C, which are the most often used in the literature [15]. We also plotted the average of P_4 and P_5 extracted by our model from our dedicated experiments. Results are shown in Fig.4.a. We note that the CTE of InP is higher than the used carrier substrates here, so the scaling is limited to expansion in this study as InP expands more than other substrates here by the effect of temperature.

For the InP carrier case, the CTE mismatch is 0. However, an average scaling factor of 4.53±1 ppm was found from our experiment. This indicates the existence of some expansion in the InP membrane. It is likely caused by the partial relaxation of residual stresses that might be present in the BCB, given that the temperature of both InP wafers is the same during bonding within 0.1°C. This is because the thermal expansion of BCB as a polymer is an order of magnitude higher than that of InP or other semiconductors, causing the accumulation of residual stresses in the BCB layer. The latter might affect the InP membrane more than the InP substrate underneath, since the substrate thickness is three orders of magnitude thicker than the membrane.

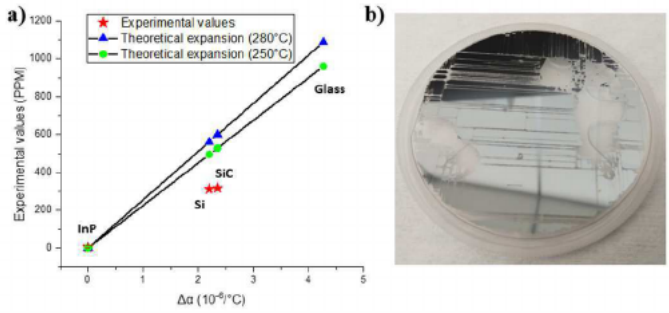

Fig. 4. a): Theoretical and experimental values of the InP membrane expansion *vs* CTE mismatch, b) image of an InP bonded membrane on top of a SiO_2 substrate before InGaAs etch-stop removal showing InP memebrane splitting

The measured scaling (expansion) factors on Si and SiC wafers are 312.4±1 and 317±1 ppm, respectively. These values are lower by 248.6±1 and 282.2±1 ppm from the expected expansion values for Si and SiC, respectively. Hence this part of the expansion could have been released after bonding as a residual stress by increasing the wafer bow. Based on this, we decompose the membrane expansion into two parts. We refer to the experimentally obtained values of P_4 and P_5 as residual expansion, while the difference between experimental and theoretical values is referred to as released expansion. It might be that the released expansion is only possible by the relatively higher elastic deformation of BCB compared to the InP semiconductor membrane on top [15]. Moreover, in all of our measurements P_4 is slightly higher than P_5. This difference is 11.22±2 ppm for Si, 7.19±2 ppm for SiC, and 5.14±2 ppm for InP carrier substrates. This might point to the existence of an anisotropic behavior in CTE or the mechanical properties of the substrate carriers. Another possibility to explain why the experimental values are much lower than theoretical values is that as the temperature ramps up during bonding, the crosslinking of BCB increases across the two wafers. A point where BCB permanently fastens the two wafers could then occur before full crosslinking. A calculation of this temperature based on experimental values yields a temperature of 170°C. The degree of crosslinking at this temperature is below 50% during the slow ramp-up [15]. Therefore, this possibility if present might only coexist with the aforementioned mechanism. This will be further investigated to determine if the membrane deformation is permanent or dynamic and can be further relieved.

For bonding to the SiO_2 wafer, an image of the bonding result is shown in Fig.4.b. Apart from the large defects where the membrane is detached, vertical and horizontal lines are apparent. These defects are only visible after substrate removal. Theoretically, the membrane is expected to expand by 1088.9 ppm given the large CTE mismatch of 4.27×10^{-6}/°C. The presence of such lines where the InP membrane split indicates that the released expansion is higher than the values previously found for Si as it required plastic deformation of the membrane. Although it is not possible to determine the values of residual expansion in this case, *i.e.* P_4 and P_5, the released expansion is higher than the highest found value in this study. Hence, the residual expansion of the InP membrane after breaking is lower than 806.7±1 ppm. Consequently, a more tailored bonding process is needed to reduce the risk of membrane breaking.

IV. Conclusions

We used EBL as a metrology tool to determine InP membrane deformation as a result of bonding to different substrates. We found residual expansion factors of 4.53±1, 312.4±1, and 317±1 ppm of the InP membrane to InP, Si, and SiC carriers, respectively. For the SiO_2 carrier, the 3" InP membrane split into smaller membranes to further release the stress as the CTE mismatch is high. These results highlight the importance of substrate choice and/or tailoring the bonding parameters for improved bonding yield and lower risks during post-bonding processing.

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