WLCSP Fully Protected Fan-In Reliability

Doug Hackler, Ed Prack PhD*
American Semiconductor
6987 W. Targee St.
Boise, ID83709USA
Ph: 208-336-2773; Fax: 208-336-2752
DougHackler@americansemi.com
*MASIP LLC

Abstract

A strong supply chain requires higher performance and lower cost processes. DCA conventionally referred to as WLCSP has been used for low density devices, however for higher density devices, reliability concerns have emerged. Six-side protected, aka "6S or fully protected", CSP is a rapidly growing market. Fully protected CSP was first implemented with processes such as M-series utilizing FO. These processes require costly and complex die reconstitution, expensive tapes, molding, and other operations. These steps can be eliminated in a P-WLCSP process to provide the cost-effective high reliability 6S format needed for high-performance higher pin count and/or thin silicon chips. American Semiconductor's Semiconductor-on-Polymer (SoP) 300mm SoP-TM, a P-WLCSP process, is an advanced packaging process optimized for protected CSP, fan-in, and chiplets. Protected FI process innovations can improve performance in power devices, RF switches, photonic IC (PIC), die stacking and thin board applications. The P-WLCSP process incorporates the best of DCA (simplicity) and FO (protection) while incorporating advanced manufacturing processes to lower cost and improve performance. This paper builds on the SoP-TM process release announced at the 2023 Device Packaging Conference earlier this year with the addition of reliability characterization beyond first silicon data for electrical test chips. Reliability data such as accelerated stress tests, die strength, operating lifetime and thermal testing are key areas of investigation for the new P-WLCSP technology that will be presented. The presentation will also include and update for ultra-thin device reliability test methods under consideration for new NIST standards.

Key words

CSP, Fan-In, Flexible, Protected, P-WLCSP, Semiconductor-on-Polymer, SoP, Thin

I. Introduction

A strong supply chain requires higher performance and lower cost processes. DCA and CSP reliability concerns have emerged as devices have become thinner. Six-side protected, aka "6S or fully protected", CSP is a rapidly growing market. Fully protected CSP was first implemented with processes such as M-series utilizing FO.[1,2] These processes require costly and complex die reconstitution, expensive tapes, molding, and other operations that can be avoided for non-fan-out devices to provide the cost-effective high reliability 6S format needed for high-performance higher pin count and/or thin silicon chips.[3] American Semiconductor's Semiconductor-on-Polymer (SoP) 300mm SoP-TM, a P-WLCSP process, is an advanced packaging process optimized for protected CSP, fan-in (FI), and chiplets. The low-cost process can also be supplemented with molding or similar materials to produce DCA, QFN and related conventional form factor packages at lower cost. Protected FI process innovations can also improve performance in power devices, RF switches, photonic IC (PIC), glass-lidded imagers, die stacking and thin board applications. The P-WLCSP process incorporates the best of CSP (simplicity) and FO (protection) while incorporating advanced manufacturing processes to lower cost and improve performance.

This year, reliability characterization beyond first silicon data for electrical test chips can be reported.[4] Reliability data such as low and high temperature humidity bias testing, die strength can be reported for a commercial IC. The Analog Devices ADA4505 has been packaged in SoP W-WLCSP for evaluation. Operating lifetime and thermal testing are key areas of investigation for the new P-WLCSP technology discussed at last year's IMAPS Symposium.[5]

The ADA4505 used for SoP P-WLCSP testing is a single

micropower amplifier featuring rail-to-rail input and output swings while operating from a single 1.8 V to 5 V power supply or from dual ±0.9 V to ±2.5 V power supplies. This amplifier offers excellent PSRR and CMRR performance and very low bias current, while operating with a supply current of less than 10 µA per amplifier. This combination of features makes the ADA4505 amplifier a popular choice for battery-powered applications because they minimize errors due to power supply voltage variations over the lifetime of the battery and maintain high CMRR even for a rail-to-rail op amp.[6] The high-performance analog capability of this device was used to determine reliability and device performance effects associated with ultra-thin device packaging and device deformation.

Initial reliability evaluations of the SoP packaged ADA4505 included high and low temperature lifetime, temperature humidity bias accelerated stress testing and die strength. Die strength of ultra-thin CSP ICs was performed using radius of curvature (RoC) testing, a method developed for characterization of ultra-thin and deformable chips. The augmentation of traditional test methods that comprehend effects of chip deformations that are becoming increasingly frequent in assembly and applications was included in testing. Test methods presented here are under development for future SEMI standards and will be reviewed by NIST. The ADA4505 evaluation builds on the SoP-TM test chip results presented at the 2023 Device Packaging Conference earlier this year.

II. SoP P-WLCSP Process

SoP-TM is the newest P-WLCSP (protected-wafer-level-chip-scale-package) process and the first process optimized for 6s protection (encasement on all 6 die sides-see Figure 1) without the use of reconstitution steps.

Figure 1- SoP-TM SoP 6S P-WLCSP

Drivers for adoption of new IC packaging approaches address specific needs and provide a path to lower cost with high performance. Traditionally, major IC packaging changes have taken ~15 years from inception to HVM (High Volume Manufacturing). SoP provides unique capability for thin and flexible devices addressing the specific needs of thin device applications. It also provides new paths to traditional and advanced IC packaging. A holistic approach as described by MASIP [7-8] was used to address key cost drivers by incorporating learning from various technology silos outside of traditional packaging. Two benefits to SoP are lower cost via processing and low-cost substrates for plastic IC packaging advantages.

The process eliminates pre-packaging wafer prep steps and eliminates taping, grinding, dicing, and reconstitution to reduce process cost and complexity. The process includes maskless PSB using adaptive processing and maskless RDL steps. Adaptive processing advances low cost via processing by eliminating photosensitive materials, masks and wet processing for develop and clean steps in the traditional packaging. Standard wafer level processing for bumps, pillars and/or RDL can be used. Only 1 thinning step is required and is implemented with a unique dry release temporary adhesive that eliminates chemical process for debonding. A low-cost recyclable silicon carrier wafer is used. Overmold processing is eliminated with application of polyimide on all 6 sided for CSP packaging.

A. Broader Application SoP processing

SoP provides an immediate advantage for CSP, but SoP IC packaging applications are not limited to CSP. ASI supplies SoP in a flex package (SoP die on flexible substrate) for specific applications, see Figure 2. These packages have a similar pad layout to standard QFN plastic IC packages.

The largest segment of the IC packaging is plastic packages, which include molded leadframe and substrate packages. Flex substrates are an integral part of the cost effective plastic IC package substrate roadmap. Methods of applying SoP to plastic IC packages include direct attach of SoP die/flex SoP to leadframes or substrates and molding into conventional form factor plastic packages. This allows application of SoP-TM cost and reliability benefits tot plastic packages with conventional form factors such as QFN, MLP, PBGA and similar plastic IC packages. For thin/flexible applications direct flex SoP packages could be used with standard bondpad layouts.

Advanced packaging applications of SoP that take advantage of its ultra small form factor include multi die form factor equivalent plastic package amd FO embedding. SoP plus mold to enable multi-die stacking while maintaining lower form factors, see Figure 3. 5-sided SoP derivative processes can be applied for thermal solutions beyond alternatives such as ESPP[9] (exposed silicon plastic package). Embedded SoP die similar to FO layers and multiple chip-on-flex substrate and/or stacked SoP die are emerging rapidly for new applications.

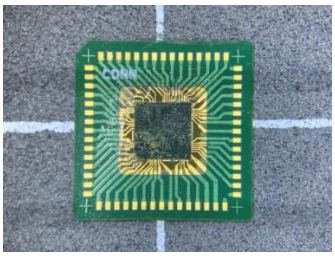

Figure 2 - Flip-chip on flex hybrid FO module

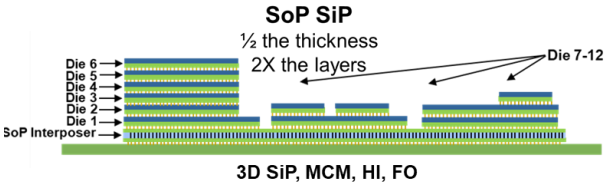

Figure 3 Multi-die Assembly enabled by ultra-thin devices and Double-Sided SoP Interposer (concept)

Hybrid integration with SoP, especially when combined with chip-on-flex, enables new options for IC packaging. The leading edge of the adoption of SoP technology is for new medical devices that require thin and/or flexible formats. Implanted devices, ultra-small sensor assemblies and smart medical labelization are relying on SoP advanced packaging capability, see Figure 4.

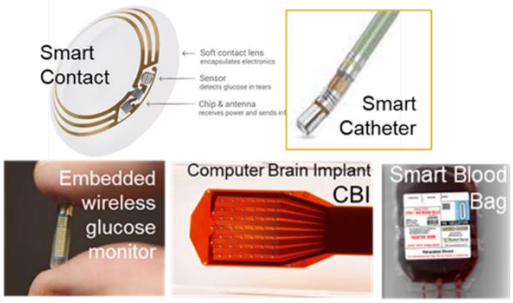

Figure 4 - Next Generation Medical Devices relying on Advanced Packaging

B. Semiconductor-on-Polymer (SoP) Reliability

The two most significant hurdles for any new technology to overcome are cost and reliability. Multiple papers have been presented documenting cost advantages for SoP. Reliability has been reported for SoP test chips. This year, silicon IC reliability testing has progressed with the evaluation of SoP packaged op amps. The ADA4505 high-performance op amp was selected for SoP evaluations based on the analog technology capability to show sensitivity of performance related to packaging. ADA4505 reliability testing consisted of Low Temperature Testing, Low Temperature Humidity Testing, High Temperature Testing, High Temperature Humidity Testing and Static RoC Testing. Environmental test set-ups included:

Low Temperature Test:
168 hours @ -25C, 1atm, n/a RH
2.5mV DC bias applied between VDD and VSS
Low Humidity Test
168 hours @ STP (22C/1atm), <10%RH
2.5mV DC bias applied between VDD and VSS
High Temperature Test
168 hours @ 125C, 1atm, n/a RH
2.5mV DC bias applied between VDD and VSS
High Humidity Test
168 hours @ STP (22C/1atm), 90%RH
2.5mV DC bias applied between VDD and VSS

Devices under test (DUT) were assembled on cu-on-PI test coupons for connection to test boards as shown in Figure 5. Current test chambers are not capable of supporting dynamic deformations of DUTs during environmental exposure. This is typical of the issues motivating development of new test capabilities for evaluations of thin-devices that deform with applied stresses in new and emerging applications.

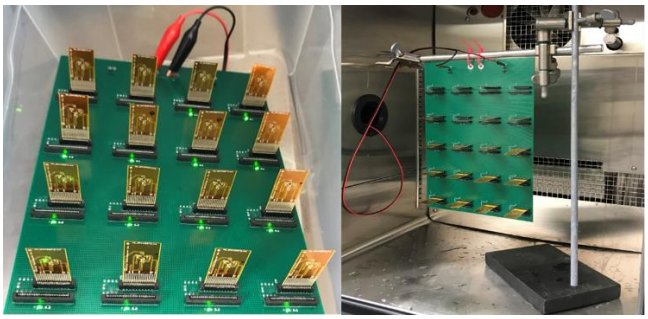

Figure 5 - SoP DUT on coupon on test board in environmental chamber

Data was collected pre- and post-environment exposure, with midpoint screening. Post-assembly testing included full electrical characterization after coupon assembly. Environmental Chamber was evaluated after first 84 hours at controlled environmental conditions with functional verification of 30mV p-p Gain. 168 hours at controlled environmental conditions included final test with full electrical characterization. At midpoint testing, all coupons passed functionality test with 1 coupon showing increased gain. At final test, no test showed any consistent shift in data compared to post-assembly results. 2 coupons failed during final testing with failure mode indicating handling damage. Environmental test results indicate all environmental exposures had no significant impact on the electrical performance of SoP packaged ADA4505 devices.

Radius of Curvature (RoC) die strength testing was completed for ADA4505 SoP-TM CSP using ASI TEST003. This static RoC test includes attachment of SoP chips to a polyimide coupon with adhesive and then bending the coupon over mandrels of specified radii. Samples were inspected for die cracking while coupons were bent and then rotated 90 degrees for orthogonal bend and inspection, see Figure 6 and 7.

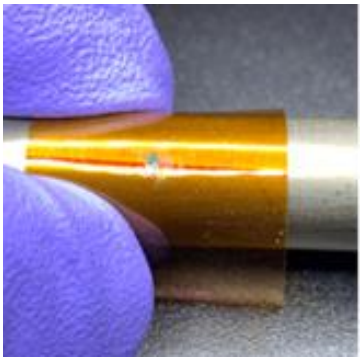

Figure 6 - ADA4505 on polyimide during TEST003 RoC Test

Radius of Curvature testing ranged from 20mm to 5mm. The results of the testing were compared to bare die. The robust performance of SoP advanced packaging was obvious. This is the enabling characteristic of SoP technology that provides the capability required for next generation thin-device applications.

	Process	DBG Thin Die					SoP-TM			SoP-TM		
	Device	Bare Silicon - Test Die					Blank Si - Test Die			AS_OPA4505P.fxd		
	Sidewall	Blade					Etch			Etch		
	Size (mm)	5					2			1.5		
	Si Thickness	100 um					12 um			10 um		
RoC	Tag ID / Bend Orientation	8A	8B	8C	8D	8E	7A	7B	7C	W3-C1	W3-C2	W3-C3
20mm	Perp	P	P	P	P	P	P	P	P			
	Orth	X	P	P	X	P	P	P	P			
15mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	P	X	X	P	P	P			
12mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
10mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
8mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
7mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
6mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
5mm	Perp	X	X	X	X	X	P	P	P	P	P	P
	Orth	X	X	X	X	X	P	P	P	P	P	P

Figure 7 - SoP Static RoC (Die Strength) Test Results

III. Conclusion

Advanced Packaging (AP) is not defined by the things it builds; Advanced Packaging is defined by how things are built. SoP provides an advanced packaging platform that can be used to support performance and cost improvements in current package formats as well as enabling the feasibility of new applications such as those common to advanced medical devices and flexible displays.

As with the adoption of all technology advancement, reliability must be characterized. New test methods are required for thin device technology, especially when devices are scaled to the point of sustaining physical deformation. American Semiconductor and Bayflex Solutions recently announce joint development supporting new SEMI Standards Development and the new SEMI Standards Committee received formal approved in September. Test methods for the new standard are being developed based on tests such as TEST003 initially demonstrated with AFRL support in 2016. The new tests and standards will include advanced test methods where device deformation can be done in situ during environmental exposure.

Acknowledgment

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