Automotive Grade WLCSP for Radar Applications

Nishant Lakhera, Burt Carpenter, Teck Beng Lau and Andrew J Mawer
NXP Semiconductors
6501 W William Cannon Drive
Austin, TX 78735, USA
Ph: 512-895-8534
Email: nishant.lakhera@nxp.com

Abstract
Wafer-Level Chip Scale Packages (WLCSPs) are becoming commonplace in the industry due to their small form factor. Applications include industrial and automotive which demand high reliability performance. Additionally, WLCSPs may be superior in some implementations to other package options for RF performance in the mmWave spectrum, which is desired for automotive radar application. In this study the industry's first auto grade 1 capable large WLCSP package. (~ 72 mm^2 body size, 18x15 BGA array, 0.5 mm pitch) will be presented. It will be demonstrated how extensive design enhancements, predictive simulations, careful process selection and assembly process optimization studies are required to develop a robust package solution.

Multiple assembly process experiments and corner studies were conducted to demonstrate robustness of WLCSP package solution to meet automotive grade quality and reliability requirements. Both component/unit level and board level reliability were evaluated as per AECQ100 standards. Robustness margins were confirmed through reliability testing as per AEC Q-100 standards.

Key words
automotive, WLCSP, chip scale package, radar, reliability

I. Introduction
Demand for more diverse applications and better performance in automotive and industrial electronics is growing astronomically [1]– [5]. The size of electrical components must shrink without sacrificing functionality, which makes Wafer-Level Chip Scale Packages (WLCSPs) an attractive solution. Wafer level packages provide superior RF performance and are a preferred choice for mmWave radar product applications. However, automotive and industrial applications require high component and board level reliability performance in severe environments, and WLCSP reliability is complex [6], [7]. As WLCSP package get mounted onto the printed circuit boards (PCB) the stress from mounting, handling and application of the product may directly transfer to the silicon due to the limited stress buffer package materials used in WLCSP by design (redistribution and repassivation layers). WLCSP packages rely on solder balls connecting the PCB to the package to relieve the strain. Hence, WLCSP packages by design have higher propensity of experiencing damage in the silicon backend of line (BEOL) or inter layer dielectric (ILD) layers. This failure mode becomes even more critical under automotive environment where the component and board level reliability requirements are much higher than consumer grade applications where WLCSP packages are more commonly used. WLCSP assembly uses fab-like assembly processes like photolithography to define repassivation opening/redistribution layer (RDL) patterns, descum etches to clean residues, sputter for seed layer deposition for RDL plating etc. which requires tight monitoring and process control to ensure a stable assembly process. Careful material selection, design and assembly process control is key to ensure a robust RDL via to aluminum (Al) pad interface to mitigate risk of via delamination.

Overall product and package co-design is a must to ensure electrical performance and mechanical reliability requirements can be met. Proper material selection, design and assembly process control can help mitigate the overall stress in the package and package-board assembly and mitigate risk of both via delamination and BEOL damage, which is the focus of the work presented in this paper. Component and board level reliability assessment was performed on the WLCSP package to validate meeting automotive requirements.

II. Discussion

A. Product and Package Design

WLCSP package presented in this work supports a radar product which includes a fully integrated radar front end for mid-range (emergency braking) and long range (adaptive cruise control) applications at 77-81GHz with high range resolution of less than 8 cm. The package is WLCSP with body size ~ 72 sq mm and BGA array of 18x18 at 0.5mm pitch. Representative top and bottom view images of the WLCSP package is shown in Fig.1. The package had high RDL density >75% which was optimized for mechanical reliability and electrical performance. BGA ball pattern was also optimized for mechanical reliability and PCB routability. WLCSP package materials and design features like RDL via sizes, re-passivation material thickness, RDL thickness, UBM size etc. were carefully selected to meet product requirements.

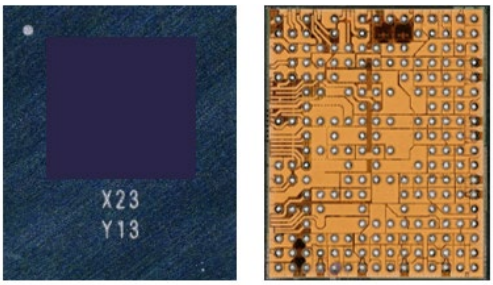


Fig.1: Top view (left) and bottom view (right) of WLCSP radar package.

B. Mechanical Simulations

Standalone WLCSP package model was constructed to assess the stress at RDL via to Al pad interface as shown in Fig.2. Full size 3D package model was constructed including the RDL design with UBM and vias. Consideration of assembly process history was also made in the simulations.

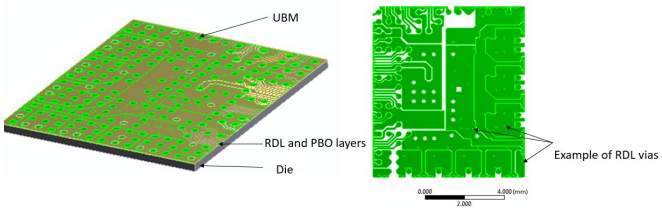


Fig.2: Full size 3D package model with resolved RDL.

Equivalent von-Mises stress contour was simulated at peak solder reflow temperature of 250C; results are shown in Fig. 3. Equivalent stress was well below 50MPa at the RDL vias indicating low risk of RDL via delamination related issue due to design of package and materials chosen.

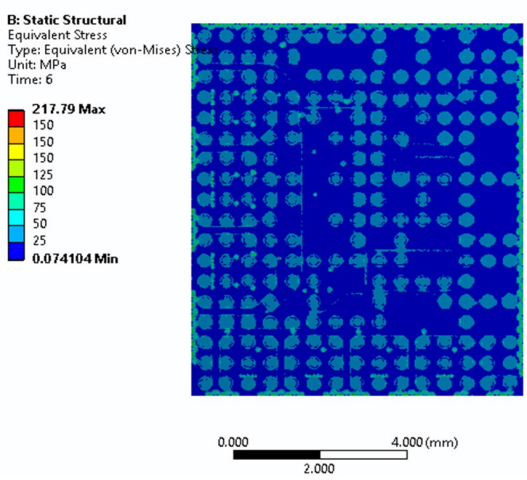


Fig.3: RDL via stress at peak solder reflow temperature.

Rigorous finite element mechanical simulations were also performed to assess package-PCB interactions with focus on BEOL integrity. Global-local modeling methodology was used as shown in Fig.4. Detailed mechanical models resolving the silicon BEOL artwork were developed to assess the impact of BEOL design and package-board interaction on BEOL integrity.

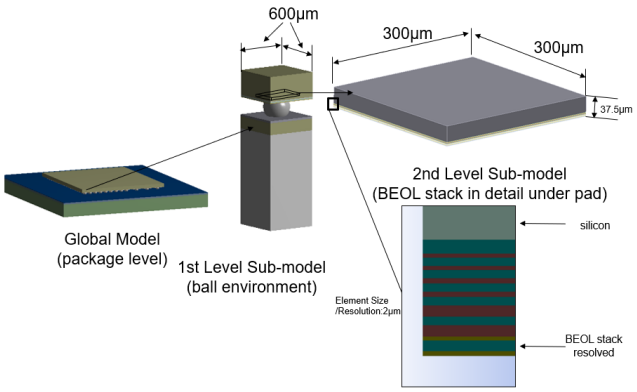


Fig.4: Global-local finite element modeling approach used.

Fig.5 shows the maximum principal stress under the solder balls simulated from the global model with and without underfill between the package and the PCB. Maximum stress is below 50MPa for both cases. Fig.5a shows that highest stress did not occur under the outermost corner spheres but some rows inwards and predominantly in the area with lower sphere density. Fig. 5b shows that application of board level underfill significantly reduced the stress under the solder balls. Stresses become compressive in nature, hence, reducing the risk of BEOL damage which is predominantly driving by tensile peel and shear stresses.

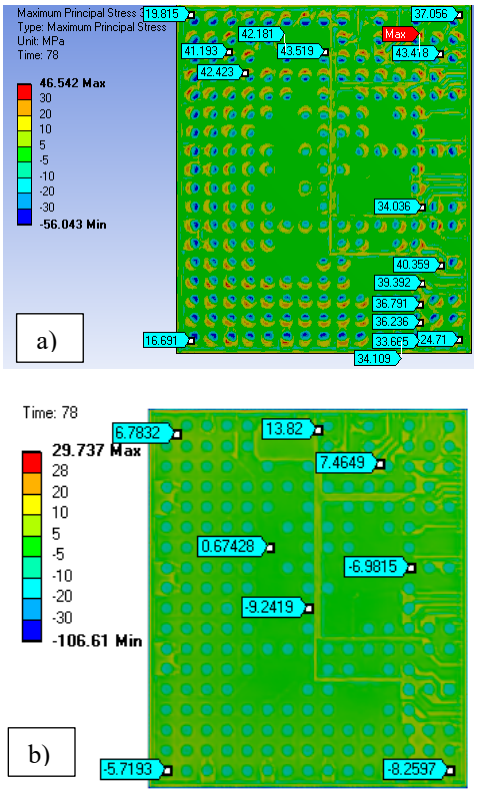


Fig.5: Maximum principal stress under BGA balls with a) no underfill between package and PCB and b) with underfill between package and PCB.

Fig.6 shows the stress in the ILD layer 1 of BEOL which also was below 50 MPa for case with board level underfill, much lower than what is known to cause issues from the past work. Results show that max stress is caused by the RDL design and not introduced by the spheres, thanks to presence of underfill. Hence, the risk of ILD damage which is typically caused by spheres pulling on the BEOL stack underneath is mitigated.

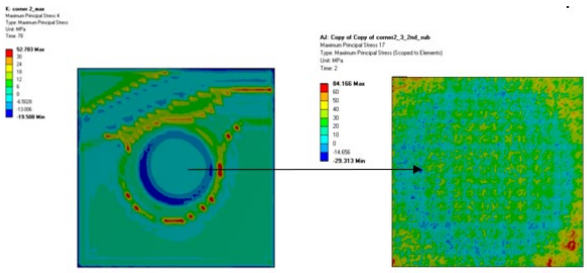


Fig.6: Stress in ILD layer 1 of the die.

C. Assembly Process Windowing

WLCSP assembly process critical parameters were windowed to confirm robustness. Key metrics windowed included but not limited to were re-passivation material thickness and photolithography parameters, clean descum parameters, plating parameters etc. Responses checked include via sizes, layer thickness, ball shear etc. Some of the results are shown in the subsequent figures. Fig.7 shows the repassivation via after developing and cure using coating thickness and photolithography corner conditions. Via sizes were confirmed to be within spec with good process capability and no dielectric repassivation to Al surface delamination was noted after cure as shown in Fig 8.

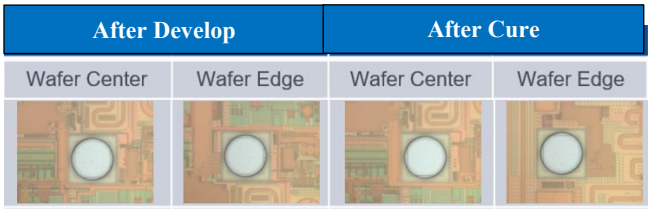


Fig.7: Repassivation via after developing and after cure.

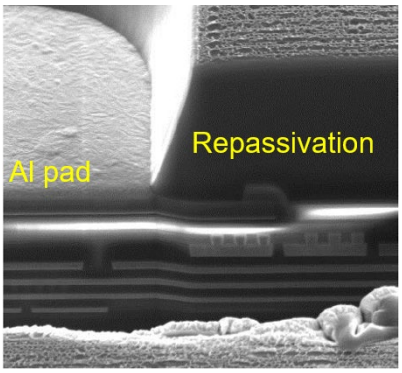
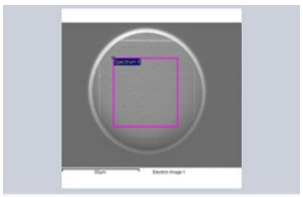


Fig.8: Al pad to repassivation interface.

Surface analysis post photolithography was performed on the Al pad surface within the via to check for presence of any halogens. EDX analysis did not reveal any halogens on the Al pad surface, as shown in Fig. 9, indicating a clean Al pad to receive the RDL layer.



Element	Weight%
Al K	95.22
Cu K	4.78
Totals	100.00

Fig.9: EDX analysis results confirmed no halogens on pad.

Copper RDL thickness after plating and after etching were also assessed under corner process conditions, results are shown in Fig.10. RDL thickness was within spec with good process capability. Ball shear testing was also performed on corner samples to validate the strength of the BGA ball interconnection to the RDL layers. Results successfully met

the criteria as shown in Fig.11.

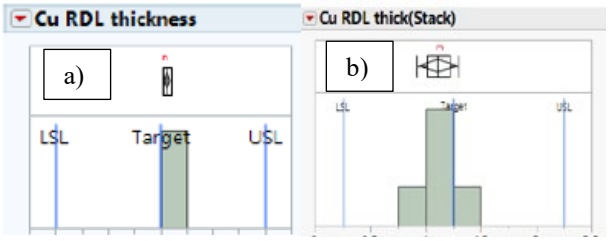


Fig.10: a) RDL thickness after plating, and b) RDL thickness after etching.

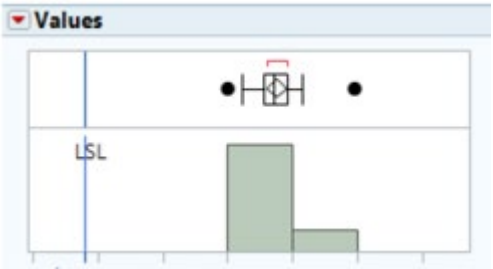


Fig.11: Ball shear results.

To validate the robustness of the assembly process corners, FIB analysis was performed with results shown in Fig.12. RDL to Al pad interface and dielectric to RDL interface were confirmed to be robust with no separation. WLCSP package samples assembled with critical process corner conditions were also subjected to 3x reflow stress to check for separation at key interfaces like RDL via to Al pad. Results from acoustic imaging are shown in Fig.13; confirmed package design and assembly process robustness, no delamination was observed.

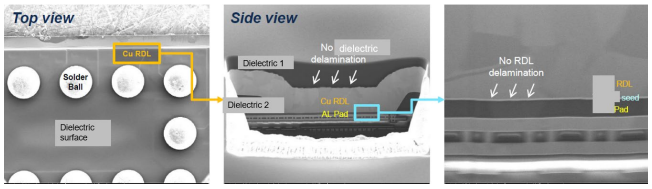


Fig.12: FIB analysis showing robust package interfaces.

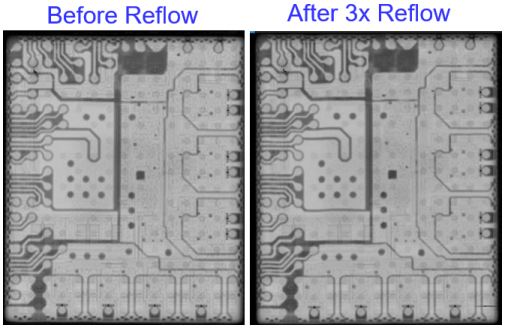


Fig.13: Acoustic images confirming no delamination before or after reflowing.

D. Reliability Validation

Reliability validation for the WLCSP radar package for RDL via robustness and BEOL integrity check was performed as per AECQ-100 standards. Component level reliability testing like temperature cycling (TC), high temperature storage life (HTSL), temperature humidity biased (THB) was performed to validate the robustness of package design and materials. WLCSP passed all AEC-Q100 stress requirements without any issues.

Table 1. Component Level Stress Results

Stress	Condition	Result
TC	-55/150C	Passed 1000 cyc
HTSL	150C	Passed 1000 hrs
THB	85C/85%RH	Passed 1008 hrs

Post TC stress, WLCSP package constructional analysis was performed to check for die passivation integrity. Fig.14 shows optical images of the die passivation showing no damage or cracks.

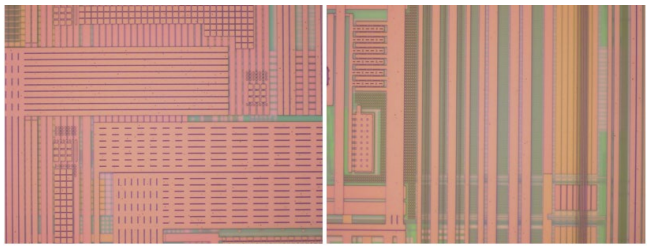


Fig.14: Optical images of die passivation post 1000cycles.

Board level testing was performed on the WLCSP package and passed 1000 cycles of -40/125C. Fig.15 shows scanning electron microscope (SEM) image of solder joint and RDL confirming no damage to either one.

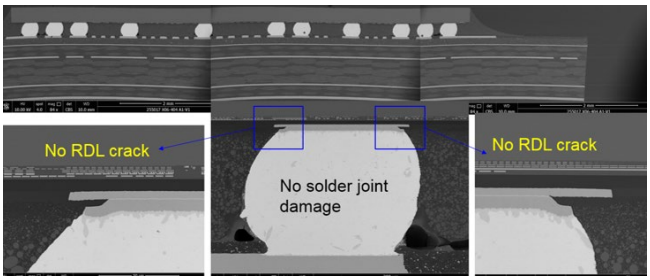


Fig.15: Solder joint and RDL post 1000 cycles of board level stressing.

FIB analysis was performed to assess the BEOL integrity in high stress areas as identified by mechanical simulations. Representative results are shown in Fig.16, no damage to the BEOL was noted.

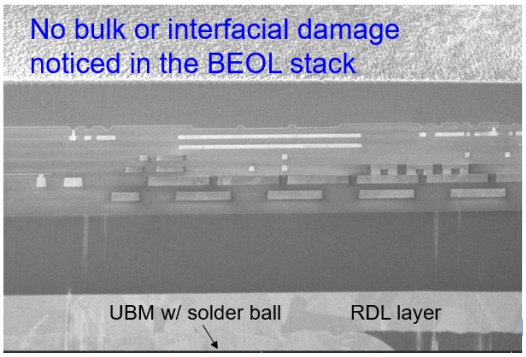


Fig.16: FIB image of the BEOL stack post 1000 cycles of board level stressing.

III. Conclusion

WLCSP package presents a significant advantage for radar applications due to loss dielectric losses, however, developing an automotive grade capable WLCSP requires thorough engineering development due to higher quality and reliability requirements. This study demonstrated that tools like mechanical simulations can heavily be leveraged to optimize the design, material, and assembly process selection. Assembly process risk assessment and windowing is important to ensure a robust assembly process and package. Developed package was proven to meet automotive grade 1 reliability requirements through component and board level testing with no risk of RDL via separation or BEOL damage.

Acknowledgment

The authors would like to thank Ilko Schmadlak for supporting mechanical simulations for this program and NXP Failure Analysis lab for support acoustic imaging and FIB/SEM/optical image analysis support.

References

[1] Berthold Hellenthal, “Inventing the Automotive Future”, *Semicon Korea*, Jan 2016, Seoul, Korea.

[2] J. Lau and R. Lee, *Chip Scale Package: Design, Materials, Process, Reliability and Applications*. New York: McGraw-Hill, 1999.

[3] P. Thomson, “Chip scale packaging,” *IEEE Spectrum*, p. 36, Aug. 1997.

[4] P. Garrou, "Wafer level chip scale packaging (WL-CSP): an overview," *in IEEE Transactions on Advanced Packaging*, vol. 23, no. 2, pp. 198-205, May 2000, doi: 10.1109/6040.846634.

[5] P. Nemeth, Z. Illyefalvi-Vitez, and G. Harsanyi, “Review of the reliability of advanced component packaging technologies,” in *Electronic Components & Technology Conference*, Las Vegas, NV, 2000, pp. 1605-1609.

[6] H. Yang et al., “Reliability evaluation of ultra CSP packages,” in Proc. *SMTA Emerging Technol. Conf.*, Chandler, AZ, 1998.