Conformal Silver Films for EMI Shielding of SiP Architectures

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Abstract

Electrospray printing is an additive manufacturing technique where a precursor solution composed of a solute material in a compatible solvent is subjected to a high electric potential, generating a spray of charged, solvent-encapsulated particles. Due to the high surface area to volume ratio, the solvent rapidly evaporates to deposit dry or partially-wet solute material onto a target surface. Over time, a thin continuous film is formed. Material emitted by electrospray is highly charged and will follow the electric field lines established between the emitter and a grounded target. As a result, this process is best suited for deploying material onto (grounded) conductive surfaces and can be used to create conformal coatings, even on non-line-of-sight surfaces. In contrast, delivering material to insulating surfaces is more difficult due to the accumulation of charge on the target, inhibiting the deposition of the solute and preventing the formation of a continuous film. We report on a new approach to improve deposition on dielectric (insulating) targets by manipulating the electric field and distribution of charge in the vicinity of the target surfaces. Colloidal silver in triethylene glycol monomethyl ether is deployed to create a conformal coating on packages consisting of a (i) broadband radiator encapsulated in epoxy molding compound and (ii) a model silicon flip chip assembly. We seek to replace board level shielding and provide electromagnetic interference protection for System-in-Package at frequencies from 100 MHz to 6 GHz, with a target of 60 dB of isolation at 1 GHz.

Key words

Electromagnetic interference protection, electronics manufacturing, electrospray deposition, EMI shielding, thin film manufacturing

I. Introduction

System in package (SiP) architectures require compartmental shielding from electromagnetic interference (EMI) protection. The current practice of board-level shielding is not ideal for space limited environments and creates the need for thin, conformal films that adequately shield high frequencies [1]. Traditional thin film manufacturing processes like chemical vapor deposition (CVD) and sputtering are costly due to their high temperature and low pressure demands, and they offer relatively poor uniformity on complex topographies [2]. An alternative and low-cost manufacturing technique is electrospray deposition (ESD) [3]–[5]. In electrospray, a precursor solution or "ink" composed of a solute material in a compatible solvent is dispensed at a constant flow rate to a microfluidic emitter. A high electric potential is applied and atomizes the solution into a "spray" of solvent-encapsulated solute droplets. This is facilitated by the formation of the Taylor cone, through a balance of electrostatic forces and liquid surface tension, which emits a charged microjet from its apex [6]–[8]. From here, the jet undergoes jet breakup, and the droplets repeatedly undergo fission events as the solvent rapidly evaporates. The dry or partially-wet solute material then continually deposits onto a target substrate and forms thin, conformal films. The processing parameters (flow rate, separation distance, etc.) control the resulting film microstructure, permitting the formation of highly-controlled films with tunable functional characteristics [9]–[15]. Additionally, electrospray is an electrophoretic process with non-line-of-sight targeting to areas not directly exposed to the emitter [16]–[18]. Here, we use ESD to create conformal, silver films on varying topographies to effectively shield electronics from EMI. We present two parallel targets: epoxy molding compound (EMC) test structures and silicon flip chip packages. We aim to provide a minimum of 60 dB of isolation at 1 GHz of applied

frequency, with testing ranges from 100 MHZ – 6 GHz.

II. Materials and Methods

A. Precursor Ink and Deposition Parameters

The precursor ink used in this work is 35 wt.% colloidal silver (≤ 50 nm) in triethylene glycol monomethyl ether (Sigma Aldrich, 736465). The ink is dispensed through a syringe pump (Chemyx) to a microfluidic glass emitter (150 µm, made in-house). The emitter is housed in a T-junction (IdexHS) that also holds a gold electrode to connect to the high voltage supply (model 2290-10, Keithley). Flow rates varied from 1 µL/min – 5 µL/min, and spray times ranged from 5 minutes – 30 minutes, yielding delivery rates from 500 µg/min – 2500 µg/min. To remove residual solvent, samples were cured for 8 hours at 95°C. The setup schematic can be seen in Fig. 1.

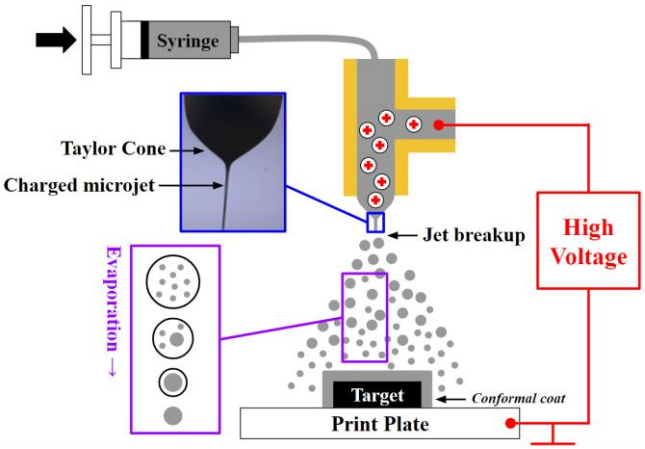

Figure 1. Electrospray schematic.

B. Target Substrates

We target two substrates using ESD. The first is an EMC test structure to explore the fundamentals of electrospray deposition, and the second is silicon flip chip packages to demonstrate this process on industry-standard samples.

i. EMC Test Structures

The epoxy encapsulated test structure is a low-cost, easily replicable target that can be manufactured in-house. It is composed of a custom printed circuit board (PCB, 25 mm x 15 mm) and a molded epoxy (832TC, Digikey). We examine two epoxy deposit shapes, cuboid and ellipsoid, to examine film conformality and uniformity on two different topographies. The PCB contains three aluminum pads that trace to an SMA connection. The two outer pads provide the film with a continuous connection to ground, and the center pad serves as a broadband radiator to broadcast the supplied signal. The test structure schematic is shown in Fig. 2.

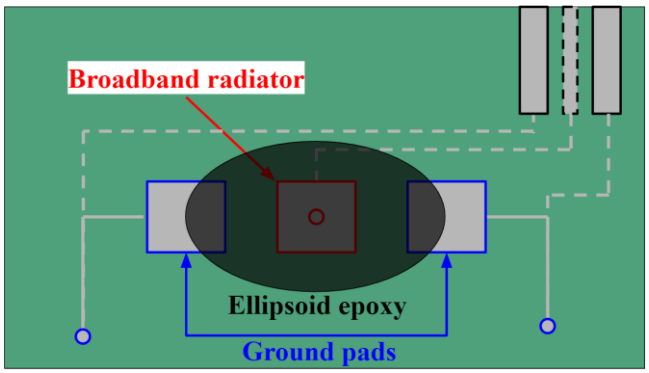

Figure 2. Schematic of an ellipsoid EMC test structure. Dashed lines show underside components and traces.

ii. Silicon Flip Chips

The second target is silicon flip chip packages. Blank flip chip substrates were provided by NXP Semiconductors. To more closely mimic industry standard samples, the team bonds a 10 x 11 mm^2 silicon rectangle (Si:Sb, <100>, 300 um thick, 0.01 – 0.02 Ω·cm resistivity) to the substrate with an electrically conductive epoxy (9410, Digikey). A schematic of this target can be seen in Fig. 3.

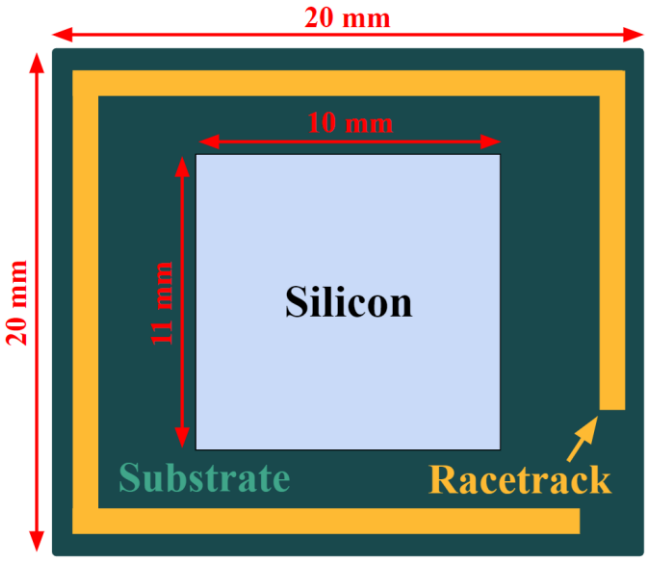

Figure 3. Schematic of a flip chip package.

Sprays were conducted onto packages with and without the silicon. Here, the target coverage area includes the silicon to the racetrack, with the intent to conformally coat the "step" created by the silicon die.

C. "Stenciling" Through a Dielectric Constant Mismatch

The electrophoretic nature of electrospray can present a challenge when targeting insulative substrates. In an electrospray, the solute material holds charge that must dissipate upon delivery to allow subsequent charged material

to deposit. When targeting conductors, the charge can rapidly dissipate to ground, thus permitting dense buildup of incoming material. However, on insulators, charge will linger and force the film to quickly reach a point of charge saturation where it can no longer accept incoming charged material, effectively repelling further material delivery, as shown in Fig. 4. This effect makes it difficult to build thick, continuous layers on insulators.

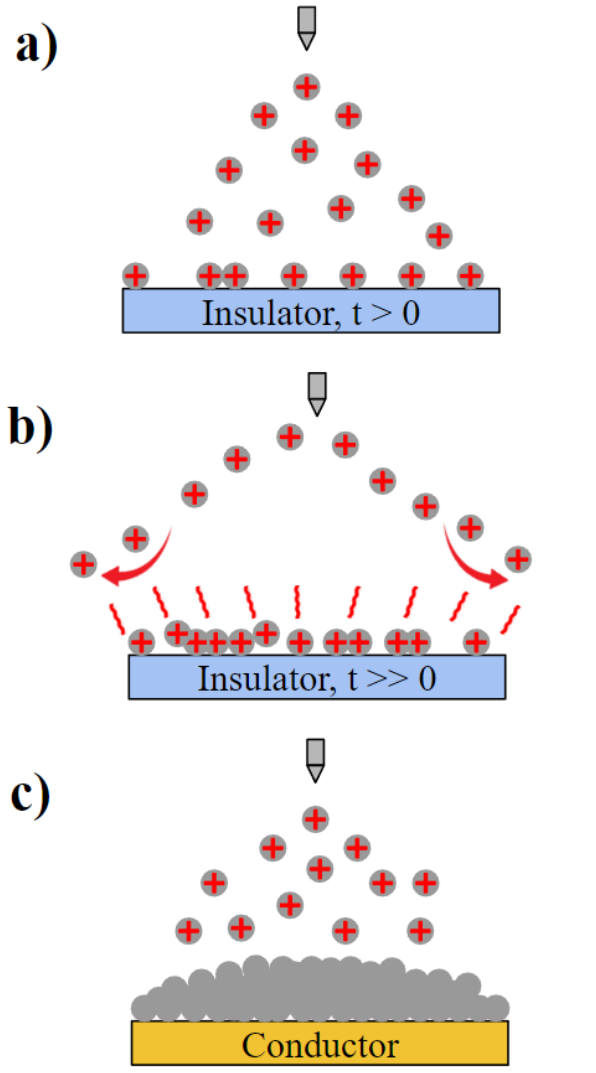

Figure 4. Schematic of an electrospray onto an insulator at (a) t > 0, (b) t >> 0 (charge saturation), and (c) a conductor.

To address this issue, we utilize a dielectric stencil to focus material to the underlying target substrate [19]–[21]. The stencil is a carefully selected material with a custom orifice that is placed on top of the target, as shown in Fig. 5. The orifice tracks the edges of the target area, with a gap to account for the behavior of the electric field lines at material interfaces. Here, a 2 mm orifice gap is used. Sprays were conducted with an ABS plastic and silicone rubber (3788T22, McMaster-Carr) stencil. The stencil increases deposition efficiency to the sample due to a dielectric constant mismatch between the stencil material and the target, which will be discussed further in the Results section.

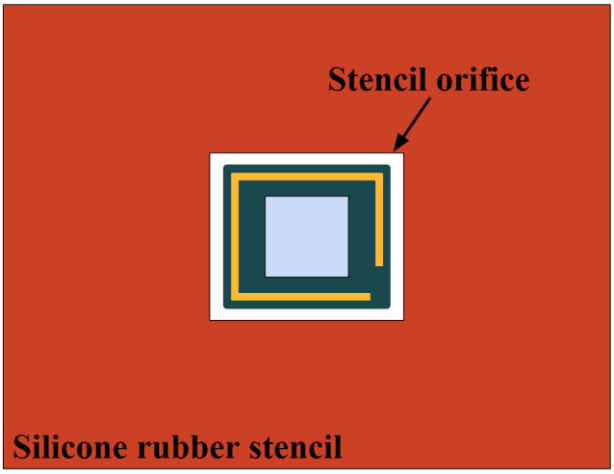

Figure 5. Schematic of a dielectric stencil with flip chip.

D. EMI Testing Setup

Work is in progress to evaluate the functional performance of the films in an EMI testing setup. We aim to establish a relationship between electrospray processing parameters, film microstructure, and shielding performance. To do this, a coated sample is placed in a Faraday cage with a receiver. A 20 GHz signal generator (Anritsu, MG3692C) is connected via a coaxial cable to the sample, and the receiver is connected to a 26 GHz signal analyzer (Agilent, EXA) that measures the attenuated signal, as shown in Fig. 6. Testing occurs at frequencies from 100 MHz – 6 GHz, with a minimum target of 60 dB of isolation at 1 GHZ of applied frequency. The collection of data is ongoing.

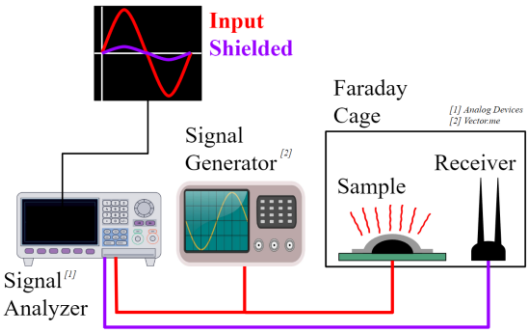

Figure 6. EMI testing schematic.

III. Results

A. Stencil Performance

Films prepared using the stencil showed a significant increase in deposition. This is likely due to the electrical property mismatch between the stencil and the target, which

relates to the charge decay of the material. The rate of charge decay (1), governed by the permittivity, ε, and resistivity, ρ, must be lower for the stencil than the target. Charge decay can be expressed as:

$$Q(t) = \frac{Q_0}{1+\frac{t}{t_{1/2}}} \quad (1)$$

where $Q(t)$ is the charge at time t, Q_0 is the initial charge, and $t_{1/2} = ln2 \cdot \tau_\varepsilon$ is the half-life, where $\tau_\varepsilon = \rho \cdot \varepsilon$. The slower rate of decay on the stencil allows charge to rapidly build up on its surface and "funnel" material to the target, as shown in Fig. 7. When targeting insulators, the electrical properties of the stencil must be carefully selected to yield a lower rate of charge decay than that of the target.

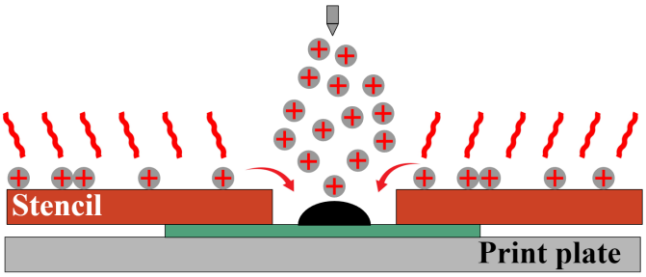

Figure 7. Cross-section schematic of a stencil during deposition.

We are investigating several unique stencil characteristics, including an increase in performance after multiple uses, and the origin of the material depletion region around the perimeter of the orifice. The stencil becomes more effective after multiple sprays. We believe this is due to dipole alignment within the stencil after exposure to the electric field used to induce the electrospray. The orifice depletion region occurs whenever the stencil is employed, and can be seen in Fig. 8.

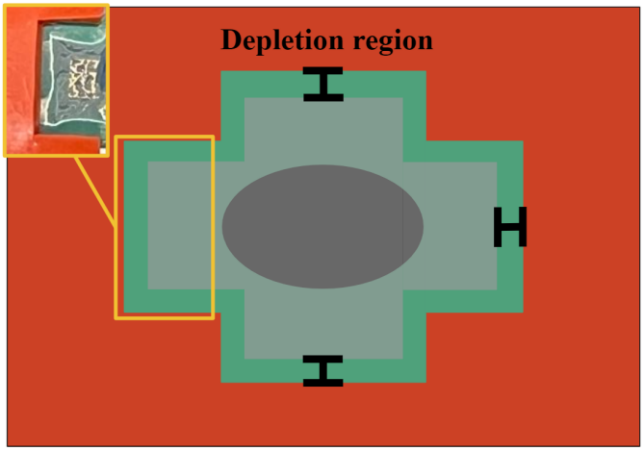

Figure 8. Schematic of a depletion region with an inset image of the region after an electrospray.

The depletion region occurs at the interface between two different materials and is likely due to the deflection of the electric field lines. Investigation of these behaviors is ongoing.

B. Film Characteristics and Microstructure

After deposition, samples were cured to remove any residual solvent and optical and electronic imaging were performed to evaluate the film characteristics.

i. EMC Test Structures

The cuboid and ellipsoid test structures were sprayed through a 1 mm thick ABS stencil at 5 µL/min for 30 minutes (2500 µg/min delivery rate). The coated cuboid test structure is shown in Fig. 9. The film conformally coats the top and undercut side of the epoxy to the PCB surface. The spray also conformally coats the ellipsoid test structure, as seen in Fig. 10.

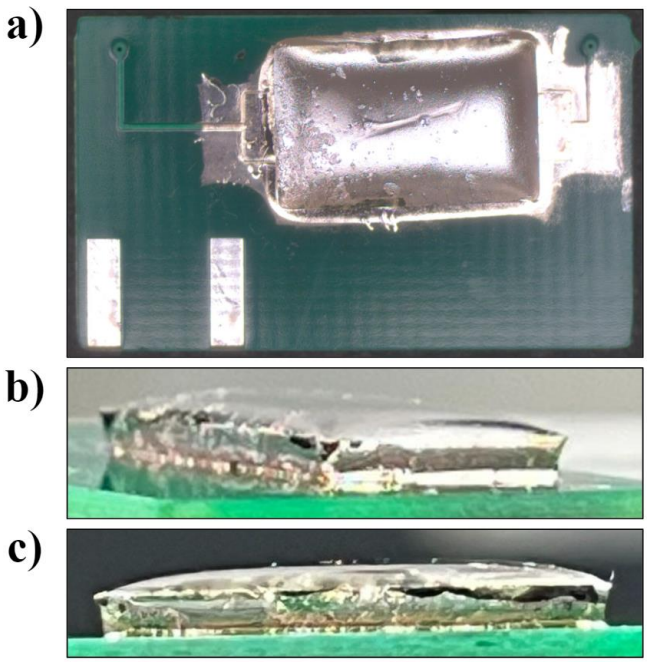

Figure 9. (a) Top view, (b) left side view, and (c) right side view of a silver coated cuboid test structure.

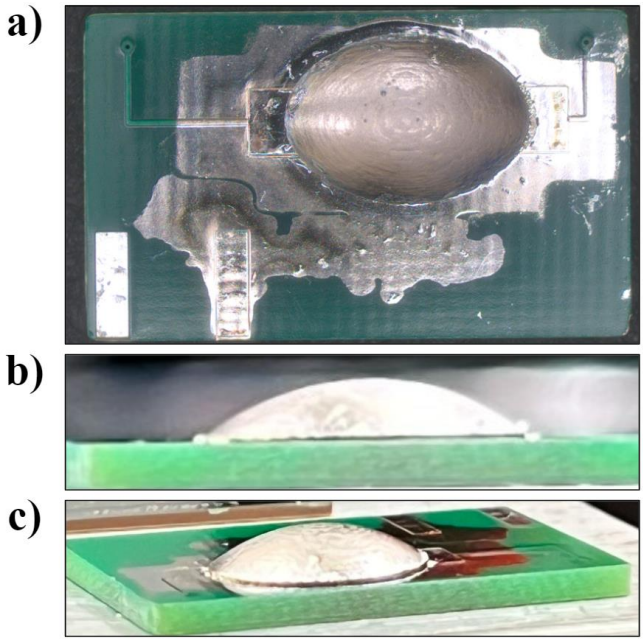

Figure 10. (a) Top view, (b) left side view, and (c) right side view of a silver coated ellipsoid test structure.

SEM imaging was conducted on the cuboid test structure, and is shown in Fig. 11. The film appears continuous, and its roughness is likely due to the underlying surface of the epoxy. Due to this roughness, it is challenging to achieve electrical continuity on the EMC test structures. Sheet resistance measurements via a four-point probe are in progress.

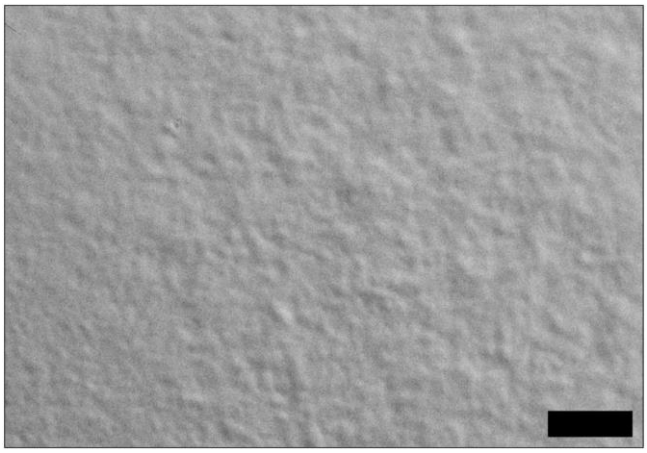

Figure 11. SEM image of a coated cuboid test structure. Scale bar is 50 µm.

ii. Silicon Flip Chips

Silicon flip chip packages were sprayed with and without the bonded silicon. Fig. 12 shows a substrate without bonded silicon before and after deposition. The sample was spayed through a 1 mm thick ABS stencil at 1 µL/min for 10 minutes (500 µg/min delivery rate).

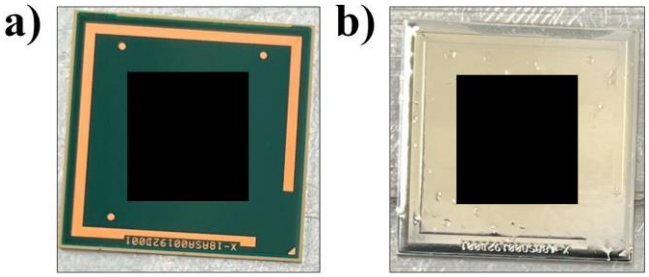

Figure 12. An (a) uncoated and (b) silver coated flip chip substrate. The pad array in the center is blacked out.

The film has continuous coverage from the substrate edge up through the center pad array and is extremely reflective. Fig. 13 shows SEM images of the film microstructure.

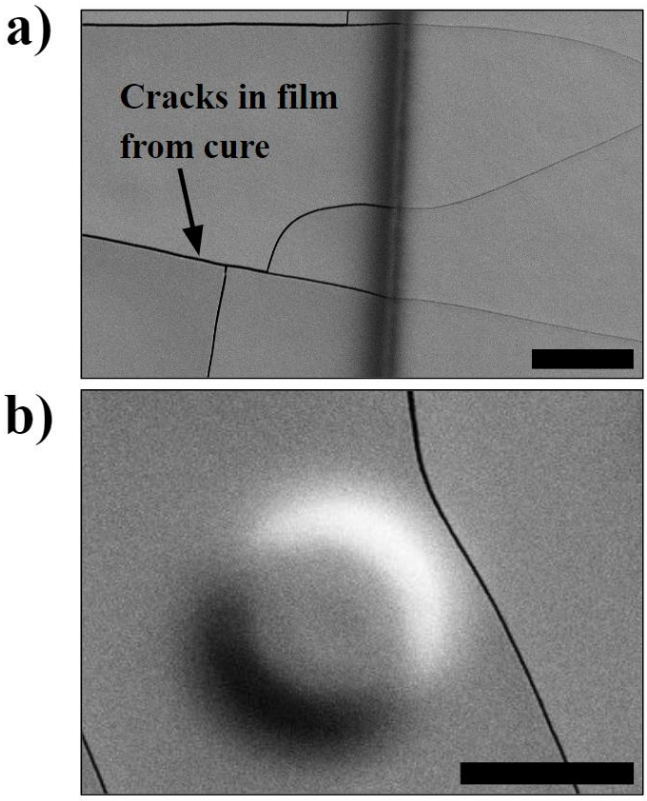

Figure 13. SEM image of a coated flip chip (a) substrate and (b) solder bump. Scale bar is 50 µm.

The cracks observed in the film are due to internal stress during the cure process and can likely be eliminated with optimized processing conditions. The film is smooth and may have achieved a degree of sintering during the cure process due to the scale of the silver particles (≤ 50 nm). The film is electrically continuous throughout. Two-point conductivity measurements report resistance values of less than 0.7 Ω across a 16 mm distance.

IV. Conclusion

We have used electrospray deposition to create conformal silver films on two targets: EMC test structures (cuboid and ellipsoid) and silicon flip chips. To overcome the issue of charge accumulation on insulators, we use a stencil with carefully selected electrical properties (a dielectric mismatch) to focus charged material to the orifice and enhance deposition efficiency on the target. The stencil becomes more effective after multiple uses, which is likely related to dipole alignment in the material. The stencil creates a material depletion region on the target that is still under investigation. The deposited films are continuous and electrical continuity is achieved on the flip chip substrates. Future work includes investigating stencil capabilities and behavior as well as collecting EMI shielding data. We aim to link electrospray processing parameters (flow rate, spray time, stencil usage) to optimal shielding performance.

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References

[1] G. Wong, N. Asymtek, and J. Choi, "Dispensing EMI Shield Materials: An Alternative to Sputtering," *SMT007 Magazine*, pp. 84–92, Aug. 2019.

[2] A. S. H. Makhlouf, "Current and advanced coating technologies for industrial applications," *Nanocoatings and Ultra-Thin Films*, pp. 3–23, Jan. 2011, doi: 10.1533/9780857094902.1.3.

[3] A. Tycova, J. Prikryl, A. Kotzianova, V. Datinska, V. Velebny, and F. Foret, "Electrospray: More than just an ionization source," *Electrophoresis*, vol. 42, no. 1–2, pp. 103–121, Jan. 2021, doi: 10.1002/elps.202000191.

[4] F. J. Higuera, "Structure of deposits formed from electrosprayed aggregates of nanoparticles," *J Aerosol Sci*, vol. 118, pp. 45–58, Apr. 2018, doi: 10.1016/j.jaerosci.2018.01.007.

[5] E. Bodnár, J. Grifoll, and J. Rosell-Llompart, "Polymer solution electrospraying: A tool for engineering particles and films with controlled morphology," *J Aerosol Sci*, vol. 125, pp. 93–118, Nov. 2018, doi: 10.1016/j.jaerosci.2018.04.012.

[6] A. M. Gañán-Calvo, "The surface charge in electrospraying: Its nature and its universal scaling laws," *Journal of Aerosol Science*, vol. 30, no. 7, Elsevier Science Ltd, pp. 863–872, 1999. doi: 10.1016/S0021-8502(98)00780-0.

[7] A. M. Gañán-Calvo, J. M. López-Herrera, M. A. Herrada, A. Ramos, and J. M. Montanero, "Review on the physics of electrospray: From electrokinetics to the operating conditions of single and coaxial Taylor cone-jets, and AC electrospray," *J Aerosol Sci*, vol. 125, pp. 32–56, Nov. 2018, doi: 10.1016/J.JAEROSCI.2018.05.002.

[8] J. Rosell-Llompart, J. Grifoll, and I. G. Loscertales, "Electrosprays in the cone-jet mode: From Taylor cone formation to spray development," *Journal of Aerosol Science*, vol. 125. Elsevier Ltd, pp. 2–31, Nov. 01, 2018. doi: 10.1016/j.jaerosci.2018.04.008.

[9] B. Almería, W. Deng, T. M. Fahmy, and A. Gomez, "Controlling the morphology of electrospray-generated PLGA microparticles for drug delivery," *J Colloid Interface Sci*, vol. 343, no. 1, pp. 125–133, Mar. 2010, doi: 10.1016/J.JCIS.2009.10.002.

[10] E. Burkarter, C. K. Saul, F. Thomazi, N. C. Cruz, L. S. Roman, and W. H. Schreiner, "Superhydrophobic electrosprayed PTFE," *Surf Coat Technol*, vol. 202, no. 1, pp. 194–198, Nov. 2007, doi: 10.1016/j.surfcoat.2007.05.012.

[11] J. Tang and A. Gomez, "Controlled mesoporous film formation from the deposition of electrosprayed nanoparticles," *Aerosol Science and Technology*, vol. 51, no. 6, pp. 755–765, Jun. 2017, doi: 10.1080/02786826.2017.1303573.

[12] Q. Guo, J. P. Mather, P. Yang, M. Boden, and P. T. Mather, "Fabrication of Polymeric Coatings with Controlled Microtopographies Using an Electrospraying Technique," *PLoS One*, vol. 10, no. 6, p. e0129960, Jun. 2015, doi: 10.1371/journal.pone.0129960.

[13] N. A. Brown, Y. Zhu, G. K. German, X. Yong, and P. R. Chiarot, "Electrospray deposit structure of nanoparticle suspensions," *J Electrostat*, vol. 90, pp. 67–73, Dec. 2017, doi: 10.1016/J.ELSTAT.2017.09.004.

[14] B. J. Kingsley and P. R. Chiarot, "Polyimide Films Manufactured Using Partially Wet Electrospray Deposition," *ACS Appl Polym Mater*, vol. 5, no. 3, pp. 1797–1809, Mar. 2023, doi: 10.1021/acsapm.2c01891.

[15] E. E. Pawliczak, B. J. Kingsley, and P. R. Chiarot, "Structure and properties of electrospray printed polymeric films," *MRS Adv*, vol. 7, no. 29, pp. 635–640, Sep. 2022, doi: 10.1557/s43580-022-00340-0.

[16] Y. Zhu and P. R. Chiarot, "Surface charge accumulation and decay in electrospray printing," *J Phys D Appl Phys*, vol. 54, no. 7, Feb. 2021, doi: 10.1088/1361-6463/ABC449.

[17] L. Lei *et al.*, "Obtaining Thickness-Limited Electrospray Deposition for 3D Coating," *ACS Appl Mater Interfaces*, vol. 10, no. 13, pp. 11175–11188, Apr. 2018, doi: 10.1021/acsami.7b19812.

[18] B. J. Kingsley, E. E. Pawliczak, T. R. Hurley, and P. R. Chiarot, "Electrospray Printing of Polyimide Films Using Passive Material Focusing," *ACS Appl Polym Mater*, vol. 3, no. 12, pp. 6274–6284, 2021, doi: 10.1021/acsapm.1c01073.

[19] B. J. Kingsley, E. E. Pawliczak, T. R. Hurley, and P. R. Chiarot, "Electrospray Printing of Polyimide Films for Electronics Packaging Applications," in *The 2022 IEEE 72nd Electronic Components and Technology Conference*, San Diego, May 2022.

[20] J.-W. Kim, Y. Yamagata, B. J. Kim, and T. Higuchi, "Direct and dry micro-patterning of nano-particles by electrospray deposition through a micro-stencil mask," *Journal of Micromechanics and Microengineering*, vol. 19, no. 2, p. 025021, Feb. 2009, doi: 10.1088/0960-1317/19/2/025021.

[21] L. Lei *et al.*, "Self-Limiting Electrospray Deposition on Polymer Templates," Jul. 2020, doi: 10.26434/CHEMRXIV.12730793.V1.