

Smart metrology control of Through Silicon Via etching process for High End Devices

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Abstract

In this paper, we report on an innovative process characterization solution that aims to control the uniformity of the Through Silicon Via (TSV) etching process. The solution relies on measuring complementary geometric characteristics of the open Through-Silicon-VIA (TSV) that are key to establish a reliable vertical interconnection. When TSV are fabricated either in high-density matrix or in isolated locations, the solution presented here allows the non-destructive reliable measurement of top / bottom diameter, depth, and thickness of top hard mask layer with a combination of optical techniques. As example of use case, we present the result of the characterization of three different products hosting TSV with top diameter as small as 3 μm and aspect ratio up to 17:1. The new methodology is compared to the state of the art of metrology control solutions used in the semiconductor industry.

Key words

Optical characterization, Process Control, Through-Silicon-VIA, VIA Etching Metrology

I. Introduction

The change in human society, with massive adoption of social networking and artificial intelligence, has pushed the semiconductor industry to develop devices capable of supporting the required infrastructures. Increasingly powerful computer process units (CPU) are used to allow data centers to process trillions of information exchanges, while faster graphic process units (GPU) enable virtual and assisted reality for gaming and advanced industrial applications.

Among the building blocks of CPU & GPU, the memory is the typical bottleneck to reach maximum performances. More specifically, the High Bandwidth Memory (HBM) is a high-speed computer memory interface for 3D-stacked synchronous dynamic random-access memory that was introduced for the first time in 2013 [1]. The HBM can achieve high bandwidth at low power consumption thanks to the vertical electrical interconnection scheme that uses Through-Silicon-VIA (TSV) to distribute the electrical signal from the top to the bottom of the die. The stacking of multiple units reduces the form factor.

TSVs are fabricated by etching the silicon bulk material down to the requested depth [2]. Once opened, each TSV is filled with metal and later the backside of the die is reworked

to reveal the nail. The typical corresponding process flow is depicted in figure 1. If the etching process step is well controlled, the next deposition steps (liner, Cu seed layer) are more likely to succeed with no uncovered area on the side wall. If the VIA is over etched, the deposited liner may be too thin, and the seed layer may not cover all the side walls. Subsequently, a void may occur when the Cu is electroplated, and the vertical electrical conductivity is dramatically reduced.

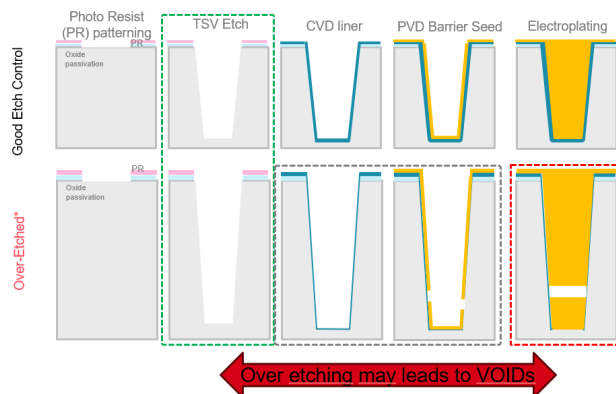


Figure 1: Process of fabrication of a TSV for vertical interconnection. Top row: normal process within requested specification; bottom row: abnormal process with over etching of the VIA.

Another major inconvenience when VIAs are under etched or over etched is the abnormal variation of the height of the pillar after the revealing step that results in an unreliable interconnection with the counterpart if the unit is stacked on top of another unit or on top of a substrate. This triggers a high risk of delamination.

Controlling the uniformity of the TSV dimensions (diameter and depth) is mandatory to realize the required vertical interconnections.

In this paper, we report on an innovative process characterization solution that aims to control the uniformity of the etching process.

As already deeply documented in the past, there is a direct correlation between the non-uniformity of the TSV size across the wafer and the increase in defectivity when performing the ensuing metallization step. Bad TSV etch control impacts chemical and physical vapor deposition (CVD and PVD) coverage that directly results in poor electrical performances and in Yield Loss.

This work includes the analysis of the here reported method in comparison with the main existing process control solutions so far adopted to secure the etch of the TSV.

II. Materials and Methods

A. Materials

All results are from 300 mm Si wafers processed with Reactive Ion Etching (RIE) to open TSVs with different photomask designs. This process includes repeated alternating isotropic dry etching and sidewall passivation/deposition steps [2]. The wafers used in this study are listed in table I with corresponding target critical dimension (CD) / depth of etched TSVs.

Product Type	Top CD (μm)	Expected Depth (μm)	Metrics measured
A	4	60	Depth & CD
B	3	30	Depth & CD
C	3	50	Depth & CD

Table I: description of the set of wafers measured in this study.

The product A hosts TSV 4 μm by 60 μm. The product B hosts TSV 3 μm by 30 μm. The product C hosts TSV 3 μm by 50 μm.

All three TSV types were fabricated with the VIA middle process.

B. Methods

We used complementary optical techniques available at UnitySC to characterize the TSV wafers.

The solution consists of measuring the depth, the top CD

and the bottom CD of the TSV. All the above metrics are derived from a combination of non-destructive optical techniques.

The depth of the TSV is measured with a Point Optical Sensor recently developed at UnitySC that illuminates the TSV hole with visible light from the top of the wafer surface. The new sensor is a Low coherent Interferometric Sensor that works at High Frequency (LISE-HF). By analyzing the reflected light, we calculate optical distances. As depicted in figure 2, each time the light beam crosses an interface, a component is reflected to the sensor. By interferometric analysis of the reflected signal, the optical thickness of each layer is estimated. In turn, the depth of the TSV is measured.

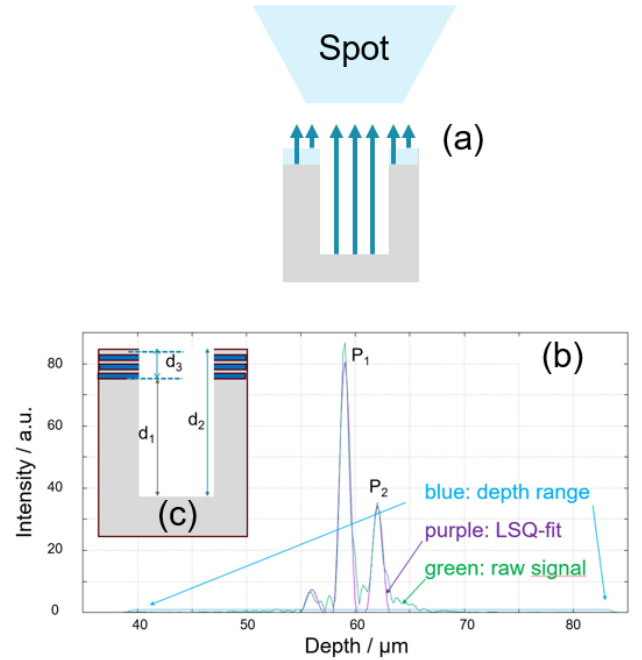


Figure 2: Method used to measure the depth of the VIA by LISE-HF sensor. Laser spot and wave reflections (a); Interference peaks representative of depth / distance in measurement signal (b); sketch of TSV designed structure (c).

The example reported in figure 2 refers to a single TSV with hard mask layer on the top of the wafer (Fig. 2a). Interference signal reported in Figure 2b shows two main peaks: the position of P1 on the FFT graph indicates the depth in the Si material without the contribution of the top layer (d1), while P2 indicates the total depth (d2). The accuracy of the metrology measurement was validated with destructive cross-section electron microscopy and with VLSI wafers hosting a trench 50 μm deep and predefined 2D structures with minimum width of 2 μm.

The top CD of the TSV is measured with the camera of the optical microscope that shares the optical path with the

sensor used to measure the depth. The image is collected at 50X magnification, with white light in reflection mode as depicted in figure 3a. Each TSV within the field of view (FOV) of the sensor can be processed simultaneously (Fig. 3b, c). The corresponding diameter is extracted (Fig. 3d) from the acquired optical image by computing the grey scale values variation at the transition area between the inside and the outside of the TSV.

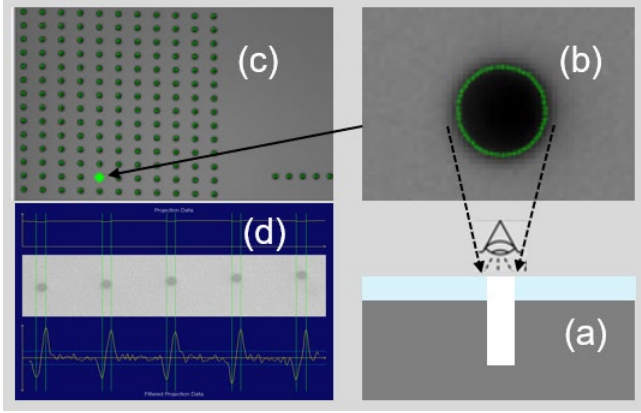


Figure 3: Top CD method: acquisition setup (a); contour detection of one TSV (b); automatic top CD detection of all TSV within FOV (c); gray scale transition edge detection (d).

The bottom CD of the TSV is measured with a similar technology as explained in figure 4.

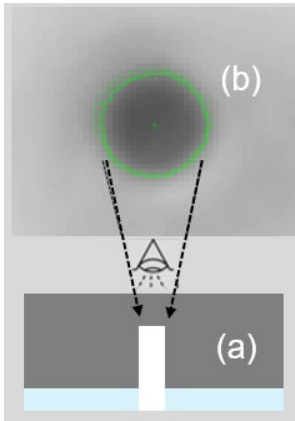


Figure 4: Bottom CD method: acquisition setup (a); contour detection of one TSV (b);

Note that in this case the sensor captures the image from the back of the TSV (Fig. 4a) and a combination of Near Infrared Lighting in transmission and reflection mode is applied to enhance the optical contrast of the bottom of the TSV (Fig 4b).

III. Experimental & Discussion

In this study, we measured either test vehicles or final products hosting TSV with top CD as small as 3 μm and aspect ratio up to 17:1.

The design of product A locates TSVs in two distinct regions within the die. In one region, the TSVs are grouped at low density with a pitch of 15 μm in the X and 30 μm in the Y direction, respectively (Fig. 5a). In the second region, the TSVs are designed in a high density 3 by 3 matrix with a pitch of 10 μm in the X and Y direction (Fig. 5b).

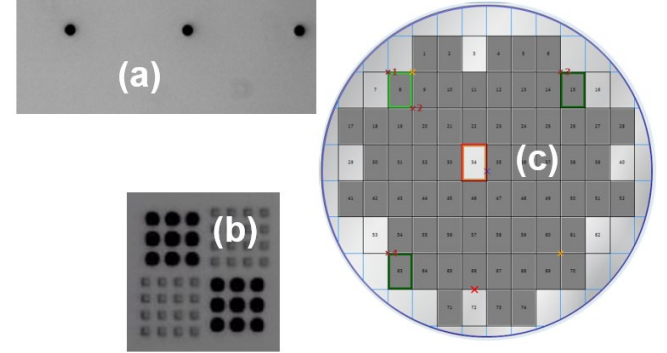


Figure 5: Low density TSV (a); high density TSV (b); wafer product layout and location of 9 measured dies (c).

The wafer was measured before removing the hard mask (multi-layer of SiO_2 and SiN). The Interference signal collected shows two main peaks in intensity: the highest in intensity is correlated to the depth in the Si material, while the second highest in intensity is correlated to the total depth though the hard mask and the Si bulk.

The precision of the measurement was tested in static mode by measuring the same site 15 times without moving the wafer, resulting in a 3σ (3 times the standard deviation, σ) value equal to 3 nm.

Point/#	Top hard mask		Total TSV depth	
	Thickness (μm)	3σ (nm)	Depth (μm)	3σ (nm)
1	3.06	12	64.69	41
2	3.07	25	63.97	44
3	3.05	14	63.49	36
4	3.07	8	62.61	22
5	3.08	15	62.99	29

Table II: average thickness of top hard mask, total TSV depth and corresponding 3σ dynamic repeatability.

The dynamic precision was estimated by measuring five sites (one at the center and four at the wafer edge) on the same

wafer. The same wafer was measured 10 times. Between each repeat of the five sites, the wafer was unloaded back to the FOUP and reloaded into the measurement chamber. Each measured site shows a 3σ precision <25 nm for the thickness of the hard mask and <45 nm for the depth of the TSV. The statistics collected are summarized in table II.

To investigate the potential TSV location density effect on the etch rate, we measured one TSV per region over nine different dies across the wafer as indicated in Figure 5c, for a total of 18 TSVs.

The comparison of the depth of the TSV located in the low-density region versus in the high-density region shown in Figure 6 clearly indicates that the high-density TSV are the deepest.

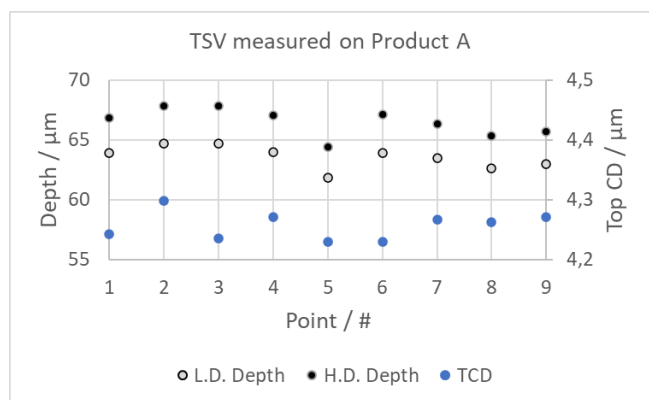


Figure 6: Low vs. High density TSV depth across the wafer of product A and corresponding Top CD.

From the same set of data, we can observe that the TSV in both regions is less deep at the center of the wafer (point 5). On the other hand, figure 6 does not show evidence of a direct correlation between the top CD variation and the corresponding depth. We can therefore conclude that the variation of depth from the center to the edge of the wafer is rather due to the inhomogeneity of the plasma used in the RIE chamber, rather than the influence of the top CD variation on the kinetics of the reaction. In summary, the variation of the etching process across the wafer of product A is $2.8 \mu\text{m}$ in the lower-density region and $3.3 \mu\text{m}$ in the high-density region, which is a high non-uniformity. On the contrary, the thickness of the hard mask varies only 40 nm across the wafer, which is well within the expected tolerance of the fabrication process. This result proves that the new sensor LISE-HF is capable of measuring not only the depth of the TSV etched into the Si material, but also the total depth that includes the thickness of the top hard mask used to define the region of interest where the VIA must be opened. This is a key benefit and improvement in accuracy versus the previous generation of LISE sensors [3,4] and versus the

panorama of existing solutions in semiconductor industry [5].

To explore the new sensor's capability on smaller TSV, we characterized the wafer of product B that hosts a unique family of TSV nominally $3 \mu\text{m}$ large at the top and $30 \mu\text{m}$ deep. To verify the precision in CD and depth we measured one TSV per die across five dies with similar procedure as adopted on Product A. The resulting 3σ value of the ten static repeats of TSV depth and hard mask layer thickness is within 3 nm at each site, while 3σ value with the wafer loaded and unloaded ten times is within 10 nm and 25 nm, respectively. To study the etch rate uniformity across the product B, we measured 12 dies evenly distributed across the wafer.

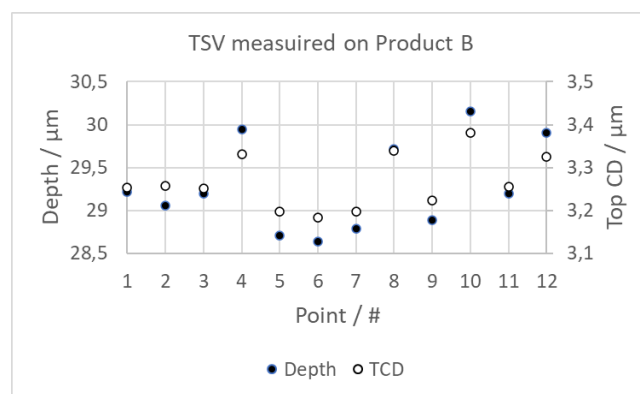


Figure 7: TSV depth vs. top CD of twelve sites across product B.

When the depth variation across the wafer is compared with the corresponding top CD values (Fig. 7), we can recognize a direct correlation between the increase in depth and the increase in top CD. This suggests the lag of RIE plasma process [6] might be the possible root cause of the depth variation. In this case, the larger CD is expected to allow more reactants / etchants entering the opening in the Si, resulting in faster etch rate, i.e., deeper TSV.

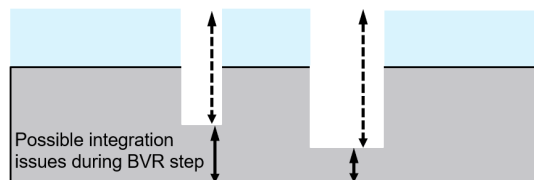


Figure 8. Expected increase of TSV depth when top CD is larger. The vertical/horizontal axis are not on the same scale.

The non-uniformity of the opening in the resist layer that is represented by the sketch in figure 8 was already well-reported in the past [7] and potentially due to resist shelf-life, non-optimized exposure parameters, and poor focus due to

extended warpage of the wafer. The detection of over/under etching of TSV across the wafer is key to avoid problems of integration during the backside revealing process step.

We completed the characterization of product B by increasing the sampling plan to 540 points across the wafer and investigated the possible correlation between the variation of the thickness of the top hard mask and the total depth of the TSVs.

Figure 9 represents the contour map of the TSV depth. The measured minimum to maximum variation of depth across the wafer is 1.14 μm .

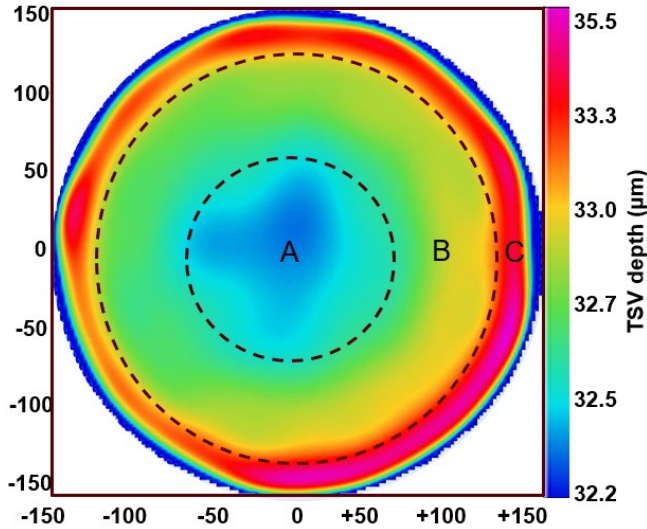


Figure 9: TSV depth contour map of product B.

The analysis of the TSV depth variation across the wafer clearly indicates three regions: the central region (A) where the TSV are less deep; a ring region (B) between 60 and 110 mm radially away from the wafer center where depth increases; an external ring (C) where the depth is deepest.

Figure 10 represents the contour map of the top hard mask layer thickness measured across the wafer which shows a measured minimum to maximum variation of 90 nm. We can also recognize three concentric regions (A, B, C) that match the position of the three rings highlighted in figure 9. Currently, it is unclear if the thickness variation of the top hard mask layer has a direct effect on the etching of the underlying Si material. In fact, while in the regions A and B we observe an increase in the hard mask thickness and in the TSV depth, the behavior is the opposite in the region C where the TSV are deeper even if the hard mask thickness is thinner with respect to the center of the wafer.

Our conclusion is that the etch profile across the product B is more driven by the trend of the top CD, than the thickness of the hard mask. Further investigations are needed to study the possible second order effect of the hard mask thickness on the etching process.

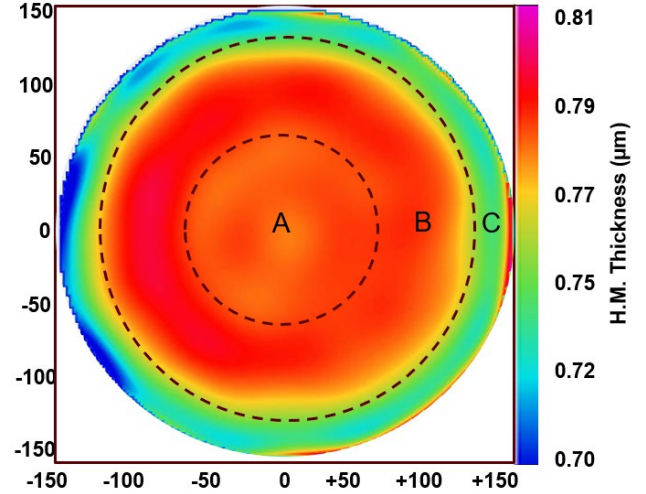


Figure 10: hard mask (H.M.) thickness contour map of product B.

The wafer of product C with TSVs targeted to be 3 μm large and 50 μm deep was measured to qualify the here presented metrology solution on structures with a high aspect ratio. In this case, the hard mask was removed from the top surface of the wafer before measuring the depth and consequently only one peak was detected in the FTT of the Spectral Power Density.

We applied the same methodology used previously on the wafers of products A and B to estimate the precision of the measurement (Table III). A comparison of the 3σ values reported in Tables II and III indicates that the shrinking of the top CD and the increase of the aspect ratio does not degrade the precision of the TSV depth control solution here used.

Point/#	TSV depth		Top CD		Bottom CD	
	mean (μm)	3σ (nm)	mean (μm)	3σ (nm)	mean (μm)	3σ (nm)
1	52.21	12	3.04	15	2.91	12
2	52.33	23	3.05	9	2.93	22
3	51.97	34	3.01	17	2.89	15
4	52.51	24	3.06	21	2.95	41
5	52.18	16	3.03	11	2.94	29

Table III: Precision of depth, top/bottom CD on product C.

The additional analysis of the data in table III confirms the linear dependency of the depth on the top CD. The comparison of the measured values of top and bottom CD indicates the etching process was well executed and resulted in TSVs with positive taper, i.e., with a side wall angle larger than 90° . Controlling the taper angle is mandatory to optimize the capacitance and the RC delay performance of

the vertical interconnection. It is also key to optimize the PVD process step to obtain a uniform coverage of the side wall with a Cu-seed layer.

IV. Analysis of state of the art in semiconductor industry

The ideal metrology solution to develop and monitor the TSV etching process is expected to fulfill the requirements listed in the table IV.

Criteria	Technique	Interferometry + imaging (Direct measurement)	WLI (Direct measurement)	Scatterometry (Indirect measurement)	X-SEM/TEM (destructive)
Depth		YES	FAILED if CD<3µm	Array only	YES but destructive
Top CD		YES	YES	Array only	YES but destructive
Bottom CD		YES	Only if taper is positive	Array only	YES but destructive
Side Wall morphology (scallop effect)		Not yet	NO	Array only	YES but destructive
thickness of hard mask layer		YES	NO	NO	YES but destructive
High Aspect ratio (A.R.>15)		YES	NO	YES	YES
Isolated TSV & non repeating		YES	Worst precision	NO	YES but destructive
Each single TSV and not miss "weak structures"		YES	YES...but at cost of TPUT	Only "Average" of ALL TSV inside spot	YES but destructive
Can precisely align each TSV by sharing sensor and camera optical paths		YES	YES...BUT X,Y positioning limited by pixel size	YES	YES but destructive
Easy Recipe Setup		YES	YES	Need DOE to build model	Need hours to prepare sample
TPUT		Best M.A.M. time	Worst MAM		Not HVM compatible
Destroys wafers				X-SEM needed to build model	Very High cost

Table IV: metrology capability needed to control the etching process versus main existing solution in semiconductor industry.

The only technology that can today fulfill all metrics is still the electron microscopy (X-SEM/TEM), but at the cost of destroying the wafer that must be cut to measure the cross section of the target TSV. In addition, this approach is subject to the human error, possibly introducing a systematic offset due to a wrong angle of imaging of the TSV target. White Light Interferometry (WLI) was successfully used in the past to replace X-SEM, because it is non-destructive, but it started to fail when measuring TSV smaller than 3 µm and aspect ratio >15:1. In addition, the WLI technology is incapable to measure negative taper (side wall angle <90°) [8]. Optical Scatterometry which is well-adopted to measure nano-TSV is limited on TSV for VIA middle design because it cannot measure isolated targets and risks missing short/long targets in the middle of an array of similar TSVs. Point sensors that measure the interferometric signal generated by the reflection of waves from the bottom of the TSV and from each interface crossed by the incident beam seem to be the best candidates to become the reference

technique to control the etching process.

V. Conclusion

In the current study, we demonstrated the capability of a newly developed sensor to measure depth and top/bottom CD of TSV, as well as thickness of the top hard mask when not removed before the measurement. The capability could be demonstrated on TSV with top CD as small as 3 µm and with aspect ratio up to 17:1.

This achievement makes the solution presented here eligible to be used for supporting the development phase of the etching process and monitoring of the stability of the etch tool when used in High Volume Manufacturing. The main benefit of this new process control solution is expected for the last and next generation of High Bandwidth Memories, where the TSV size is below 5 µm and the aspect ratio above 10:1, and for the heterogeneous integration of chiplets with 2.5D interposer [9].

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