Stress Analysis and Optimization on Saddle-shape Warpage by Direct Patterning of Stressed Film

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Abstract

As the stacks of the three-dimensional integrated circuits (3D-ICs) increases, the mechanical stress issues are challenging due to the increases in the asymmetry saddle-shape warpage. Various approaches to decrease asymmetric warpage were proposed by forming trenches of tens of micrometers or laser annealing treatment on the backside of wafer, but they had low throughput or lack of improved value. In this paper, we present a novel method to decrease the mechanical stress depending on the shape of the warpage by applying direct coating to the backside of wafer. The proposed method is to release the warpage by patterning a photo-sensitive polyimide (PSPI) with the inkjet-printing to adjust the surface characteristics and the steps, and then depositing tetraethylorthosilicate (TEOS) film with high compressive stress. We measured the changes in the asymmetric bow alongside the x-axis and y-axis before and after the process on the bare wafer by a finite element analysis using ABAQUS. Through the experiment and simulation, the x-y skew of about 230μm was obtained when 10μm-thick TEOS film was partially deposited on a 300mm wafer. In addition, by taking advantage of this process, the localized bow (warpage) can be released according to the changes in the thickness and area of the TEOS film. These results provide an effective guideline to solve unusual warpage caused by stacking process and can be applied to 3D integration in advanced packaging.

Key words

Warpage, Saddle Warpage, NAND, 3D NAND, backside patterning

I. INTRODUCTION

As the NAND was further scaled down to 20 nm or below, it has approached the limits of two-dimensional scaling, necessitating a shift towards 3D NAND flash memory, which allows for vertical cell stacking [1]–[3]. This transition to 3D NAND offered notable advantages, such as increased bit density and expanded process windows. However, with the successive increase in the number of channel holes and layers, a new challenge has emerged in the form of warpage issues attributed to inter-layer stress discrepancies at the interface within the multi-layered structure. Throughout the manufacturing process of 3D NAND, the wafer experienced stress accumulation in the direction perpendicular to the stacked films. This phenomenon was further aggravated by subsequent annealing processes and the inherent structural asymmetry of the NAND, leading to stress-induced degradation problems. The resulting wafer warpage posed critical concerns, as it could cause alignment errors during lithography processes [4], [5].

Furthermore, the growing complexity of the 3D NAND, with an increasing number of stacked layers, has led to heightened difficulties in the etching processes. In response to these challenges, researchers have proposed an innovative solution called "Bonded 3D NAND" as a promising next-

generation architecture [6], [7]. This approach involves the segregation of cell and peripheral circuits, facilitating the independent processing and bonding of the circuits within the two wafers. Bonded 3D NAND offers a parallel processing method, which not only reduces product development time but also widens the process window by enabling the independent manufacturing of each module.

Turning to the domain of semiconductor packaging, addressing wafer warpage remained a key problem. Conventional methods involved the application of heat or deposition of films on the backside of the wafer [8]. However, these methods have limitations, with heat application lacking precision in controlling wafer shape deformation and the deposition of films across the entire backside failing to effectively control asymmetric warpage along the x and y axes due to the overall stress imposed on the backside. To control the asymmetric wafer warpage, recent research proposed various approaches such as creating trenches on the backside of the wafer or selectively depositing stress relief films in the showerhead area during film deposition within the Chemical Vapor Deposition (CVD) equipment [9]. However, implementing trench formation introduced process complexity, including lithography steps, and increased the risk of particle contamination on the active surface. The technique of separating the showerhead area for film deposition has limitations, as it restricted the potential for improving wafer warpage within predefined regions of the equipment.

In this paper, we have developed a technique to selectively control the warpage of wafer in an asymmetric manner along the x and y axes. Leveraging a developed 3D finite element analysis model for prognosticating alterations in wafer geometry, we achieved the capability to regulate x-y skew by appropriately applying the stress-inducing films to the backside of wafer. We conducted a comprehensive assessment of warpage alignment between the simulation results and the fabricated samples, employing the commercial finite element analysis software ABAQUS as the simulation tool. By means of our model, which encompasses the novel asymmetrical warpage compensation pattern, we introduced a useful methodology to address intricate anomalies in warpage stemming from intricate lamination processes. This approach empowers the design and implementation of compensation patterns, subsequently leading to heightened yields in NAND memory fabrication, along with the resolution of critical issues like misalignment during bonding processes.

II. EXPERIMENTAL

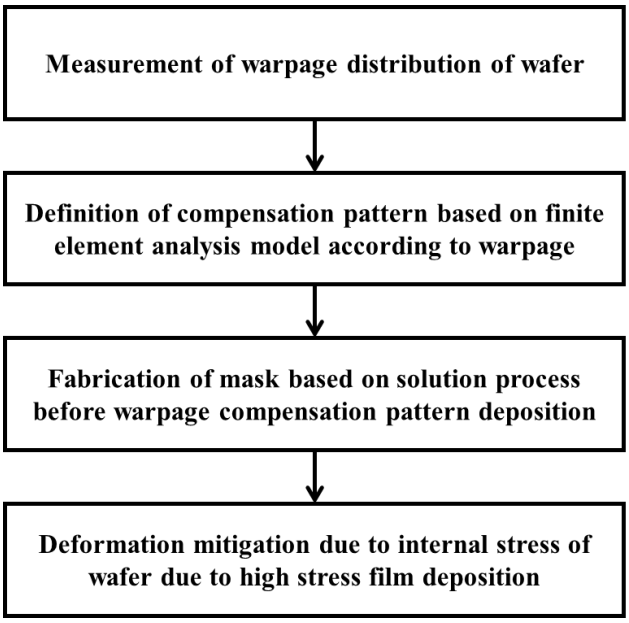

Figure 1. A schematic diagram of asymmetric warpage compensation process

As described in Fig.1 above, in order to compensate for the asymmetry warpage of the wafer, the present model devised a method of measuring the asymmetry and numerical value of the warpage and proposing a compensation pattern. We measured the warpage distribution on the rear surface of the wafer by the moiré method through the equipment named TDM (INSIDIX). This method need the pretreatment process depending on the sample condition. The warpage can also be measured by a white light interferometer (WLI) or other method. We made a simplified method of improving asymmetric warpage by depositing a compensation pattern on a wafer with warpage. First, the warpage distribution of the bare wafer was measured, and the warpage change was measured by forming the devised compensation pattern on the back of the wafer. Consistency was evaluated by comparing this method with the simulation method.

Material	CTE(ppm)	Elastic Modulus (GPa)
Si	2.6	169
TEOS	0.5	70
PSPI A	35	3.4
PSPI B	133	0.3-1.2

Table 1 Material characteristics of Thin film

A plasma-enhanced chemical vapor deposition (PECVD) system equipped with RF power 200W was used to deposit TEOS films. Deposition rates of 2nm/min were obtained at 400 degrees. A thickness of 6µm was targeted. The films were deposited on p-type 200mm-diameter, 725µm-thick silicon wafers. The coefficient of thermal expansion (CTE) and viscosity of the two photo-sensitive polyimide (PSPI) inks and tetraethylorthosilicate (TEOS) layer in sample production and simulation properties are as shown in the Table 1. PSPI is a UV curable solution and has the advantage of maintaining physical properties even in a process of 350 degrees or more after final curing. Here, the PSPI B ink is capable of direct patterning such as inkjet printing with low viscosity ink of 20cP or less depending on the temperature at the time of coating. With this advantage, this ink may be manufactured as a mask by inkjet printing or the like without a separate lithography process to perform a role of patterning a stress film on the rear surface of the wafer.

Prior to real verification, we developed a three-dimensional finite element analysis model to predict changes in wafer shape due to compensation pattern deposition. This model was developed as ABAQUS, a commercial finite element analysis software. The model consisted of three structures: a silicon wafer, a stress membrane TEOS layer, and a PSPI layer serving as a mask. Simulation for wafer warpage prediction proceeds in several stages as follows. Mechanical and thermal changes during the real process to compensate for wafer warpage were reflected as much as we could. First, an initial warpage was formed on the bare wafer. In the next step, the temperature of the simulation was raised to the deposition temperature of the TEOS layer, and the TEOS layer was modeled on the wafer surface. In the third step, the temperature was cooled to room temperature and rises to the deposition temperature of the polymer PSPI. Then, the polymer layer was modeled and the temperature was cooled to room temperature. The warpage of the wafer during the simulation was caused by the difference in the coefficient of thermal expansion and the contraction of the polymer layer during the curing process.

III. Result and Discussion

In order to verify the consistency between the developed model and the actual sample, we conducted a numerical comparison between the simulation result and the warpage measurement result. By substituting the warpage values of TEOS and PSPI ink into modeling, the shape change of the wafer by CTE and Elastic modulus was modeled. The completeness of modeling was evaluated by comparing it with the result value of the moiré analysis of the sample produced. At this time, it was assumed that the curing shrinkage of the PSPI does not affect the warpage change of the wafer in the previous soft break or exposure. It was

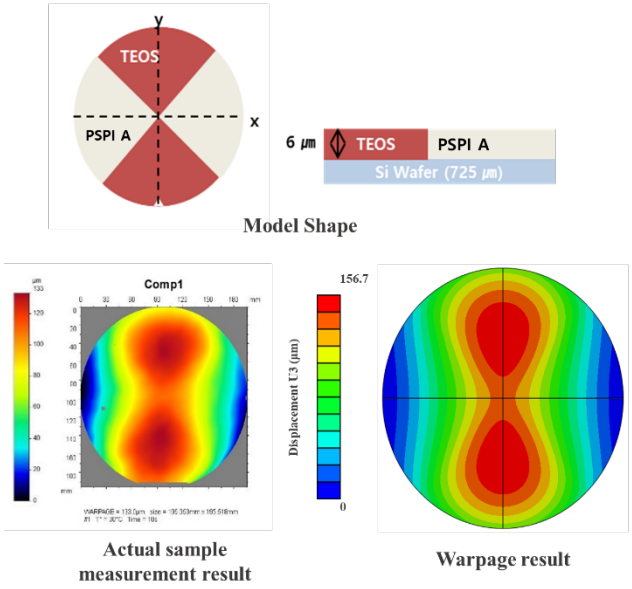

Figure 2. A schematic of model shape (top) of TEOS (6µm) and PSPI A (6µm) and the validation results (bottom) of the measured result and the simulation result

assumed that gravity acted in the direction of decreasing warpage.

As shown in Fig. 2, assuming that the thickness of the TEOS layer is 6µm, the x-y skew of the produced sample is about 100µm, which is almost similar to the simulation result of 94.5µm, indicating that consistency between the experimental value and the simulation model has been secured. That is, it was found that the simulation model we developed can simulate the stress change caused by the actual process on the wafer and be used for warpage

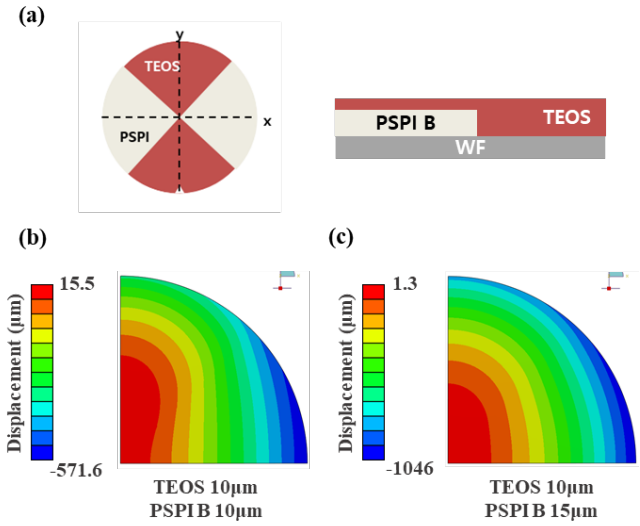

Figure 3. (a) A schematic of model shape of TEOS (10µm) and PSPI B (10, 15µm), the simulation result of (b) case 1 (thickness of PSPI B: 10µm) and (c) case 2 (thickness of PSPI B: 15 µm)

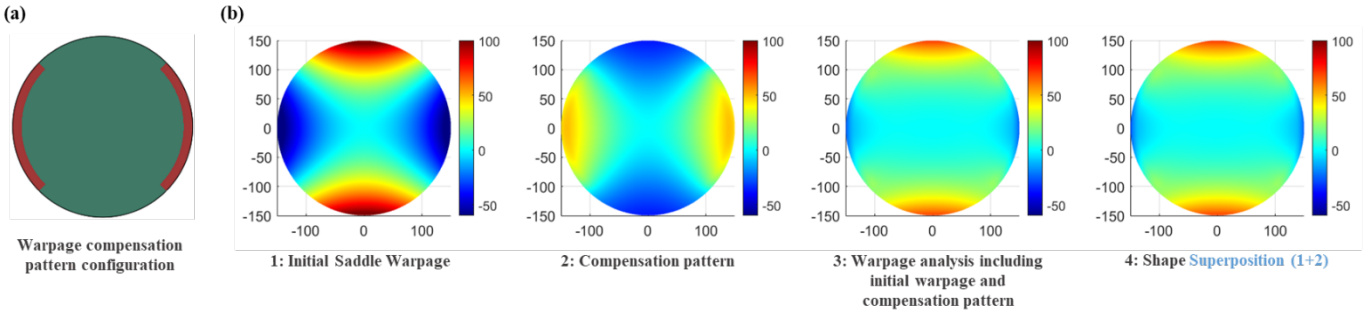

Figure 4. (a) Configuration of warpage compensation pattern, (b) Comparison between 3: simulation result of warpage analysis including initial warpage and compensation pattern and 4: Shape superposition of 1: initial saddle warpage and 2: compensation pattern

prediction. Furthermore, it is possible to predict the compensation performance of patterns for compensating for warpage according to the previous process and present an optimal compensation pattern. Using this model, we verified warpage compensation performance with various compensation patterns. The pattern was made of TEOS pattern side and PSPI B layer. As a result of the evaluation, it was confirmed that pattern deposition can compensate not only for representative warps such as concave, convex, and saddle-type warpage, but also for other complex warpage.

Based on the real validation result using PSPI A, a compensation pattern was produced using PSPI B ink. The model was a 12-inch wafer of 775μm full-thickness, with a thickness of 10μm for TEOS layer and 10μm and 15μm for PSPI B layer. The gravitational effect was excluded, and it was assumed that PSPI B layer was cured at room temperature with a solution developed to be cured only with ultraviolet rays. Since PSPI B film has a volume shrinkage of 5% when cured compared to PSPI A film, the warpage generated when depositing PSPI B layer 10μm was 11μm. As shown in Fig. 3(b) and Fig. 3(c), when the TEOS layer was 10μm and the PSPI B layer is 10μm or more, the x-y skew was made to be about 230μm. The deviation was within 10% of the measured sample value of about 213μm. This shows that the stress relaxation can be predicted with the warpage generated as a compensation pattern in simulation for any initial warpage shape.

The saddle shape warpage was implemented as a compensation pattern on the bare wafer as shown in Fig.2. As the basic form, it was divided into quadrants and applied in the TEOS and the PSPI planes. Based on the y-axis, both the values of the measured result and the simulation model measured the largest bow value inside the edge rather than increasing the smile bow value from the center of the wafer to the edge. Therefore, as shown in Fig. 4(a), we devised a pattern for implementing the maximum-minimum bow at the edge. It was confirmed that the implementation of the compensation pattern also works on the actual initial saddle shape warpage. As shown in Fig. 4(b), the value of x-y skew measured by creating a warpage with the compensation pattern in the bare wafer and the value of superposition of the initial saddle warpage (4) were compared with the warpage value of the model reflecting the initial saddle warpage and the compensation pattern. The initial warpage was a saddle shape with a y-axis of smile and an x-y skew of 179μm. The compensation pattern made an x-y skew of 86.3μm in the form of a smile x-axis. The warpage compensation simulation result value on the wafer by the compensation pattern decreased by 81.2μm to 97.8μm. This analysis result was found to be almost the same as the value obtained by super-positioning the initial warpage shape and the warpage shape generated by the compensation pattern and the maximum error of 0.31μm. That is, it is viable to predict the compensation value of the initial saddle shape warpage with the warpage made of the compensation pattern on the simulation.

IV. Conclusion

We developed a method of modeling and manufacturing a compensation pattern that resolves the warping of the wafer in the form of saddles with different internal stress directions of the x-axis and y-axis. In order to predict the shape change of the wafer, we adjusted the x-y skew by applying the stress induction film only to the desired area on the back of the wafer using a commercial 3D finite element analysis model. The consistency of the model was secured by comparing the produced sample with the warpage result of the simulation model. Through a combination of experiments and simulations, we secured an x-y skew of about 230μm through partial deposition of a 10μm thick TEOS layer on a 300mm wafer. In addition, this technique enables stress relief of localized warpage based on thickness and coverage adjustment of TEOS film. This model proposes valuable solutions to solve alignment problems in subsequent bonding and photo processes by compensating for asymmetric warpages occurring in stacking and etching processes in 3D NAND flash memory.

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