Study on the Manufacturability of XDFOI Package with Organic RDLs (XDFOI-O)

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Abstract
The concept of chiplet has been proposed in the post Moore era, while how to achieve the layout of multiple chips of different processes and sizes in the manufacturing process is a coming problem that needs to be considered. Different layouts may significantly affect the manufacturability during the packaging process. Prospective finite element analysis (FEA) can evaluate various layouts by optimizing the layout and increasing the placement of dummy chips as stiffeners, thereby selecting the best layout and combination method. In addition, the characteristic of chiplet packaging is that multiple chips may come from different sources, such as different foundries, processes, sizes, or even thicknesses. This really poses challenges to the subsequent flip chip and wafer thinning process for leveling the total package. It is necessary to confirm the evaluation of the impact of chips with different thicknesses and underfill coverage in the process, so as to ensure the consistency in processing and improve the yield of packages.

Key words
chiplet, manufacturability, RDL interposer, wafer thinning, XDFOI-O

INTRODUCTION
With the increasing cost of advanced wafer manufacturing processes in foundry, the concept of chiplet has gained increasing attention in the post Moore era [1-2]. Chiplet is the concept of breaking down the functions of a single SOC chip into numerous small chips, and then using advanced packaging technology (MCM/2.5D/3D, etc.) to reassemble a large and complex system into one package, thereby reducing the total cost of the chip. Some modules do not require the use of the most advanced wafer process, and can also utilize some chiplets in subsequent projects to achieve IP reuse and significantly reduce the costs [3].

The implementation methods of chiplet packaging mainly include the following: MCM, 2.5D packaging, 3D packaging, etc. At present, 2.5D packaging is the mainstream method of chiplet packaging, which refers to the packaging of high-density I/O interconnections between chiplets through interposer layers, characterized by the ability to integrate multiple dies and achieve high density. According to the current technologies, 2.5D packaging is mainly divided into redistribution layer (RDL) interposer and Si interposer. RDL interposer packaging enables multiple chips to be electrically connected in wafer level through RDLs (redistribution layers). Compared to traditional MCM packaging, RDL interposer packaging technology can reduce the distance between chips, significantly reducing the signal connection width and spacing. In addition, compared to Si Integrator, 2.5D RDL interposer eliminates the silicon through via (TSV) process, has lower thermal resistance and better mechanical properties [4-5], and has significant cost advantages. Therefore, 2.5D RDL interposer (named XDFOI-O, X dimension fan out integration [6] with organic RDLs, in this paper) is a more balanced chip solution in all aspects. At present, the minimum line width/spacing of RDL interposer can be 2 um/2 um and the layer counts reach 6 to form a 6P6M (6 passivation layers and 6 metal layers) routing structure. The distance between chips can reach 60-100 um. The dielectric layer is made of polymer material, with a thermal expansion coefficient similar to that of the substrate, which can reduce the mechanical stress on chiplet. In addition, due to the bumping process used in the middle-end packaging, which is a role of OSAT (outsourced semiconductor assembly and testing), the size of the metal copper in the RDL interposer can be made larger in tandem with a lower resistivity, which can significantly reduce the signal transmission loss through RDLs [7].

In this work, the manufacturing processes of XDFOI-O packaging were mainly explored, focusing on two aspects. Firstly, under the constraint that the packaging area is defined specifically, chiplets cannot fully fill the entire packaging area and the stress issue may happen in the following processes [8]. Finite

element analysis (FEA) simulation was conducted on the layout and the structure of stiffeners, thus providing some directional guidance for layout. Secondly, due to the fact that chiplets may come from different suppliers and have significant differences in the size and thickness of their incoming materials [9], subsequent processes may also face challenges after assembly onto interposer wafers [7]. Therefore, we discussed the subsequent processes and provided directional guidance for incoming materials. Through this series of investigation, it is expected to improve efficiency and accelerate the introduction of chiplet products in terms of manufacturability.

EXPERIMENTAL METHODS

A. Test Package Structure

Fig.1 illustrates the process flow of XDFOI-O. The entire flow is a typical RDL-first process, divided into six major steps. Firstly, high-density RDLs is completed on the carrier wafer for chip interconnection. Then flip the chip onto the high-density RDLs, and then encapsulate the chip with underfill and wafer molding materials. Grind the back of the chip and molding compound to expose the silicon, remove the carrier wafer, and perform bumping on the other side to produce C4 (Controlled Collapse Chip Connection) bumps. Finally, metals can be selectively deposited on the wafer back for achieving high performance heat dissipation of the package. The reconstructed package may have a significant impact on the stress of the C4 in Step5 and the following fcBGA processes [10].

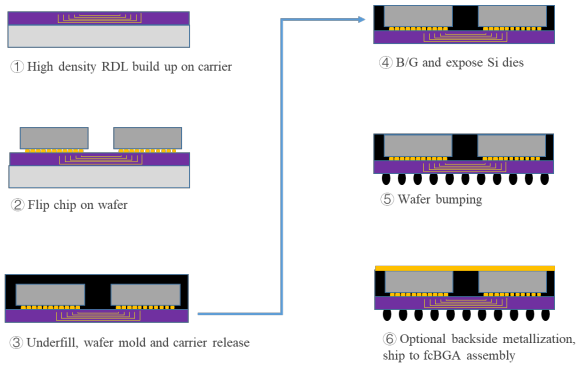


Fig.1 XDFOI-O process flow

The chiplet sets and package size are shown in Table I. In this XDFOI-O package, assuming the package functionality can form a complete system, three chips, namely computing chip (A), memory chip (B), and I/O (input/output) chip (C), are assigned the sizes of 16.7*10mm, 4.8*3.2mm, and 0.6*0.4mm respectively. The size of the primary packaging body is 19*16mm. There is obvious area redundancy in distributing the three chips into the packaging body, and optimization of the layout is needed. Stiffeners should be configured in the structure to reduce the stress inside the packaging body and increase the process window and yield for subsequent processes. Table 2 shows the combinations of three types of chips and stiffeners. From the schematic diagram, it can be seen that the scheme involves a total of three types of chip-and-stiffener combinations. In Layout 1, D-0 replicates Chip B, with the same size and thickness. Layout 2 adds stiffeners D-1 on Layout 1, and Layout 3 adds stiffeners on the two previous layouts. After D-2 is added, the combination of the right chip and stiffer is flush with Chip A. For ease of comparison, both the chip and stiffener are made of the same silicon material and have the same thickness. In addition, the connection between the stiffeners and the reconstructed wafer is evaluated using two methods, namely DAF (die attach film) or conventional flip chip interconnection, therefore the assembly processes of silicon stiffners are divided into die attachment (DA) and flip chip attachment (FC). For flip chip method, after the interconnection, the bottom of the chip is filled with underfill material.

According to the layout shown in Table II, the best combination can be preliminarily obtained after simulation. On this basis, further research will be conducted on the subsequent processes. Although in the layout simulation, it is assumed that both chips and stiffeners have the same thickness, while in actual production, it is difficult for small chips to have the same thickness setting as large chips. Due to the need for thicker chips to maintain the feasibility of flip chip and other processes, small chips may need to be thinned in advance due to the insufficient sawing street dimension for blade singulation. As shown in the Fig.2 below (under microscope), without controlling the thickness of the incoming chiplets, it is easy to detect chip cracking issue in the distinguishing area after wafer thinning, which seriously affects the yield of the product. Therefore, as a further combination adjustment compared with that in Table III, thickness of chip B and Chip C is adjusted, and an extreme assumption is made for underfill coverage, that is, the thinnest chip has underfill coverage on the chip back due to the material properties. Finally, the dynamic simulation is conducted to verify the tendency. The setting conditions are shown in Table III.

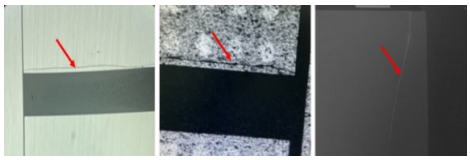


Fig.2 Chip cracking after wafer thinning

Table I
The chiplet sets and package size in this evaluation

	Item	Size	Thickness
A	Compute Die	16.7*10	0.75
B	Memory Die	4.8*3.2	
C	I/O Die	0.6*0.4	
	Package Size	19*16	

Table II
The layout of chiplets and stiffeners

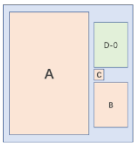
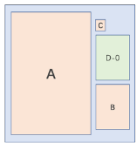
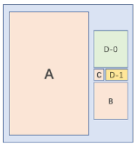
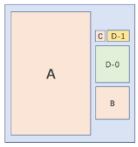
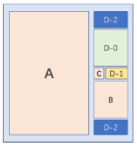
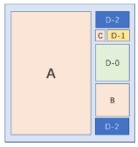
Layout Options	Schematic
Layout 1	1-1  2-1 
Layout 2	1-2  2-2 
Layout 3	1-3  2-3 

Table III
The combination of chip thickness and underfill coverage

Condition		Thickness			Underfill on chip
		Chip A	Chip B	Chip C	
A	A-1	750	750	300	Y
	A-2		750	300	N
B	B-1		300	750	Y
	B-2		300	750	N

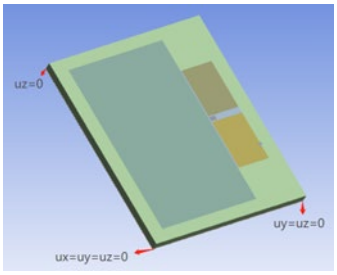
Table IV
Material properties of XDFOI-O package

Item		Unit	Si	Copper	PI	SnAg	EMC	Underfill	DAF
Tg		℃	NA	NA	230	NA	160	95	177
CTE	α1	ppm/℃	2.62	17	65	22.5	9	25	144
	α2	ppm/℃					38	95	188
E	25 C	GPa	129	110	3.5	11.6	18	11	0.6
	260 C	GPa					2.5	0.15	0.002
Poisson's ratio		--	0.28	0.33	0.3	0.4	0.3	0.3	0.3

B. Simulation Work Description

For the different package layouts, the finite element analysis software ANSYS with the Statics module is applied to study the characteristics of stress performance. The ELK layer is not modeled in the FEA, so only stresses on the different materials and the total packge deformation are compared.

For example, build the model using the Layout 1-1 in Table II, as shown in the Figure 4. Simplify multi-layer RDLs in a stacked form with RDL and PI thicknesses unchanged. Select a reflux temperature of 175℃ as the stress free temperature, and then extract the stress at room temperature. Table IV shows the material properties, and only linear elasticity is considered for all materials. Try to choose a hexahedral mesh as much as possible. Due to the special nature of solder balls, it is a tetrahedral mesh, as shown in Figure 4.



(a) Top view

(b) Multi-layer RDL equivalent

Figure 3. Model simplification (a) Top view, (b) Multi-layer RDL equivalent

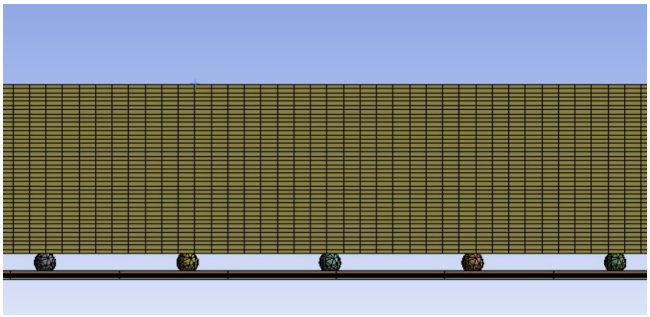


Figure 4. Model mesh generation

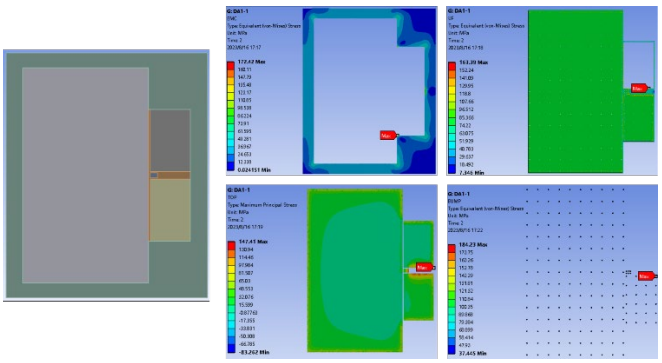
Furthermore, ANSYS/LS-DYNA is applied to develop a dynamic finite element modeling method for wafer thinning process. In order to simulate the effect of wafer thinning on the stress around the chip, a dynamic modeling method for the influence of underfill thickness was established. Boundary conditions are defined in the three-dimensional strain model. The bottom of the wafer is fixed, and the upper surface is free. Model the grinding wheel as a rigid body. The grinder comes into contact with the wafer at a fixed speed. Defined the frictional contact between the grinding machine and the wafer surface. Simulated the friction effect between the grinding machine and the wafer surface. When a high-speed grinding machine impacts the wafer surface, this impact load introduces dynamic stress into the wafer

Taking the previous Table I's solution as an example, the chip A has a larger size and is set to the normal original chip thickness. However, chips B and C may require pre thinning due to their small size in order to perform better singulation. In actual operations, chips B and C may have different thicknesses (less than half thickness of other two chips), and

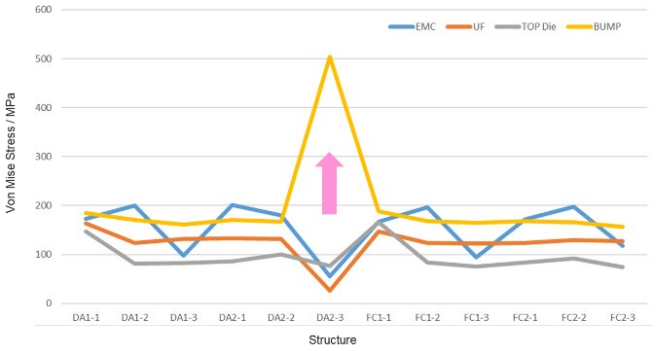
chips are covered with underfill creeping on the back of the chip (set the thickness of underfill 25um). Talble III is the combination of chip thickness and underfill coverage.

RESULTS AND DISCUSSION

A. Stress analysis between the layouts



(a)

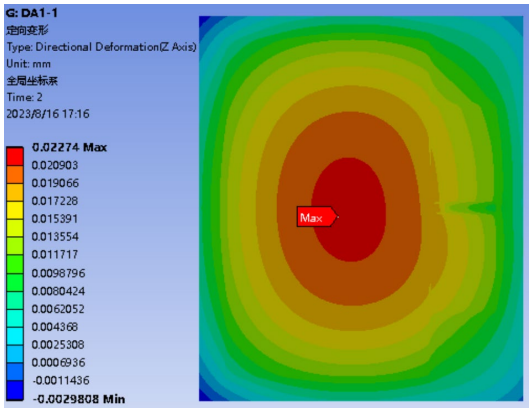


(b)

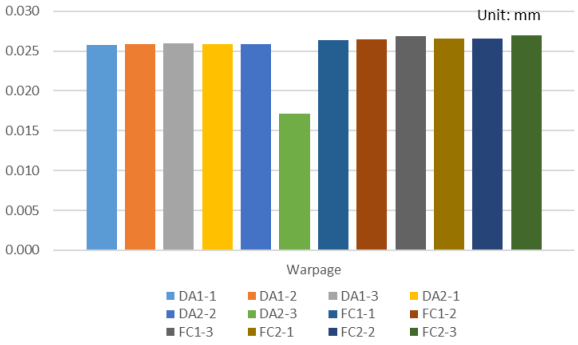
Fig. 5. Stress distribution by layer of different XDFOI-O layouts

Considering the situation in Figure 2, where there is cracking during the packaging process, it is necessary to pay close attention to the stress situation during chip layout. Generally, as the material gradually accumulates, the mismatch of CTE will cause stress generation. For this known possible anomaly, it is necessary to analyze the stress distribution of adjacent materials. Simulate the corresponding stress of the structure in Table II and summarize the stress of each layer. As the crack situation occurs on chip silicon, the chip, underfill, molding compound and the adjacent chip bumps are analyzed with emphasis. Fig.7 (a) analyzes the stress in each layer through peeling-off analysis of Structure DA1-1 as an example, and displays the all the structure results in Fig.7 (b). It can be seen that except for the structure of DA2-3, the stress difference between each layer is not significant under the same chip layout, which means that whether it is a die-attach or flip-chip method, the impact on stress tends to be consistent. DA2-3 has less stress in the top die, underfill and molding compound layers except bump layer, it can be explained that with the introduction of more polymer materials, more stress is concentrated on the bumps of the live chip, resulting in a stress blockage in stress transmission.

B. Warpage analysis between the layouts



(a)

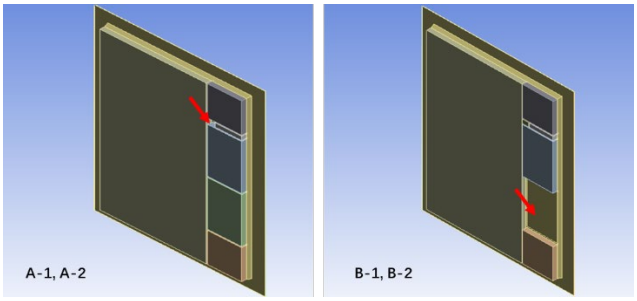


(b)

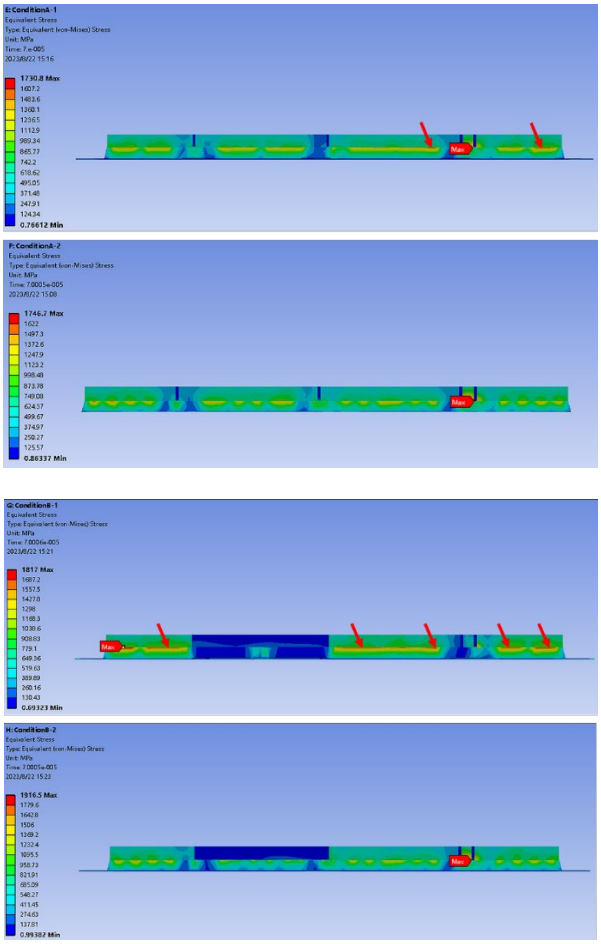
Fig. 6. Warpage distribution of different XDFOI-O layouts

The wapage data of different XDFOI-O packaging structures can be obtained from the Fig. 6, where Fig. 6 (a) is a typical schematic diagram of warpage simulation for DA1-1, and Fig. 6 (b) is a summary of specific layout warpage data. From this figure, the overall warpage difference of the packages is not significant in most cases, locating between 25 um and 30 um. However, there is a significant change in the warpage of the DA2-3 structure, with a decrease of approximately 30%. The explanation for this result can be attributed to the fact that the size of chip B is significantly larger than that of chip C, and its support capacity is stronger. Positioning chip B in the middle of the right side of the package can significantly increase the stiffness of the package, and with the addition of D-2, it can reduce the warpage. In addition, DA2-3 does not have a similar effect, possibly due to the larger CTE of die attach film. Underfill material combined with micro pillar bumps and silicon has a greater effect on the CTE mismatch with RDL interposer, resulting in a reduced ability to mitigate the warpage.

C. Effect analysis of chip thickness



(a)



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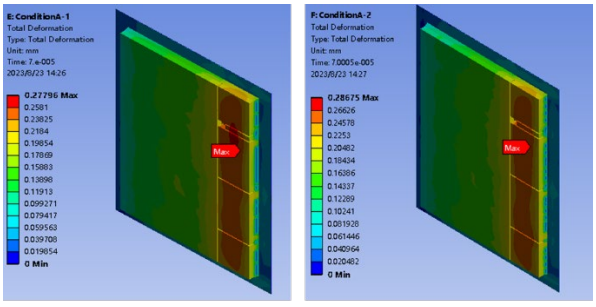

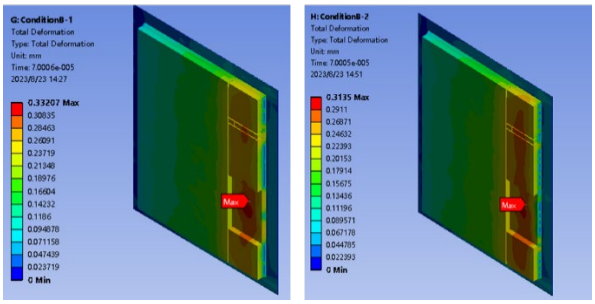

(c)

Fig. 7. Effect analysis of chip thickness in XDFOI-O layouts

Furthermore, based on the cracking phenomenon observed in the XDFOI-O structure during the process, corresponding dynamic analysis was conducted as Fig. 7 (a). Equivalent stress and total deformation results are shown in Fig. 7 (b) and Fig. 7 (c). In fact, in the actual thinning process, the grinding wheel and wafer rotate in opposite directions at a certain speed and angle. For the sake of model simplification, this simulation focuses more on the cause of chip cracking, and this condition has not been further set. Assuming that the grinding wheel presses towards the wafer at a certain speed and pressure, observe the changes in internal stress in the model during this process. From the results, it can be seen that with the application of grinding extrusion stress, normally the maximum stress concentration is distributed around the thin chip, which is consistent with the situation where chip cracking occurs at the thin chip during the process. When there is underfill creeping on the back of the thin chip, more servere stress and deformation spread around the thin chip as indicated in Fig. 7 (b) and Fig. 7 (c). From the material properties in Table IV, the elastic modulus of EMC or underfill is significantly lower than that of silicon materials, while for the encapsulation materials, EMC also has a much higher elastic modulus than underfill. In the cases, thin chips are encapsulted by more underfill materials, resulting in a significant increase in deformation and weakened support in this area during the thinning process. More stress will be added to surrounding silicon materials, leading to cracking of the chips located in this area.

CONCLUSION

This paper selects a chip size and thickness combination for XDFOI-O packaging, conducts stress and warpage analysis on different layouts, and simulates the subsequent wafer thinning process. Different chip bonding methods, except for the full use of die attachment, have similar warpage conditions. However, during stress analysis, the EMC, UF, and top die are subjected to relatively small stresses, with a large amount of stress concentrated in bumps. This creates some obstacles for the selection of this solution. Therefore, in actual production, more consideration should be given to the convenience of manufacturing, such as increasing manufacturing efficiency through repeated use of the same type of equipment, and stiffener chip sizes that are more convenient to pick and place.

During dynamic analysis, significant stress was found crowding around the thinner chip due to the smaller modulus of the polymer materials. Therefore, during package assembly layout, it is necessary to relocate the smaller and thinner chips to avoid excessive stress concentration in specific areas.

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