Optimized Die Preparation and Handling for High Yield Hybrid Die to Wafer Bonding

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Abstract

Hybrid Cu/dielectric bonding is a well-established technology for Wafer-To-Wafer (W2W) bonding, but it is challenging to apply this technology to Die-To-Wafer (D2W) bonding. Very small particles on the die or wafer can lead to voids/non-bonded regions. Processes to clean and activate wafers for hybrid W2W are quite mature, but it is very challenging to apply these to thinned and singulated dies for D2W bonding. To allow a (partial) re-use of the existing wafer level cleaning, metrology and activation processes and equipment, we propose a new concept where dies are being singulated, cleaned and activated on a glass carrier wafer. After the die preparation steps, the dies are directly picked from the carrier wafer. This approach does not involve additional pick & place steps and avoids the use of conventional dicing tapes. The first direct dielectric D2W bonding experiments using this new approach show a very promising bonding yield, with a high number of completely void-free bonded 50 µm thin dies. Additionally, by eliminating dicing tapes, thinned wafers and singulated dies are always supported by a rigid surface, enabling ultrathin die handling. In this study we also report the handling of dies down 10 µm thickness.

Key words

Carrier system, Hybrid bonding, Interconnects, Pick and place, Thin die

I. INTRODUCTION

Die To Wafer (D2W) bonding plays an important role in the production of heterogeneous and 3D integrated devices, as well as advanced packaging in general. Traditionally, solder micro-bump-based chip stacking is the process of choice for the assembly of products like High Bandwidth Memory (HBM), and other 3D and 2.5D (interposer) integrated devices. The micro-bump interconnect pitch of these devices is typically in the range of 50 to 40 µm.

Thermal Compression Bonding (TCB) is the preferred bonding technology for such small pitch interconnects. Conventional solder-based micro-bump interconnects in combination with a TCB process can be scaled down further to around 20µm pitch with existing processes and technologies [1]. New solutions such as the embedded bump TCB, can allow a further scaling of the micro-bump pitch to 10 µm and below, while still using a TCB process [2].

However, when the interconnect pitch decreases to values below 10 µm, TCB becomes increasingly difficult. TCB bonding equipment needs to achieve sub 1 µm post-bond accuracy, while applying fast heating and cooling rates combined with high pressure. Additionally, further scaling of solder-based bumps results in even higher bump aspect ratios and corresponding fragility. Finally, the high process temperatures can induce metal oxidation resulting in poor solder wetting. While traditionally flux or pre-applied underfills are used to reduce Cu and solder oxides, flux and underfill residues are becoming increasingly problematic for smaller bump pitches. Any residue entrapped in such a small solder joint can cause severe reliability issues.

Several flux-less bonding approaches such as bonding in inert or reducing atmosphere [3], metallic or organic capping and passivation layers [4] are proposed, but these typically further complicate the process or bonding equipment.

Because of the challenges related to very small pitch TCB, hybrid copper dielectric bonding is becoming an attractive alternative for sub 10µm pitch interconnects.

Copper bonding pads are embedded in a bonding dielectric and planarized to achieve very smooth and flat surfaces. After cleaning and activation of both chip and substrate surfaces, a room temperature bonding step is performed, typically followed by a thermal anneal to increase the final bond strength.

A room temperature bonding process allows higher placement accuracy and avoids the thermal oxidation issues seen associated with TCB. Furthermore, by using a short Cu to Cu interconnect instead of a tall Cu/solder joint, the interconnect resistivity decreases, resulting in lower power consumption. The dielectric/copper hybrid bonding process is already being used in volume production for several years in a wafer-to-wafer (W2W) mode. The best known example is the production of backside illuminated CMOS image sensors [5].
However, a direct transfer of a W2W hybrid/dielectric bonding process to a D2W process is not straightforward. Especially the cleanliness of singulated dies is critical. Since no solder or additional polymer layer in between the 2 surfaces is present anymore, any particle or foreign material will hinder good bonding. [6]. While wafer level cleaning activation and handling is relatively straightforward, performing the same steps on singulated dies is much more complex.

To mitigate the difficult and time-consuming die level cleaning, activation and handling, Collective Die-To-Wafer (CoD2W) hybrid bonding is proposed [7]. In a CoD2W process, the chips are first being accurately placed on a temporary carrier, which can then be handled, cleaned and activated. Finally, the dies are collectively bonded to the target wafer using conventional wafer level bonding equipment.
On the other hand, compared to the Direct D2W approach, CoD2W requires extra process steps and often expensive wafer level bonding equipment. Furthermore, the collective bonding step will introduce an extra misalignment component. Finally, only limited die thickness variations are allowed to achieve good CoD2W bonding yield. [7] [8]

Therefore, direct hybrid/dielectric D2W bonding is being investigated as an alternative for CoD2W. Different combinations of dicing techniques and cleaning concepts are suggested to increase the process yield. Blade dicing and stealth dicing often induce large amounts of particles [9], which can be mitigated by protection layers and process optimization [10] [11]. Other papers propose cleaner singulation techniques like laser and plasma dicing as well as combined approaches [12].
However, after any type of die singulation on dicing tapes, further cleaning, activation, handling and optionally inspection are required. While these process steps are typically well established on wafer level, it`s not always straightforward to apply these on diced dies on tape, and equipment options compatible with dies on tape are limited.Some papers propose the use of an intermediate carrier for cleaning and activation after die singulation on tape [13] [14] [15].

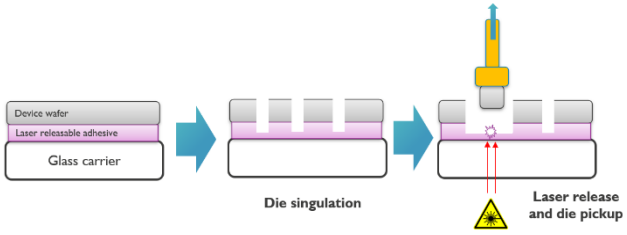

Figure 1. Pickup from glass carrier concept

This extra intermediate carrier implies the need for an additional die pick & place process. Furthermore, for very thin dies, pickup from dicing tape becomes challenging, and requires complex ejection systems and longer process time [16] [17].

This paper proposes a novel die preparation flow compatible with direct hybrid/dielectric D2W bonding. The approach is compatible with most dicing techniques and conventional wafer level equipment for die singulation, cleaning and inspection. Furthermore, this concept is promising for ultra-thin die handling, since the dies are at all moments supported by a rigid surface instead of a flexible dicing tape.
Figure 1 illustrates the proposed die handling concept. A (thin) wafer is transferred or directly thinned on a glass carrier wafer. Afterwards, the wafer can be further processed, singulated, cleaned and activated on the glass carrier, followed by direct pickup from the glass carrier.
To enable the pickup from a rigid glass carrier, we integrate a laser release layer between carrier and thinned wafer. Laser release is a fast and low stress process typically used for the debonding of temporary bonded wafers [18].

II. DIE HANDLING PROCESS FLOW

A. Process flow

Full thickness 300mm Si wafers are covered with a SiCN dielectric. SiCN gained a lot of attention as promising direct and hybrid bonding dielectric, because of a higher bondstrength at lower anneal temperatures, as well as improved Cu diffusion barrier performance compared to SiO_2 [19]. After SiCN Chemical Mechanical Polish (CMP) surface finish, the wafers are bonded to a temporary silicon carrier. Now the wafers are grinded to a thickness of 50µm, followed by a further thinning to 30, 20 and 10 µm by plasma etching for some of the wafers.
Since no (excimer-) laser source is integrated in a die bonding equipment, we propose a (wafer level) partial (laser) release step before moving to the die bonding step, as shown in figure 2.
To enable the laser release process step, the backside of the thinned wafer is coated with a ~2µm BrewerBond® T1107 laser release layer (LRL). This relatively thick LRL is selected to mitigate potential acoustic shockwaves that could damage the (ultra-) thin dies [20].

Afterwards, the thinned wafer is transferred to a glass carrier wafer, coated with a BrewerBond® C1301-50 temporary bond material (TBM).
Now the first silicon carrier is (mechanically) debonded, and the residual temporary bonding adhesive is stripped.
Finally, the thinned wafer is singulated into 7.2*7.2mm dies directly on the glass carrier, using a conventional blade dicing process.

B. Partial laser release optimization

The partial laser release process is performed using the SUSS XBC300GEN2 wafer debonder equipped with a LD300 excimer laser.
Finetuning this partial laser release process is essential. If the dies are completely released, the dies might drop from the carrier wafer during the laser release or transport to the die bonder. On the other hand, if the dies are not sufficiently released, it will be impossible to pick the dies by the vacuum pickup tool in the die bonder. Therefore, we need to determine the optimal laser fluence. The blade diced 50um thin 7.2*7.2mm^2 dies on glass carrier are used to optimize the partial laser release process. The laser fluence was varied, and the dies were afterwards picked in a BESI TC^{advanced} D2W bonder with a conventional vacuum pickup tool. Figure 3 depicts the results of the laser release optimization experiment. A laser fluence of 155mJ results in optimal residual adhesion where no dies drop from the carrier wafer, and >99% of the dies can still be picked.
Figure 4a shows a glass carrier with thin dies after the partial release process. Looking from the backside of the glass wafer, the part of wafer where the LRL was partially decomposed can be clearly distinguished from the non-treated part.

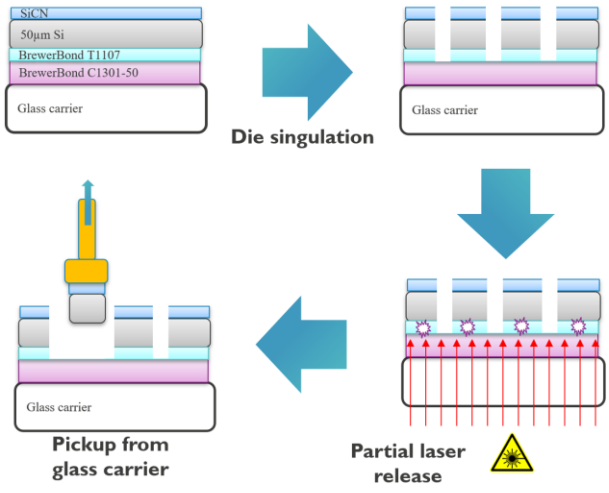

Figure 2. Pickup from glass carrier including partial laser release approach.

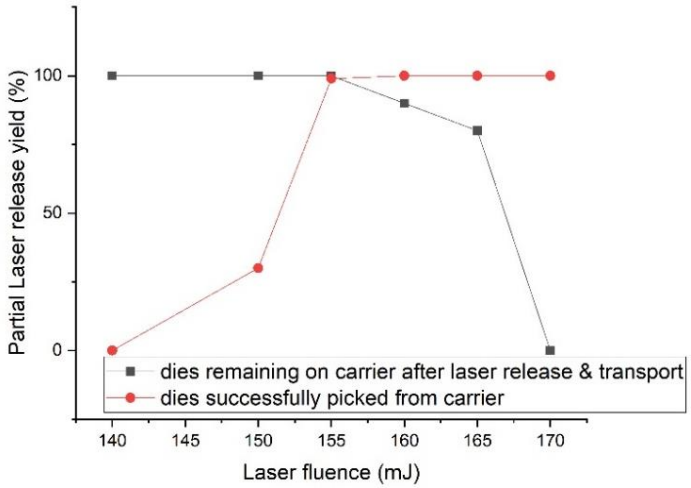

Figure3. Partial laser process optimization

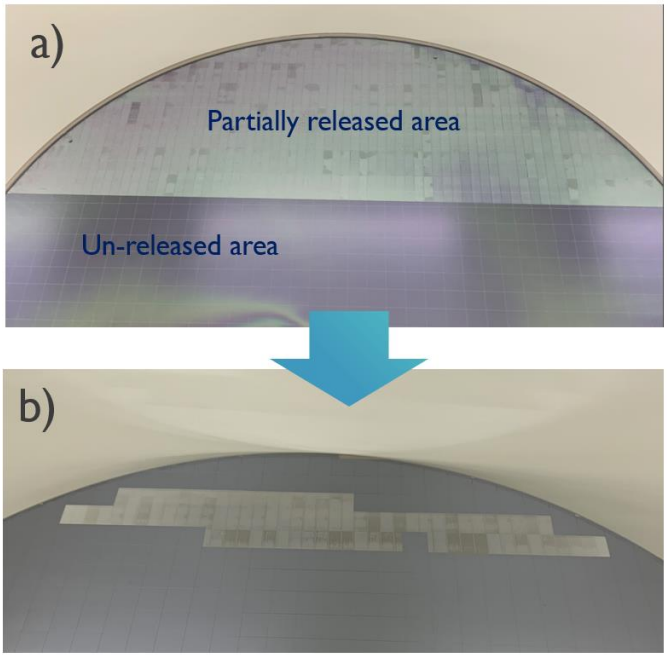

Figure 4. a) Wafer view through the glass carrier after partial release process. b) Wafer after pick & place of several dies

III. ULTRA-THIN DIE PICK AND PLACE

After optimizing the partial release process, pick and place tests are done with 50, 30, 20 and 10µm thin dies on glass carrier. The glass carrier is loaded into the BESI TC^{advanced} die bonder. The dies are picked with a conventional vacuum pickup tool, transferred to the bondhead, and finally bonded to a carrier wafer coated with a TBM.
Table 1 summarizes the results of the pick & place experiment. 100% pick & place yield was achieved for dies down to 20µm thickness, while <80% yield was obtained for

the 10µm thin dies. Figure 5a shows an overview of the dies with different thickness placed on the carrier wafer, while 5b shows a close-up image of a non-damaged pick and placed 10µm thin die.

However, we observe 2 issues for the 10µm thin die partial release and pick & place tests.
First, damage was observed on several of the 10µm thin dies after the partial laser release process.
Second, during the pick & place process, the thin dies are deformed by the vacuum of the pickup tool. This deformation on the pickup tool can be reduced by optimizing the pickup tool design, replacing the relatively large vacuum holes with much smaller holes or different vacuum patterns. Figure 6 illustrates both issues encountered with the 10µm thin dies.

The damage during partial laser release process is a more complex issue to solve. The damage is most likely caused by the acoustic shockwave during the laser ablation process, despite a relatively thick LRL. [20] This hypothesis is supported by the location of the defects, which matches the laser spot overlap area.
This acoustic shockwave induced issue could be mitigated by further optimizing the laser release parameters. A more convenient option would be to move away from the LRL to a more general UV release layer, which does not require an excimer laser but could be released with a conventional, small formfactor UV source (e.g. LEDs). This approach will avoid a shockwave generation and enable a release step fully integrated in the die bonder, without the need of a difficult and expensive integration of an excimer laser. This UV release layer should however be capable to withstand all wafer and die preparation processes, including die singulation, cleaning and activation, and potentially even dielectric deposition [21] and damascene processing [22].
Alternatives such as thermal release materials are less attractive since they are not compatible with higher temperatures during wafer/die preparation steps. Another downside of thermal release is the difficulty to selectively release a single die as horizontal heat dissipation is difficult to control.

Another potential contributor to thin die damage is the singulation process. Blade dicing typically creates chipping and small defects which decreases die strength. Therefore plasma dicing is expected to result in stronger dies and less damage and defects. [23] [24]

Table 1: number of damaged dies during pick and place test

Die Thickness (µm)	Nr. of dies damaged during pick and place process out of total amount of picked dies
50	0/9
30	0/45
20	0/45
10	2/24

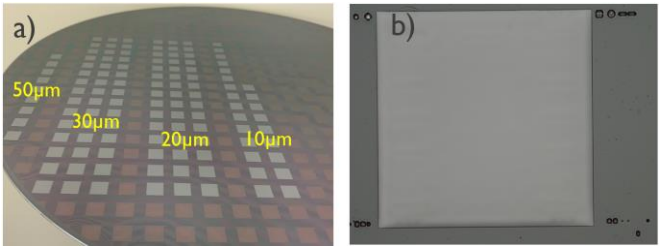

Figure 5. a) Thin dies from 50µm down to 10µm placed on a wafer. b) Close-up of a 10µm die placed on a wafer

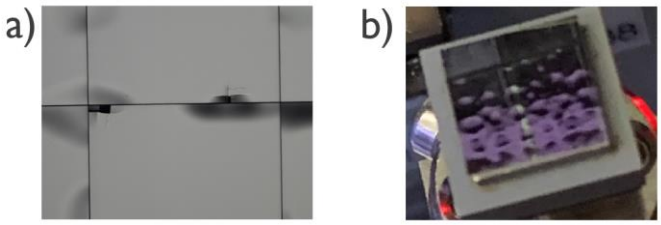

Figure 6. a) Damaged 10µm thin die on glass carrier after partial laser release process. b) 10µm thin die deformed by vacuum of pickup tool in die bonder

IV. DIRECT DIELECTRIC DIE TO WAFER BONDING

After process development and testing the concept of die pickup directly from glass carrier, the novel die handling approach is applied to direct dielectric bonding.
The thin die handling experiments as described in section III did not involve cleaning and activation of the dies. However, both die cleanliness and activation are vital to enable yielding direct or hybrid bonding.
To improve the incoming die cleanliness, the 50µm thin wafer is now plasma diced instead of blade diced. A lithography process defines the dicing lanes, followed by plasma etch and resist strip.
Just before the D2W bonding process, the dies on carrier are collectively activated by plasma and DI water rinse, immediately followed by partial laser release. At the same time, a blanket SiCN finished target wafer is also activated for direct dielectric bonding.

Finally, the thin dies are picked and bonded to the target wafer in the BESI TC^{advanced} D2W bonder.
In total 99 dies are bonded to the target wafer. All dies seem strongly bonded, as they all survive transport and Scanning Acoustic Microsocpy (SAM) inspection. Figure 8 shows the SAM inspection results of the direct bonded D2W assembly. Only small non-bonded areas can be observed, many dies are completely void free.
Image analysis of the SAM image reveals a total void free area of 98.5%. Figure 9 shows the bonded area per die for all bonded dies.
This is a promising result, especially considering the use a D2W bonder with standard tooling and no additional cleanliness measures, as well as the absence of an additional clean between resist strip and direct bonding activation steps. Further analysis of the voiding dies does not reveal a structural pattern, but rather random voiding as shown in figure 10. This suggests the voids originate from particles and defects, and not related to tool imprints.
Therefore, future experiments will focus on characterizing and improving the incoming die cleanliness, and the impact of the several process steps, especially the partial laser release process. Furthermore, the new BESI Chameo $^{Ultra\ Plus}$ die to wafer bonder, designed for high cleanliness direct dielectric and high accuracy hybrid bonding will be used for future direct D2W bonding experiments. [25]

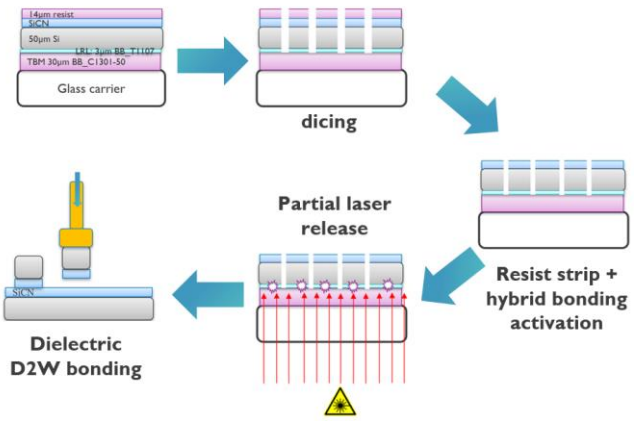

Figure 7. direct dielectric D2W bonding process flow

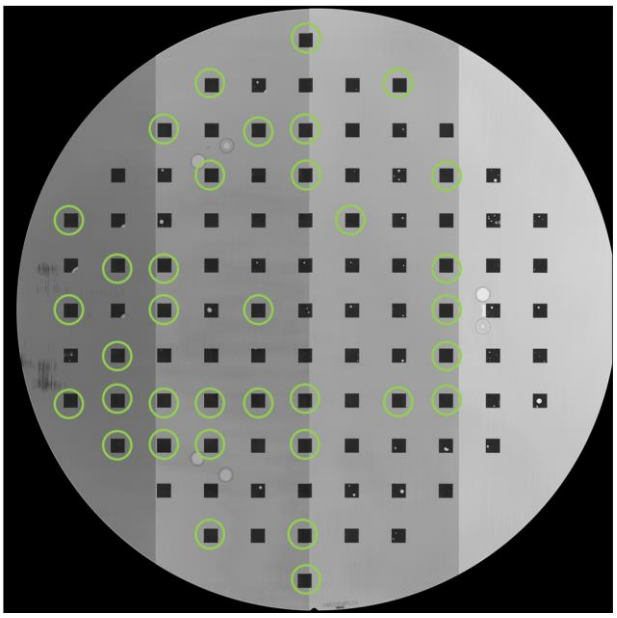

Figure 8. High-resolution SAM image of the direct D2W bonded wafer. Marked dies are completely void-free

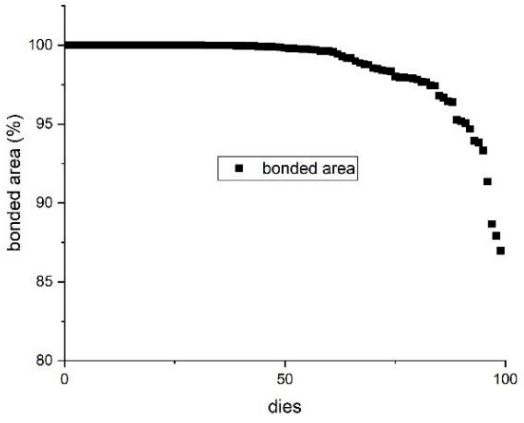

Figure 9. bonded area per die

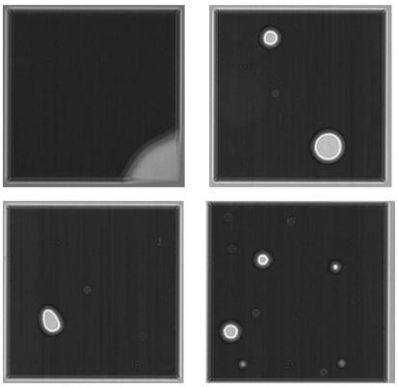

Figure 10. close-up SAM of random voiding dies

V. CONCLUSION

In this paper we propose and demonstrate a new process flow to enable thin die handling, suitable for dielectric or hybrid D2W bonding.

Conventional dicing tapes can be eliminated, leading to the possibility to use conventional wafer level equipment for die singulation, cleaning, metrology, and activation without having to pick and place the dies on a secondary carrier.

Ultra-thin dies from 50 down to 10 µm thickness could be successfully picked directly from a rigid glass carrier wafer. However, damage observed after the partial release process of the thinnest 10 µm suggests the current laser release process is too aggressive for these ultra-thin dies.

A potential improvement would be the use of an alternative release layer by using conventional (UV) light sources like LED`s. This approach would also allow an in-situ release in a die bonder, rather than relying on a separate partial laser release process.

The first direct dielectric D2W bonding experiment utilizing the new die preparation and handling concept shows promising results. SAM inspection results reveal many completely void free dies. Further analysis of voiding dies do not show a systematic voiding signature. This suggests that the voids originate from particles and defects rather than D2W bond tooling imprints.

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