Assembly of Large Flip Chip Die in Ceramic Packages

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Abstract

Hermetic packaging is required to ensure the reliability of processors and application specific integrated circuit (ASIC) chips that are used in strategic systems, whose operating lifetimes typically exceed thirty years. Performance requirements for emerging system applications are dictating the need for one thousand or more I/O, which precludes the use of wire bonded devices. These packaging requirements can be met by flip chip bonding die onto multilayer, high temperature cofired ceramic substrates. The hermetic environment is provided by a Kovar metal ring that is brazed onto the ceramic and sealed in the final assembly step, by welding on a metal cover. Several process and design requirements must be met to achieve high reliability flip chip assemblies. Reflowed devices must be free of flux residues because they are corrosive, provide a path for ion diffusion, are a source of moisture and degrade the adhesion of underfill to chip and substrate. Removal of flux residues by cleaning is problematic because the gap between chip and substrate is very small relative to chip area. A better approach is to bond chips without flux, as we do, by reflowing them in a formic acid environment.

An important reliability requirement for strategic hardware is the ability to sustain many cycles over extended temperature ranges. Temperature cycles induce plastic deformation in the solder connections as a result of stresses generated by the mismatch in thermal expansion coefficients of the chip and package. These stresses can be reduced significantly by underfilling the bonded chip with a filled adhesive. Choice of material as well as process execution impact the effectiveness of underfill enhancement of reliability. Optimization of both the physical design and composition of the solder connections is essential to producing reliable flip chip assemblies. We make extensive use of finite element analyses (FEA) in which we track the accumulation of plastic strain energy in the solder connections as they are subjected to temperature cycle induced stresses. Good correlations between the energy accumulated per cycle and the number of cycles to failure can be achieved if accurate state models of the solder are used. We have a catalog of Anand models for the solder compositions that we use in our FEA simulations.

One of the more challenging aspects of designing high performance flip chip packages is matching the size and pitch of the bond pads on the ceramic with those on the chip. Current devices use 90 micron diameter pads on 200 micron pitch, but newer designs are migrating towards 80 micron diameter pads on 180 micron pitch. It challenging to maintain tight tolerances on pad geometries in these higher density packages and to route all the additional signals. Thermal management is also an important component of the package design. Thermal vias and thermally conductive underfills are used to remove heat from the front side of the chip. On the backside of the chip, the gap between chip and cover is minimized and filled with a high thermal conductivity interface material. High fidelity FEA modeling is necessary to ensure that the chip can be adequately cooled in its hermetic environment. This paper discusses the impact of these design and assembly factors on the reliability of high performance, hermetically packaged flip chip assemblies.

Key Words:

Flip Chip, Hermetic Packaging , Co-Fired Ceramic , Reliability,

1. Introduction

Flip chip technologies are rapidly advancing, and present both unique advantages and challenges for use in hermetically sealed packages.

1.1 Reliability advantages of hermetic packaging

For high-reliability applications, evidence supports the advantages of a hermetically sealed package. Moisture and contaminants contribute to failure of an electronic device in numerous ways, including electrochemical migration (ECM), reactions with between ionic contaminants and water, radiation-induced degradation, and induced stresses.

Electrochemical migration It is well known that moisture causing failure in electronic devices due to ECM. ECM causes dendrite growth of metallics in the device, which then cause short circuits [1]. Growth of dendrites on devices exposed to moisture have been observed for many metals, including Sn, Pb, Cu, [2] [3]

Reactions between ionic contaminants and water A common source of ionic contaminants in microelectronic devices are epoxy resins used as molding compounds. Moisture interacts with these compounds in ways that can cause failure. First, as water diffuses into the resin, it expands the matrix, effectively acting as plastication. Water in the matrix hydrolyses chlorides, which then diffuse as hydrochloric acid. The hydrochloric acid causes failures both by formic electrolytic distances between electrodes and corroding aluminum [4] [5].

Radiation-induced degradation The presence of moisture or hydrogen in a package has significant impact on the device's radiation hardness. Both H_2O and H_2 have been shown to facilitate radiation-induced charge buildup, even in devices with nitride passivation. The voltage shifts observed are large enough to cause enhanced parametric degradation of an IC [6].

Induced stresses A lesser-documented failure mechanism is stress induced in a die due to adsorption of moisture by the substrate or underfill. Some evidence of significant die stresses due to humidity exposure have been reported [7], [8].

1.2 Effect of solder flux in hermetic packages

For most flip-chip technologies, a flux is applied at the connection interface to prevent oxidation during solder reflow. While the effect of flux on reliability of PCBs has been well-studied for the past 2 decades [insert refs], there is very little published about its impact on the reliability of flip chip die [insert refs], and nothing was found regarding flux-assisted flip chip assembly processes for hermetic packages. The little evidence present suggests incompatibility of flux residue with underfill could be a failure mode. Additionally, there are many unstudied failure modes which are theoretically possible.

Take, for example, how flux residues in a hermetic package could compound the detrimental effects of small amounts of moisture. MIL-STD-883 test method 1018 specifies 5000 PPMv of moisture to be permissible in the headspace, HS, of a hermetically sealed package, but this much water vapor can cause adsorption of multiple monolayers of water in many common package volumes [8]. The moisture concentration, C, threshold to form three monolayers of water as a function of headspace volume is [9]

$$C\,[PPMv] = 1295.5 \times HS[cc]^{-0.3341}. \quad (1)$$

The package presented in this paper has a headspace volume of approximately 0.6 cc, so equation 1 predicts a concentration above 22000 PPMv is sufficient to form a 3 monolayer coating of water within the cavity. Adsorption of a few monolayers of pure water on the surface of devices isn't often a cause of failure on its own because of very low conductivity. However, if hygroscopic contaminates are present, their ionization in water can cause a large increase in conductivity of those few monolayers. In turn, this increase can be enough to cause failure due to electrochemical migration [1].

2. Hermetic flip chip package

2.1 Package description

The package for the development of all the assembly processes needed to achieve a high reliability, high performance hermetic environment is shown in Figure 1. It is a custom designed, multilayer, high temperature cofired ceramic substrate that has over 900 I/O at a uniform pitch of 205 microns. In addition to the flip chip pads, the package also contains more than 30 chip capacitor pads for conditioning voltage rails that are supplied to the chip. The metallization/plating of the package is W + Ni + Au. A Kovar metal ring is brazed onto the substrate, which allows the die to be hermetically sealed by seam welding a metal cover onto the ring. Solder balls, reflowed onto pads on the bottom of the substrate, enable attachment of the package to a system circuit board.

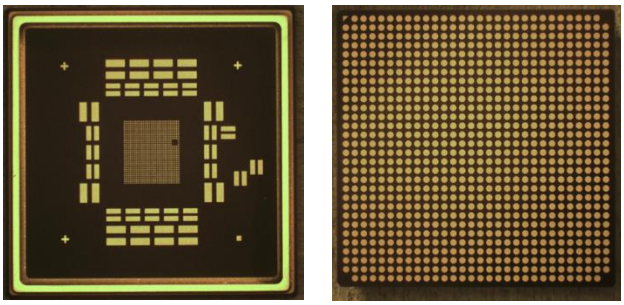

Figure 1. Internal view of package with metal pads and seal ring (left) and bottom view of package with the solder ball pads (right).

2.2 Assembly process

Die bonding Flip chip bonding is done using a Fineplacer femto2 from Finetech. It has the capability to heat both the substrate and the chip with temperatures exceeding 400°C. It also has a removable shroud that's serves as a chamber that gets placed to surround the heating plate and create an inert environment while doing thermocompression bonding. The shroud has three connections: an inlet where N2 can be flowed, another inlet where formic acid can be flowed in vapor form, and an exhaust for the whole chamber. A custom tool was needed to place the package accurately and precisely in the center of the heating plate. This custom tool is shown in Figure 2. The die is picked up and placed onto the package using tips dedicated for die bonding. The flip chip bumps composition is the eutectic 96.5Sn/3.5Ag solder. The reflow profile is designed based on this composition. The first step on the profile is to purge the chamber with N_2 to create an inert environment. After this is done, formic acid is flowed at 190°C for a couple of minutes to remove oxidation of the solder bumps. The quickest ramp up rate that the equipment can provide is used to reach a temperature above the melting temperature of our bumps which is 221°C, while still flowing formic acid. This volatilizes the formic acid complexed oxides while the chip and package are brought together. It is left at this temperature less than 30 seconds before cooling down to ambient temperature. Afterwards, the solder bumps are inspected, as shown in Figures 3 and 4, to ensure proper wetting unto the pads is achieved while being clean of oxides. More detailed discussion of the chemistry of formic reflow can be found in these references [9], [10], [11], [12].

Underfill After the chip is bonded onto the package, an epoxy based insulating material or underfill is applied using a pneumatic syringe dispenser. The package is heated to 60°C to lower the viscosity and to increase flow of the underfill.

It is then applied on two adjacent sides of the chip as to prevent voiding formation during flow. After the underfill propagates to the entire area under the chip, it is then cured for 2 hours at 165°C. The underfilled chip is shown in Figure 5.

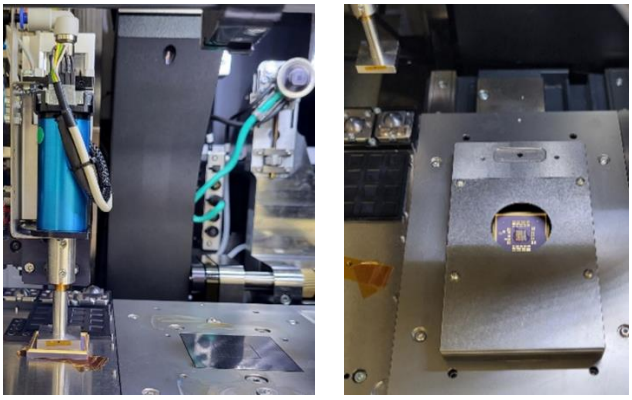

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Figure 2. a Custom tool picking up the package **b** package on heating plate with the shroud covering in place.

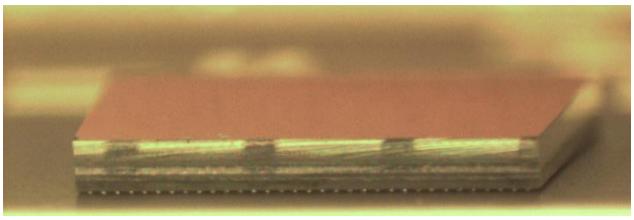

Figure 3. Side view of bonded die.

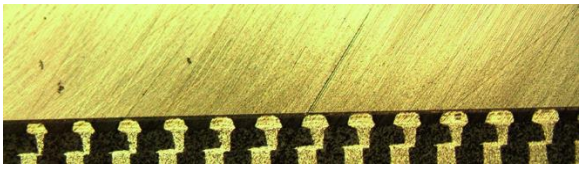

Figure 4. Cross sectional view of the bonded die.

Capacitor attachment The capacitors are attached using two types of epoxy, a non-conductive for structural integrity, and a filled conductive epoxy for electrical connections. Figure 6a shows the non-conductive epoxy applied between the capacitor bond pads. The epoxy is applied by dipping the tip of a wedge chisel tool into a drop of epoxy spread on a glass slide and then

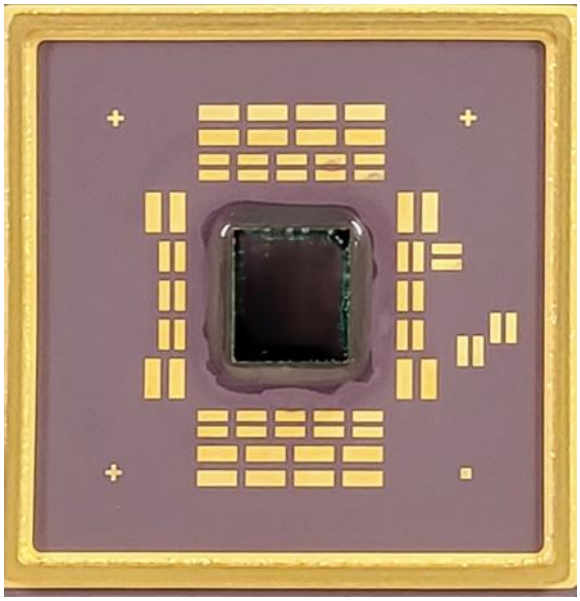

Figure 5. Die with underfill applied to it.

transferred by contacting the tool to the package surface. The chip capacitors are then picked and placed on the bond pads using a pair of tweezers. After placement, each capacitor is pushed down to insure it contacts the bond pads of the package. Images of the capacitors after placement are shown in Figure 6b. The non-conductive epoxy is partially cured at 150°C for 30 minutes. Pictures of the capacitors after this partial cure step appear in Figure 7a and show that there is no appreciable shift in their positions relative to initial placement. Finally, conductive epoxy is applied to the capacitor terminations and cured at 150°C for one hour to complete capacitor attachment. Images of the completed capacitor installations appear in Figure 7b.

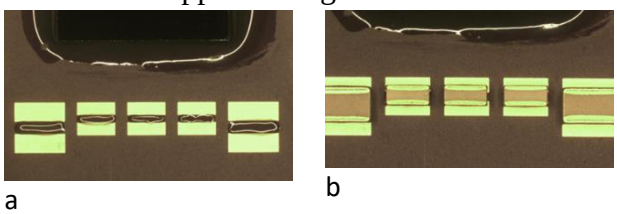

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Figure 6. a Dispense of non-conductive epoxy between pads **b** after placement of capacitors.

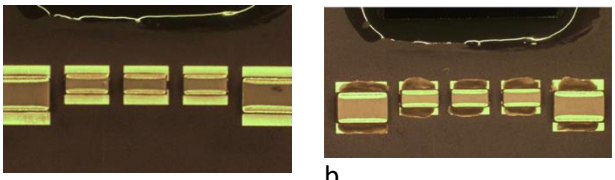

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Figure 7. a Capcitors after partial cure of non-conductive epoxy **b** after application and cure of conductive epoxy.

Thermal interface material After the curing of the capacitors, the thermal interface material (TIM) is applied before lidding the package. It is a diamond filled, electrically insulating and thermal conductive epoxy paste adhesive. The dispense is done manually with a syringe and a droplet is deposited on top of the chip, as shown in Figure 8a. Afterwards, the packaged is lidded applying downward force making the TIM spread uniformly unto the surface of the die. Since it is non-conductive, there is no concern for electrical shorting, thus the dispense doesn't have to be precise or accurate, as long as the whole surface of the die is completely covered. A fixture is needed to ensure proper constant force is being applied during the curing of the TIM. It is highly likely, that the TIM will expand during curing if not kept in place and lift the lid off from the seal ring, therefore affecting the sealing process and the hermetic requirement. The material is cured for 1 hour at 150°C. Figure 2.2.4.1 shows the fixture with a package in place.

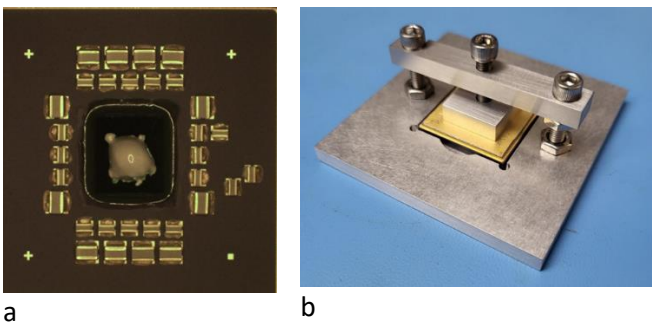

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Figure 8. a Droplet of TIM on top of the die **b** Custom fixture with lidded package

Seam seal After the thermal interface material between the die and package cover is cured, packages are immediately transferred to a bake out oven under nitrogen atmosphere set to a temperature of 60°C. The oven is attached to a Solid State Technology glove box that contains a Benchmark SM8500 seam sealer that is used to weld a cover on to the Kovar seal ring of the package. A custom nest, shown in Figure 9, is needed to hold the package for seam sealing. It is fabricated from G10 material to minimize thermal shock to the ceramic caused by the welding process. The seam sealing process creates a weld by flowing high current pulses through a roller in contact with one side of the cover through the seal ring, and out through a second roller in contact with the opposite side of the cover. The contact resistance between the cover and seal ring causes most of the power to be dissipated in the interfaces, heating the metal hot enough to melt it and form a weld. There are three distinct steps in the seal process. First, the rollers advance to the center of the package and contact the cover on its center line to create a pair of tack welds that hold the cover in position. Then the rollers move to the end of the package, reverse their direction of travel and move to the opposite side of the package to weld the first two sides of the cover. Finally, the nest rotates ninety degrees, and the rollers reverse direction again to weld the other two sides of the cover. A completed seal is shown in Figure 10.

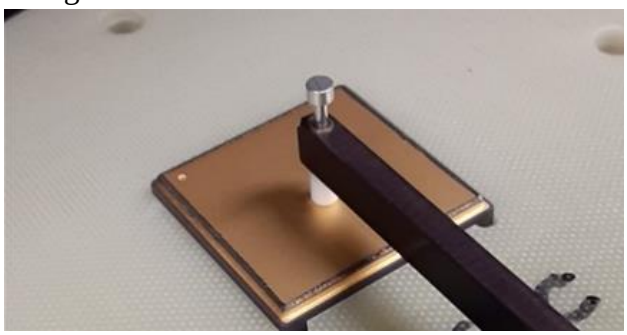

Figure 9. Package and cover in custom fabricated nest for seam sealing.

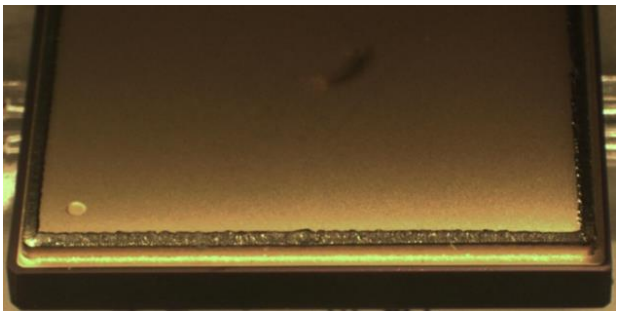

Figure 10. Perspective view of a portion of a welded cover which shows good quality seam weld.

Solder Ball attach In the final fabrication step, either solder balls or solder columns are attached to the bottom of the package. We describe the solder ball attachment process that is performed in house. Since 90Pb/10Sn solder balls are needed the recommended attachment method is a ball-drop approach. A ball-drop tool is needed since the solder balls are acting as "non-collapsible," therefore, solder paste is needed to attach the solder balls to the pads on the package. The tool system consists of an outer frame, to locate the inner nest along with the package, as well as a print and a ball-drop frame. The inner nest locates the package and it gets dropped into the center of the outer frame. The print frame holds the print foil and along with the outer frame it can align the apertures to the pads on the package for screen printing solder paste, as shown in Figure 11a. A small bead of solder paste 63Sn/37Pb is used with this stencil. A small squeegee blade is also provided with the tool set for the printing process. The ball-drop frame holds both the ball-drop foil as well as the ball-drop spacer, and along with the outer frame it can align the apertures to the pads/solder paste depositions on the package for the solder balls to be "dropped" onto, as shown in Figure 11b. After using the tool to place the solder balls, the package is moved onto a piece of perf-board and put into the reflow oven. The package is cool downed to room temperature, and then it is placed into a dish with a solvent cleaner .

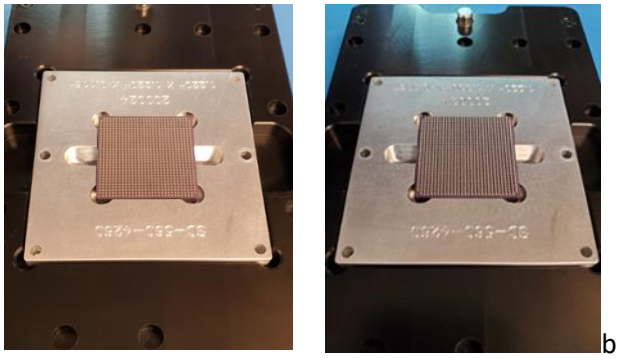

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Figure 11. a Package with solder paste **b** package with paste and solder balls pre reflow

It sits in the dish for a period of time, before gently brushing the solder balls with a soft bristle brush. After that, the process is repeated with IPA, before blowing it dry with an inline air-ionizer. The completed package appears in Figure 12.

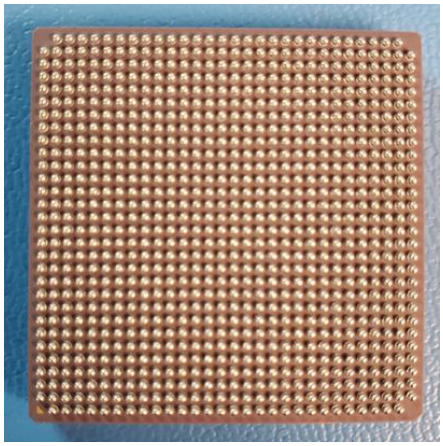


Figure 12. Solder balls post reflow and cleaned

3. Reliability Modeling

3.1 Solder Damage Models

Over the last several decades, many different models have been proposed to describe the failure of solder connections subject to cyclic mechanical loading. A comprehensive catalog of these models has been published by Su et. al. [13]. They divide the models into four categories based on, (1) plastic strain, (2) creep damage, (3)

energy dissipation, and (4) damage accumulation and provide in-depth discussion of their class features. For our reliability predictions, we utilize the energy dissipated per cycle, as proposed by Morrow, as the basis of our estimates [14].

Following Morrow's development, an expression for cycles to failure as a function of energy dissipated in each cycle, proceeds as follows. A hysteresis loop of shear stress, $\tau_{0'}$ and shear strain, γ_{P0} associated with a fatigue cycle is shown in Figure 13. The top, solid curve of the loop is described by a power function of the form

$$\gamma_{p0'} = \Delta\gamma_p \left(\frac{\tau_{0'}}{2\tau_a}\right)^{1/n'} \quad (2)$$

In which n' is the strain hardening exponent of the material, which has a value of approximately 0.15 for most metals. The area enclosed by the curve represents the energy, Δw that is dissipated during each fatigue cycle. It given by

$$\Delta w = 2\tau_a\Delta\gamma_p - 2\int_0^{2\tau_a} \gamma_{p0'} d\,\tau_{0'}$$

$$\Delta w = 2\tau_a\Delta\gamma_p \left(\frac{1-n'}{1+n'}\right) \quad (3)$$

Experimentally, it is observed that a log-log plot of plastic strain against fatigue life fits a straight line. The intersection of this line with the ordinate, $\gamma_{f'}$ is assumed to equal the strain at fracture of a monotonic stress-strain curve. The slope, *c* of the line ranges between -0.7 and -0.5 for most metals. These experimental observations can be expressed as a function of the form,

$$2N_f = \left(\frac{\Delta\gamma_p}{2\gamma_{f'}}\right)^{1/c}. \quad (4)$$

The cyclic plastic strain can also be written as a power function of the stress amplitude,

$$\frac{\Delta\gamma_p}{2} = \gamma_{f'}\left(\frac{\tau_a}{\tau_{f'}}\right)^{1/n'} \quad (5)$$

In which $\tau_{f'}$represents the stress at fracture of a monotonic stress-strain curve. Substitution of 5 into 4 yields

$$2N_f = \left(\frac{\tau_a}{\tau_{f'}}\right)^{1/b} \quad (6)$$

In which $b = n'c$.

Morrow's expression for cycles to failure as a function of energy dissipated per cycle is obtained by combining equations 3, 4 and 6, which yields,

$$(2N_f)^{b+c} = \frac{\Delta w}{4\tau_a\Delta\gamma_p}\left(\frac{c-b}{c+b}\right). \quad (7)$$

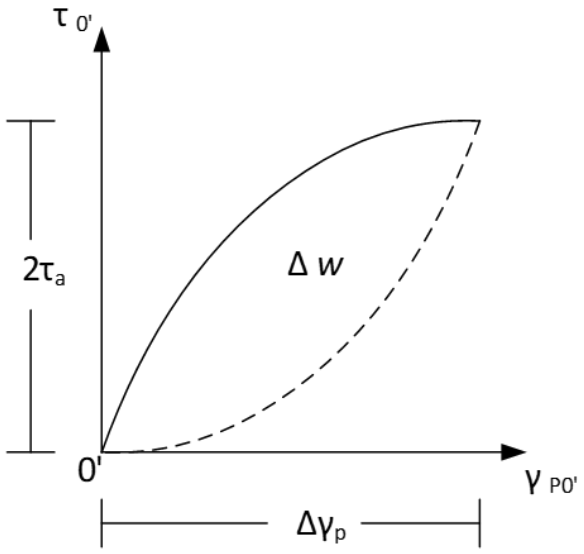


Figure 13. Construction used in derivation of energy accumulated in a fatigue cycle

3.2 Analytical Description

When the bottom pad of the solder connection shown in Figure 1 is fixed, while a shear force *F* is applied to the top pad, a displacement of ΔL results. Since the cross-sectional area of the solder connection is not constant along the z axis, both the shear stress and strain vary along z. If the solder connection is assumed to be spherical of radius *R*, then at height z, measured from the bump center, the cross-sectional area, *A*, is

$$A(z) = \pi r(z)^2 = \pi(R^2 - z^2) \quad (8)$$

The shear stress, τ, and strain, γ, are

$$\tau(z) = F/A(r) = F/\pi(R^2 - z^2) \quad (9)$$

$$\gamma(z) = \tau(z)/G \quad (10)$$

In which G represents the shear modulus. The shear displacement ΔL can be written as

$$\Delta L = \int_{-h/2}^{h/2} dl = \int_{-h/2}^{h/2} \gamma(z)dz$$

$$\Delta L = \frac{2F}{\pi G}\int_0^{h/2} \frac{dz}{(R^2 - z^2)} = \frac{F}{\pi GR}\, ln\left(\frac{R+z}{R-z}\right)\Big|_0^{h/2}$$

$$\Delta L = \frac{F}{\pi GR}\, ln\left(\frac{R+h/2}{R-h/2}\right) \quad (11)$$

By rearranging terms an expression for the force is obtained

$$F = \Delta L\pi GR/ln\left(\frac{R+h/2}{R-h/2}\right). \quad (12)$$

At the pad interface,

$$\tau(h/2) = F/\pi(r_p)^2$$

$$\tau(h/2) = \Delta LGR/ln\left(\frac{R+h/2}{R-h/2}\right)(r_p)^2. \quad (13)$$

$$\gamma(h/2) = \frac{\tau(h/2)}{G} = \Delta LR/ln\left(\frac{R+h/2}{R-h/2}\right)(r_p)^2 \quad (14)$$

$$\Delta w = \tau(h/2)\gamma(h/2) - 2\int_0^{2\tau_a} \gamma(\tau)d\tau \ .$$

$$\Delta w = G\left[\Delta L/ln\left(\frac{R+h/2}{R-h/2}\right)\right]^2 \frac{R^2}{(r_p)^4}\left(\frac{1-n'}{1+n'}\right) \quad (15)$$

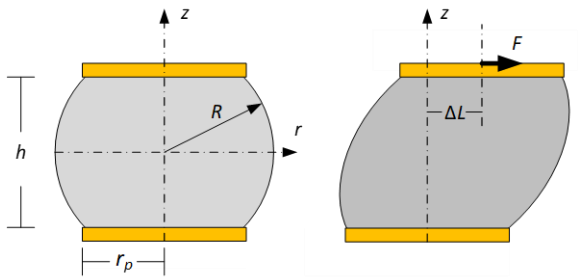


Figure 14. Solder connection in unloaded condition (left) and sheared distance ΔL by application of force F (right)

For equal diameter pads on the chip and substrate

$$R = \sqrt{\left(\frac{h}{2}\right)^2 + (r_p)^2}. \quad (16)$$

If it is assumed that the solder connections are arrayed on a square chip of edge length, l the corner connections would be subjected to the greatest shear strain so ΔL could be written as

$$\Delta L = \frac{\sqrt{2}}{2}\, l(\alpha_s - \alpha_c)\Delta T \quad (17)$$

In which α_s and α_c are the coefficients of thermal expansion of the substrate and chip with values of 6.5e-6 and 2.6e-6 [m/m ºC], respectively. The temperature range of the thermal cycle is ΔT.

Equations 16, 17, 15 and 13 were encoded in a spreadsheet program that was used to calculate cycles to failure. Some representative results are shown in Table 1 for different chip sizes, bump stand off heights, temperature ranges and solder compositions. The properties of the solders are listed in Table 2. In equation 6, the ultimate tensile stress value was used for τ_a, $1 + \%\, elong/100$ was used for $\Delta\gamma_p$, and a value of -0.3 was used for c.

Table 1. Analytical Model Parameter Values

l mm	r_p µm	h µm	R µm	Solder Alloy	ΔT ºC	ΔL µm	Δw MPa	N_f
12	45	50	51.48	A	100	3.31	32.9	2.08e2
12	45	50	51.48	A	50	1.65	8.23	1.82e4
12	45	75	58.58	A	100	3.31	20.8	9.08e2
12	45	75	58.58	A	50	1.65	5.21	7.96e4
16	45	75	58.58	A	50	2.21	9.26	1.24e4
16	45	50	51.48	B	50	2.21	24.4	2.84e3
16	45	75	58.58	B	50	2.21	15.5	1.25e4

Table 2. Solder Property Values

Solder Alloy	Composition wt %	E GPa	UTS MPa	Elong %	Hardening exponent	Ref
A	63 Sn/ 37 Pb	15.7	27.2	48	0.033	[15]
B	96.5 Sn/ 3.5 Ag	26.2	38.7	73	0.026	[15] [16]

3.3 Anand Solder Model

A significant short coming of our analytical model is that it does not incorporate the viscoelastic properties of solder. Consequently, its predicted number of cycles to failure is not dependent on either the extreme values of the temperature or its time duration. All commercial finite element codes provide various material models to support calculations in which the temperature or strain rate change over time. A material model that is well suited to solders, which tend to be used at temperatures in excess of half their homologous temperature is the Anand model [17] [18].

The Anand model for plastic deformation of metals at temperatures above half their absolute melting temperature, presumes that the time rate of plastic deformation, $\dot{\epsilon_p}$ is dependent upon applied stress, σ, absolute temperature, T, and a scalar isotropic flow resistance, *s*, which reflects the state of microstructural strengthening mechanisms, such as grain size, dislocation density, etc. The functional form of this relationship is,

$$\dot{\epsilon_p} = Aexp(\frac{-Q}{RT})[sinh(\xi \frac{\sigma}{s})]^{\frac{1}{m}} \quad (18)$$

in which A is a material dependent constant, m is the strain rate sensitivity, Q is an activation energy, ξ is a stress scaling factor and R is the gas constant. The flow resistance of the material changes over time in response to strain hardening and dynamic recovery processes. In the Anand model, the time rate of change of *s* takes the form,

$$\dot{s} = h_0[|1 - \frac{s}{s^*}|]^a sign(1 - \frac{s}{s^*})\dot{\epsilon}_p \quad (19)$$

in which h_0 and *a* are material dependent constants and *s** represents a saturation value of the flow resistance. The functional form of this saturation value is,

$$s^* = \hat{s}[\frac{\dot{\epsilon_p}}{A} exp(\frac{Q}{RT})]^n \quad (20)$$

in which $\hat{s}$ and n are constants. To find the value of the flow resistance at any time, its value, s_0 at time $t = 0$, must also be known. Thus, a total of nine constants are used in the Anand model to describe the plastic deformation of a metal. These constants are listed in Table 3.

Table 3 Anand Model Material Parameters

Symbol	Units	Description
A	sec^{-1}	Pre-exponential factor
Q/R	K	Activation energy divided by gas constant
ξ	none	Stress scaling factor
m	none	Strain rate sensitivity
h_0	Pa	Hardening / softening constant
$\hat{s}$	Pa	Coefficient for deformation resistance saturation value
n	none	Strain rate sensitivity of saturation value
α	none	Strain rate sensitivity of hardening
s_0	Pa	Initial value of deformation resistance

The determination of these coefficients requires a significant amount of experimental data along with a nuanced approach to fitting non-linear functions to the data. This methodology is described in papers by Motalab et. al and Wilde et. al. [19], [20]. In table 4, we list Anand parameter values for various solder compositions that were obtained from the literature.

3.4 Finite Element Calculations

Numerical estimates of temperature cycles to failure are made by creating solid models of the package assembly. When the solder connections are uniformly distributed over the die, the assembly is bisected by orthogonal planes that pass through the die center, to yield a one-quarter section to which boundary condition are applied as shown in Figure 15. The lower corner of the package is fixed in space and zero normal displacement conditions are applied to the faces that intersect the fixed point. For most analyses we do not explicitly model all the solder connections, but instead include 9 to 12 corner connections and represent the other connections by a continuous slab of material whose mechanical properties are the volume weighted properties of the solder and underfill.

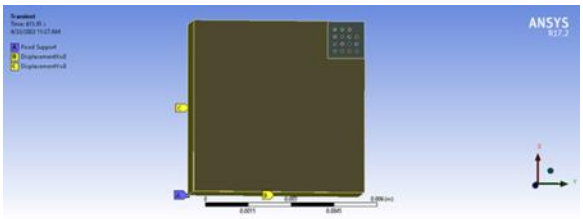


Figure 15. One-quarter model of a flip chip package assembly showing boundary conditions applied to corner and adjacent faces. The package is hidden in this view.

In this construction, only 11 corner solder connections are explicitly modeled. The others are represented by the slab of material that covers the rest of the die face. The material properties of the solder connections are represented by the appropriate composition dependent Anand model, while experimental TMA data is used to represent the temperature dependent modulus of the underfill material.

Prior to meshing the model, one or more volume slices of selected solder connections are defined. These slices are made adjacent to die and package interfaces and given a thickness of approximately one-twelfth the solder height. These slices are used to track the accumulation of strain energy in the solder connections during temperature cycling. Figures 16 and 17 show the stress distribution in the solder connections and underfill, respectively. The package is hidden from view in both images. Figures 18a and 18b show the distribution of strain energy and von Mises stress in a slice after four temperature cycles. Our usual practice is to subject the

assembly to four complete cycles and use the strain energy added in the fourth cycle to estimate cycles to failure. A plot of strain energy versus time for four temperature cycle appears in Figure 3.4.5.

Estimates of cycles to failure are made by inserting the energy accumulated per cycle into an equation obtained from a linear fit to log strain energy versus log cycles to failure data. A plot for 96 Sn/ 3.5 Ag/ 0.5 Cu solder, constructed from literature data, appears in Figure 20 [28], [29], [30], [31]. A similar plot is shown in Figure 21, for 63Sn/ 37 Pb solder [28], [29], [32].

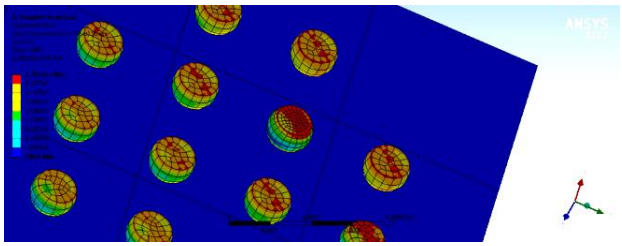


Figure 16. Von Mises stress distribution over solder connections after four temperature cycles. Both the package and underfill are hidden from view.

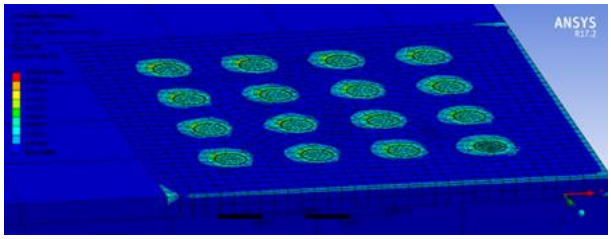
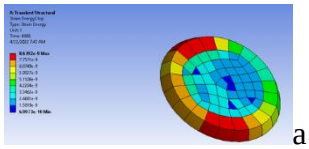


Figure 17. Von Mises stress distribution over underfill after four temperature cycles. The package is hidden from view.


a

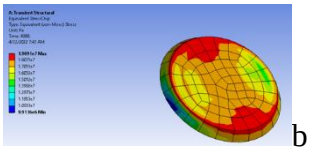

b

Figure 18. At the end of four temperature cycles (a) strain energy (b) stress in solder slice adjacent to silicon chip

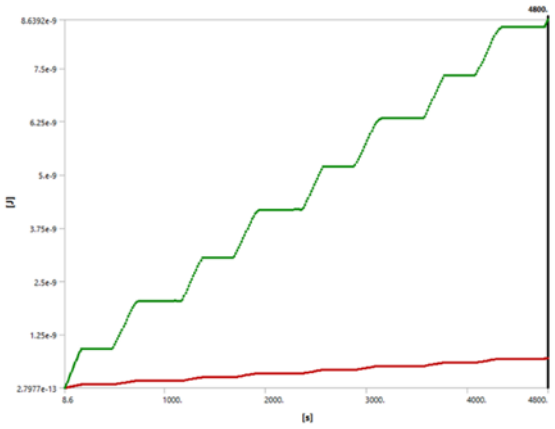


Figure 19. Strain energy accumulated in a solder slice during temperature cycles.

Table 4 Values for Anand Model Parameters Obtained from Literature

ANSYS constant	C1	C2	C3	C4	C5	C6	C7	C8	C9	
Solder Composition [wt %]	**s_0 [MPa]**	**Q/R [K^{-1}]**	***A*** **[sec^{-1}]**	**ξ [ ]**	***m*** **[ ]**	**h_0 [MPa]**	**$\hat{s}$ [MPa]**	**n [ ]**	***a*** **[ ]**	**Ref**
92.5Pb 5Sn 2.5Ag	33.07	1.102e4	1.052e5	7.00	0.241	1.432e3	41.63	0.002	1.30	[20]
60Sn 40Pb	56.33	1.083e4	1.490e7	11.00	0.303	2.641e3	80.42	0.0231	1.34	[21]
62Sn 36Pb 2Ag	12.41	9.400e3	4.000e6	1.50	0.303	1.379e3	13.79	0.070	1.30	[22]
62Sn 36Pb 2Ag	42.32	1.126e4	2.300e7	11.00	0.303	4.121e3	80.79	0.0212	1.38	[21]
95.5Sn 3.8Ag 0.7Cu	27.0	8.015e3	2.210e4	4.1	0.15	4.132e3	59.0	0.0154	2.0	[23]
95.5Sn 3.8Ag 0.7Cu nAl	39.5	8.710e3	2.430e4	5.8	0.183	3.541e3	62.3	0.019	1.9	[23]
95.5Sn 4Ag 0.5Cu	20.00	1.056e4	3.250e2	10.00	0.320	8.000e5	42.1	0.020	2.57	[24]
96.5Sn 3.5Ag 0.5Cu	16.33	9.096e3	3.518e3	4.0	0.188	1.600e5	24.64	0.015	1.79	[25]
96.5Sn 3.5Ag	39.09	8.900e3	2.230e4	6.00	0.182	3.321e3	73.81	0.018	1.82	[21]
97.5Pb 2.5Sn	15.09	1.558e4	3.250e12	7.00	0.143	1.787e3	72.73	0.00437	3.73	[21]
96.5Sn 3Ag 0.5Cu 63Sn 37Pb mixture	68.31	8.115e3	4.758e3	4.41	0.430	1.259e4	30.88	0.030	1.88	[21]
In	28.30	9.370e3	2.33e8	49.97	0.2985	0.0	28.3	0.0	1.0	[26]
80Au 20Sn	14.75	5.240e3	69.53	0.4	0.2598	2.760e4	27.11	0.0917	1.017	[27]

Table 5 Computed Cycles to Failure

Model	Die Size [mm]	Solder	Height [µm]	Underfill	Temp Cycle	ΔE [J/m^3]	N_{fail}
1	12x12	Sn/Ag	62	none	A	3.763e4	9.79e3
2	12x12	Sn/Pb	62	none	A	4.290e4	9.19e3
3	12x12	Sn/Ag	62	none	B	5.416e4	6.75e3

4	12x12	Sn/Ag	62	U1	B	3.383e4	2.35e4
5	12x12	Sn/Pb	62	U1	B	5.647e4	6.61e3
6	8x8	Sn/Pb	90	none	A	3.752e3	1.71e5
7	8x8	Sn/Ag	90	none	A	3.827e2	1.05e6
8	8x8	Sn/Pb	62	none	A	1.952e3	3.74e5
9	8x8	Sn/Ag	62	none	A	5.526e2	7.25e5
10	16x16	Sn/Ag	57	U1	B	5.484e4	6.66e3
11	16x16	Sn/Pb	57	U1	B	3.156e4	1.32e4
12	16x16	Sn/Ag	57	U2	B	3.092e4	1.19e4
13	16x16	Sn/Pb	57	U2	B	3.113e4	1.35e4

Temperature Cycles

A: -55 to +125°C, 300 sec dwell, 300 sec ramp

B: -55 to +125°C, 120 sec dwell, 10 sec ramp

C: -65 to +150°C, 600 sec dwell, 60 sec ramp

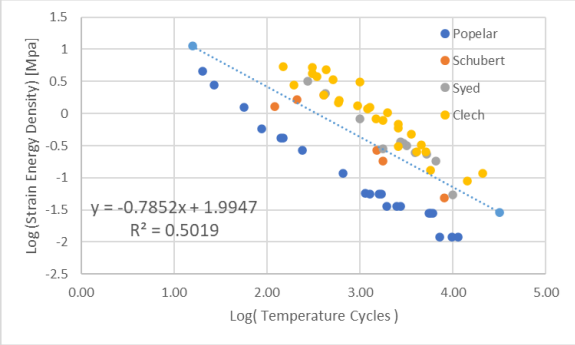


Figure 20. Correlation between calculated strain energy density per cycle versus measured cycles to failure for 96 Sn/ 3.5Ag/ 0.5 Cu solder constructed using literature data.

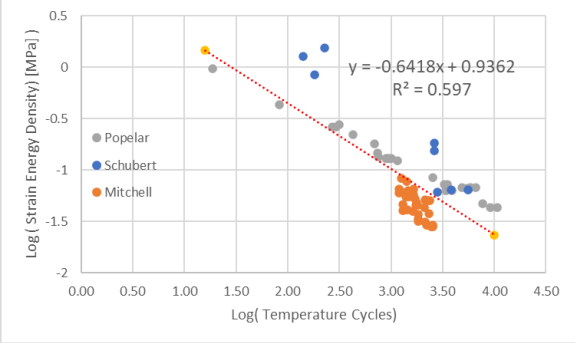


Figure 21. Correlation between calculated strain energy density per cycle versus measured cycles to failure for 63 Sn/ 37 Pb solder constructed using literature data.

In Table 5 we present computed cycle to failure to demonstrate the effect of die size, solder standoff height, underfill, solder composition and range and frequency. The measured modulus as a function of temperature is shown in Figures 22 and 23.

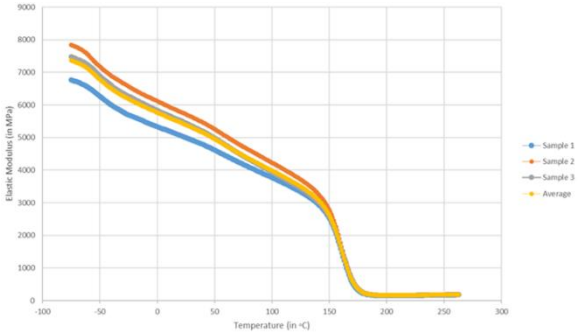


Figure 22. Modulus versus temperature of underfill U1

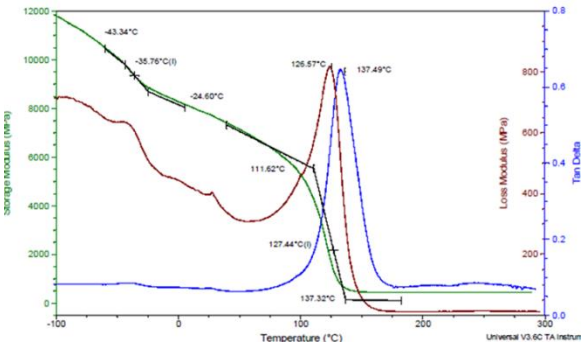


Figure 23. Modulus versus temperature of underfill U2

4. Thermal Management

Thermal management of hermetically packaged, high powered, flip chip devices is challenging because there are limited pathways for heat extraction from the die. Heat can be conducted away from the die face through the solder connections and underfill material. The thermal conductivity, ρ_s, of 96.5Sn/ 3.5Ag solder is 33 [W m^{-1} K^{-1}]. For N_s = 900 solder connections, 90 µm in diameter by h = 75 µm tall, the thermal conductance is

$$k_c = \rho_s N_s A_s / h = 2.5\ [W\ K^{-1}]$$

The thermal conductivity of the underfill material is $\rho_u = 2\ [W\ m^{-1}\ K^{-1}]$. For a square, l = 12 mm die, its thermal conductivity is

$$k_u = \rho_u\ (l^2 - N_s A_s)/h = 0.75\ [W\ K^{-1}]$$

The temperature drop between the chip and package is $\Delta T = Q/(k_c + k_u) = Q/3.25$ for a power dissipation of Q. At the package interface, heat flows through the package and solder columns that connect it to a circuit board. The thermal conductivity of the ceramic is $\rho_p = 14$ [W m^{-1} K^{-1}]. For a package thickness of t_p = 3 mm, the thermal conductivity is

$$k_p = \rho_p l^2 / t_p = 0.672\ [W\ K^{-1}]$$

Thermal vias can be added to the package to improve its thermal conductivity, but the number is limited because they reduce the number of signal routing channels that are available. Heat is conducted from the package to the board through the solder columns that join them. The columns are 0.4 mm in diameter by 2.2 mm tall and arrayed on 1 mm pitch. For a 12 mm square chip, the thermal conductivity of the solder columns, k_{sc} is

$$k_{sc} = \rho_s N_{sc}\, A_{sc} / h_{sc} = 0.434\ [W\ K^{-1}]\ .$$

The thermal conductivity from the die to the circuit board is,

$$k = 1 \Big/ \left[\left(\frac{1}{k_s + k_u} \right) + \frac{1}{k_p} + \frac{1}{k_{sc}} \right] = 0.244\ [W\ K^{-1}].$$

Heat can also be extracted through the back of the die into the package cover. The critical link in the heat flow path is the thermal interface material that fills the gap between the die and cover. These materials have thermal conductivities of 2 [W m^{-1} K^{-1}], so for a 0.25 mm gap between a 12 mm square die and cover this results in a thermal conductance of

$$k_{TIM} = \rho_{TIM}\, A_c / h_{TIM} = 1.15\ [W\ K^{-1}].$$

We have used a numerical model to examine the thermal performance of various heat flow paths for a 12 mm square chip bonded in a 30 mm square ceramic package and mounted on a test board compliant with the 1S2P board design from the JEDEC EIA/ 51-X Series Standards. Images of the solid model are shown in Figures 4.1a through 4.1c. Figures 4.2a and 4.2b show top and cross section views of the steady state temperature distribution resulting from 3 Watts of power dissipated in a package with just heat flow into the test board. Figures 4.3a and 4.3b show top and cross section views of the temperature distribution resulting from 8 Watts of power dissipation in a package with both heat flow into test board and forced convection cooling. The air flow velocity across the top of the package is 5 [m/sec]. Figure 4.4 shows a cross section view of the temperature distribution that results from 1 Watt distribution in a package with an aluminum plate attached to its cover. The edges of the plate are held at 22°C. A summary plot of the results of these calculations is presented in Figure 4.5. Chip temperature is plotted as a function of power dissipation for four case; 1) no convection, 2) natural convection, 3) forced convection at a flow rate of 5 [m/sec], and 4) conduction through an aluminum plate attached to the top of the package.

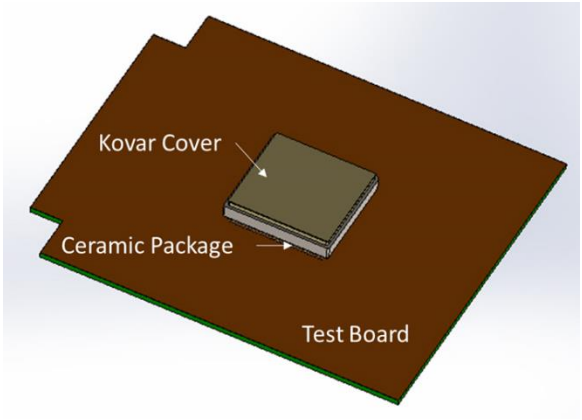


Figure 24. Ceramic package with Kovar cover mounted on thermal test board.

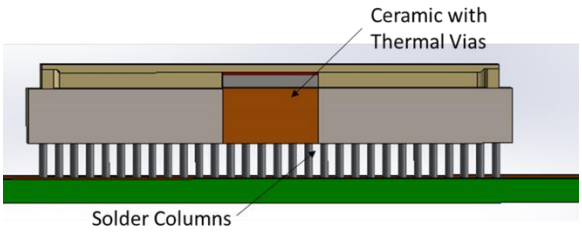


Figure 25. Cross section view of package mounted on test board.

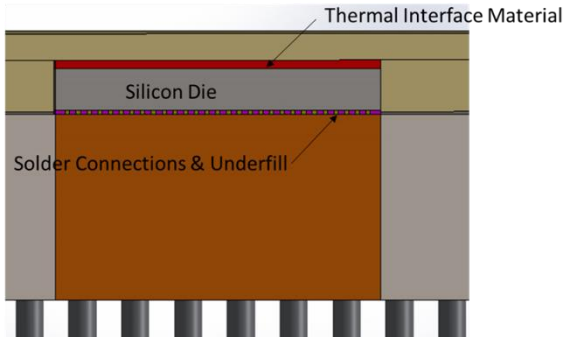
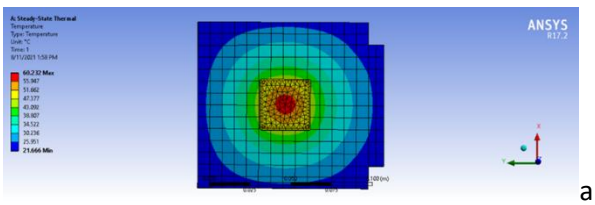
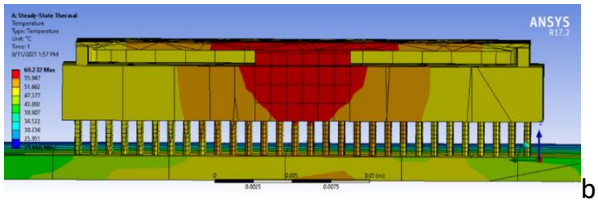


Figure 26. Magnified cross section view showing die attachment to package and thermal interface material on top of die.

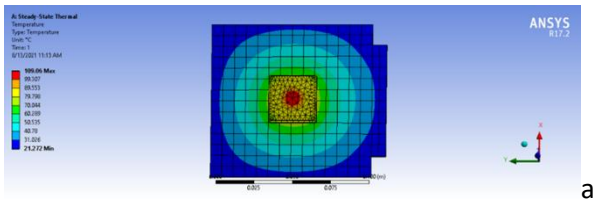


a

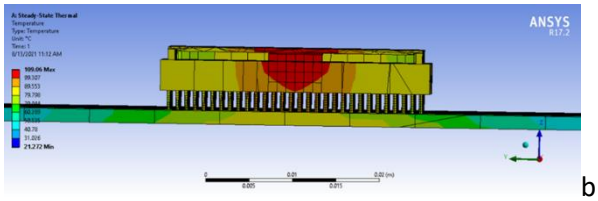


b

Figure 27. Top (a) and (b) cross section views of temperature distribution resulting from 3 Watts of power dissipation in package with heat flow only into test board.



a



b

Figure 28. Top (a) and (b) cross section views of temperature distribution resulting from 8 Watts of power dissipation in a package with both heat flow into test board and forced convection cooling.

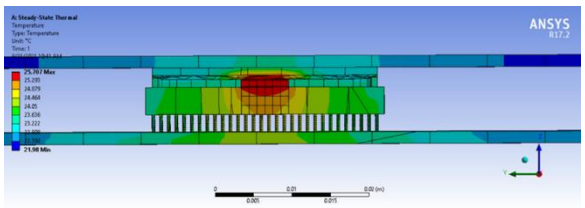


Figure 29. Cross section view of temperature distribution resulting from 1 Watt distribution in package with an aluminum plate attached to its cover. The edges of the plate are held at 22°C.

5. Discussion

There are many applications in which high device reliability over a service life of thirty or more years is of paramount importance. Hermetic packaging is a key technology for meeting this high reliability objective. In the introduction of this paper, we cite numerous published results that illustrate how corrosion, induced by

dissimilar metal contacts, reversion of crosslinked polymers, or low-level ionic contamination can cause device failure.

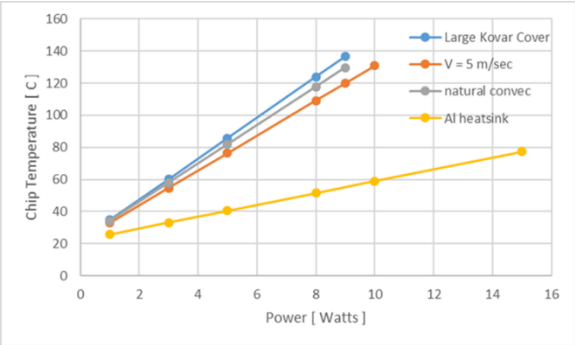


Figure 30. Summary plot of chip temperature versus dissipated power for configurations of heat extraction through circuit board (Large Kovar Cover), natural convection, forced convection (V = 5 m/sec), and heat conduction through top of package (Al heatsink).

It has also been shown that even at low humidity levels, a three-monolayer coating of water molecules on a device surface is thermodynamically stable and is thick enough to support electrical currents for galvanic corrosion.

We describe a packaging technology by which a high I/O flip chip device along with decoupling capacitors is bonded to a multilayer ceramic substrate. The device is underfilled to enhance temperature cycling performance. A metal cover is seam sealed to a Kovar ring, which is brazed onto the ceramic to create the hermetic environment. Our assembly process is straight forward and avoids the use of fluxes, which eliminates the need for cleaning processes and allows for extension to assembling large 2000 I/O devices.

An important part of the package design process is numerical modeling of the fatigue life of the flip chip solder connections, which is impacted by die size, composition and stand off height of the solder connections, underfill properties, as well as the in-service temperature cycle environment. We use an Anand model of a selected solder composition to calculate the accumulation of strain energy in a thin section of a solder connection that occurs during each temperature cycle. This value is then used in a solder specific correlation between strain energy and cycles to failure to estimate the fatigue life of our packaged device. This is an empirical estimate, but as we showed in the development of a simple analytical model, the approach can be directly related to a measurable stress-strain hysteresis loop of the solder.

Thermal management is another important design element of high reliability packaging. We showed that heat is most effectively extracted from flip chip devices by conduction through the package cover. Forced convection is the next most efficient means of removing heat from the chip, but that is not an option in many applications. The least effective heat extraction path is through the bottom of the package and into the circuit board via the solder connections. This is, however, the simplest scheme to implement and is viable for chips dissipating up to 5 Watts.

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