Electromigration of power devices part 2: power device in applications in controlled environment

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Abstract

In the power semiconductor industry, there is a continuous development toward a higher current capability of devices while device's dimensions shrink. Although higher current is preferred, the reliability risk of the electromigration (EM) remains challenging. In the present study, a special EM test vehicle is used to investigate the pure EM behavior of power device, following our previous work. The selection of the test condition is discussed in detail, which is defined based on the temperature and current profiles of the device in the actual application, focusing on the applications of the power devices in a controlled environment, i.e., data centers or telecommunication servers. The current and temperature profiles of the device are discussed based on the device's maximum power dissipation and its respective thermal design. The results show that the different combinations of currents and temperatures can lead to different ratios of acceleration factor between the temperature and the current. Consequently, an inappropriate selection of the testing condition can result in the over-domination of temperature over the current, leading to wrong conclusions. The effects of the PCB surface finish (both Ni and Sn plating) as well as different electron flow directions on the EM were studied. It is concluded that the maximum current that can be applied to a power device in the application within a controlled environment is rather limited by the cooling capability of the system than the EM induced device failure.

Key words

Electromigration, Application, power devices, solder joint.

I. Introduction

In the past years, the development of the power devices has been strongly driven in the direction towards higher current densities, thanks to the improvement of frontend wafer technology and the device miniaturization. The maximum current handling capacity of a device is primarily determined by two factors: the maximum power dissipation and the device's Rdson. For instance, the widely used Quad Flat No-leads (QFN) 5×6 power package, SSO8, is shown in Fig. 1a-c. If the system is designed to operate under a power dissipation of 10 W, a device with R_{dson} = 1 mΩ can handle a maximum current of 100A. This estimation is based on the power dissipation equation $P = I^2 \times R$. If there is an improvement in the technology that would lead to a 10% reduction in Rdson, it can result in a roughly 5.4% increase of the maximum current density without any modifications to the system. However, it is important to note that the failure of the Sn-Ag-Cu (SAC) solder joint between the device and the PCB board remains a significant reliability risk for the system, particularly under high temperatures and high currents [1-2]. The primary cause of this issue is the diffusion of Cu from the Leadframe (LF)/PCB trace into the solder. This leads to the prolonged growth of brittle intermetallic compounds (IMCs), specifically Cu_3Sn and Cu_6Sn_5, which ultimately results in the brittle failure of the solder joint. Additionally, the formation and coalescence of Kirkendall voids occur at the interface between Cu (LF or PCB trace) and solder, creating separation gaps in that region [3]. An elevated operating temperature intensifies the diffusion process, as indicated by the Arrhenius equation. Concurrently, the current flow induces an additional accelerated unidirectional diffusion mechanism known as electromigration (EM), propelled by the movement of electrons, often referred to as the electron wind [4]. In general, a current density of 10^3-10^4 A/cm^2, which corresponds to ~80 A for an SSO8 package shown in Fig. 1b and c, is sufficient to trigger the EM [6].

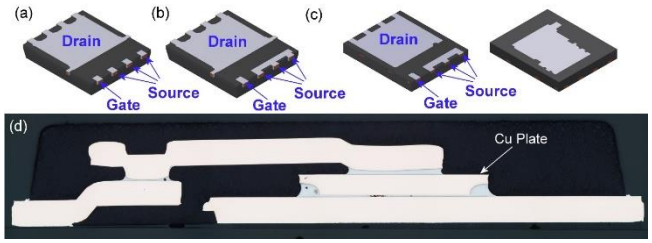

Figure 1. (a-c) different PQFN 5×6, SSO8, power packages: (a) standard source leads SSO8, used as EM test vehicle in the present study; (b) fused source leads SSO8 and (c) fused source leads SSO8 with exposed clip for top side cooling (top view on the right side); (d) Cross-section image of the special EM test vehicle. A Cu plate was used instead of the MOSFET chip to lower the electrical resistance of the device.

In one of our previous publications [1], we investigated the electromigration (EM) behavior of power devices using the SSO8 test vehicle depicted in Fig. 1b. In order to get as much acceleration as possible based on the Black's equation [5], we applied a current of 120 A and a temperature of 150°C to the test system, resulting in significant self-heating of the device. The elevated temperature created a thermal gradient between the device and the PCB, inducing thermal migration (TM) in addition to EM within the solder. It is crucial to note that during field application, there is almost no thermal gradient within the solder. This phenomenon can lead to the misinterpretation of test results. To address this issue, we utilized another SSO8 test vehicle shown in Fig.1a, where we replaced the metal-oxide-semiconductor field-effect transistor (MOSFET) chip with a Cu plate to reduce device resistance. Instead of applying stress to all three source pins, we focused on stressing the mid source pin with a relatively lower current of 40 A. This approach significantly reduced self-heating while maintaining a high current density within the stressed solder, specifically 1.8×10^4 A/cm^2 at 40 A.

In the current study, a comprehensive analysis of the electromigration (EM) behavior of the aforementioned test vehicle was conducted. As previously mentioned, the diffusion of Cu can lead to the extended formation of brittle intermetallic compounds, which may result in the brittle fracture of the solder joint under temperature cycling (TC) conditions. To avoid introducing complexity in data evaluation caused by TC, we maintained a constant test temperature throughout the study. Therefore, the conclusions drawn from this study are specifically applicable to devices operating under controlled and constant environmental conditions with minimal TC stress, such as data centers or telecommunication servers.

II. Experimental setup and analysis

Fig. 2a presents a photograph of an SSO8 device soldered onto the test board using SAC solder. The test board utilized in this study is a 3layers PCB with a thick Cu core. Two different surface finishes for the board are investigated: Sn and NiAu. The board design ensures that only the center 'source' pin and the drain pad carry the current. Fig. 2b showcases the 3D model of the electromigration (EM) test vehicle, with the 'source' pin having an area of 0.22 mm². For this study, the test current was fixed at 40 A, considering limitations of the testing equipment, thermal heating, and the maximum acceleration factor, which will be discussed in detail later. This current value results in a current density of 1.82×10^4 A/cm² at the source pin. Meanwhile, the current density at the drain pad is significantly lower at 2.33×10^2 A/cm², almost two magnitudes lower than that of the source lead. Two different current directions are tested: from the lead to the PCB and vice versa. This allows for an understanding of the electromigration behavior at different interfaces. Despite using a Cu plate instead of the MOSFET chip inside the package, we maintained the original nomenclature of the lead as 'source lead' and the large pad as 'drain pad' regardless of the current direction, to prevent confusion. The temperature of the board was regulated using a temperature sensor attached to the side of the device. Each group consisted of 10 tested samples. Cross-section samples were prepared by embedding the samples in the resin for mechanical polishing, followed by Ar ion milling [8]. This preparation method enables better visibility of the intermetallic compounds (IMC). Scanning electron microscope (SEM) and optical microscope were employed to capture cross-sectional images of the samples.

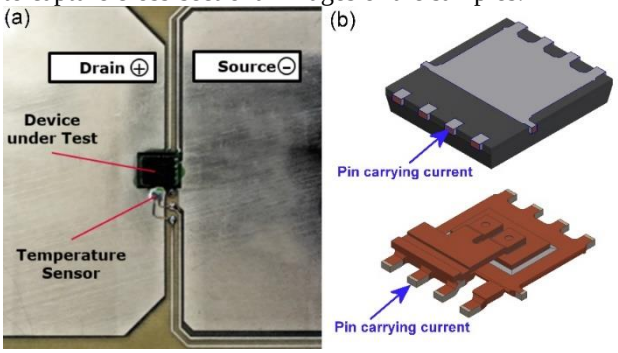

Figure 2. (a) A photo of the device soldered on the test board with temperature sensor attached; (b) Illustration of the pin of interest. Only the middle pin is connected to the board electrically and stressed under current flow.

III. Results and discussion

In order to determine the electromigration (EM) limit of the device within a reasonable stress time, it is crucial to carefully select the test conditions. However, it is important to ensure that the selected test conditions do not overly stress the components, as this may result in failure modes that are not representative of field application scenarios. The Black's equation, which is a widely accepted empirical model, is

used to describe the failure induced by electromigration.

$$Mean\ time\ to\ failure\ (MTTF) = \frac{A}{j^n} e^{\left(\frac{E_a}{kT}\right)} \quad (1)$$

where, **A** is a constant, ***j*** is current density, the current density exponent ***n*** is the model parameter, E_a is the activation energy, **k** is the Boltzmann constant and ***T*** is the absolute temperature in Kelvin. The system specific values for **A**, ***n*** and E_a can be obtained by fitting the experimental data of a given package-solder system. In one of our previous studies, we determined the values of ***n*** and E_a to be 1.7 and 1 eV, respectively, for the SAC solder system [7-8]. Apparently, current density ***j*** and temperature ***T*** are the main influencing factors with respect to EM. Consequently, the acceleration factor ***AF*** is calculated by:

$$AF = \left(\frac{j_{stress}}{j_0}\right)^n \times e^{\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_{stress}}\right)} \quad (2)$$

where, j_{stress} and T_{stress} represent the current density and temperature during the EM test, while j_0 and T_0 represent the current density and temperature during the field application of the device. It is important to note that depending on the stress conditions, the current density and temperature contribute differently to the overall acceleration factor. Mathematically, there are infinite combinations of current density and temperature that can achieve the same acceleration factor. As an example, let's consider an arbitrarily defined application with usage conditions of 5 kA/cm² and 85°C. Table 1 illustrates two different EM test conditions that both result in a final acceleration factor (AF) of 260. On the other hand, the current density of 5 kA/cm² corresponds to a current of 33 A for the SSO8 package depicted in Fig. 1a. If the device's lifetime is designed for 15 years (131,400 hours) in field application, subjecting it to 500 hours of EM stress would be sufficient to cover its expected lifetime. It is important to note that different test conditions yield varying contributions of current density and temperature to the final acceleration factor (AF). In this context, we define the portion of the acceleration factor attributed to current density as AF_j, and the portion attributed to temperature as AF_T.

$$AF_j = \left(\frac{j_{stress}}{j_0}\right)^n, \quad AF_T = e^{\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_{stress}}\right)} \quad (3)$$

In the case of a 'T dominated' condition, where temperature is the primary driving factor for acceleration, the high temperature of 150°C significantly influences the acceleration. The current density, although contributing to the acceleration, plays a lesser role compared to the temperature. Consequently, this type of test may not fully represent the device's EM behavior during actual application but can be considered more as a "biased high-temperature storage" test. On the other hand, in a "j dominated" condition, the high current density of 61 kA/cm² plays a more significant role in the acceleration compared to the temperature. However, achieving such a high current density in the test, which corresponds to a stressing current of approximately 400 A on the SSO8 package, poses technical difficulties and can result in substantial Joule heating even if the MOSFET is replaced with a Cu plate. Additionally, such a high current density can lead to failure modes that do not typically occur in the field applications [4]. It is worth noting that reducing the temperature in the "T dominated" condition (Condition 1 in Table 1) would increase the contribution of EM to the acceleration factor. However, this would decrease the overall acceleration factor, resulting in longer stressing times.

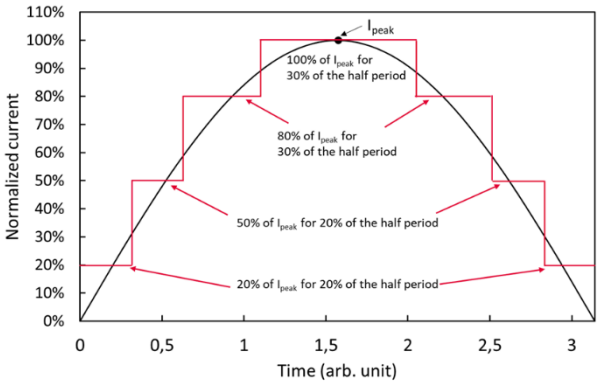

Figure 3. The sinusoidal waveform of the current through MOSFET (black curve) and its simplification (red lines)

To strike a balance between temperature and current density in defining the EM test conditions, it is crucial to have a clear understanding of the application conditions of the power devices. Considering the potential complications arising

Table 1. Example of the contribution of different testing current densities and temperatures on the acceleration factor

Conditions	j [kA/cm²]	T [°C]	AF_j	AF_T	AF_{total}	AF_j/AF_T
Application	5	85	-	-	-	-
Test condition 1 (***T*** dominated)	7	150	1.77	146.52	260	0.012
Test condition 2 (***j*** dominated)	61	100	70.50	3.69	260	19.12

from temperature shocks and the $I_{peak} = 0.25 \times I_{max}$

Table 2. Simplified current profile of the power device in server PSUs throughout its lifetime

Percentage of lifetime	Working hours scaled up to 15 years lifetime [h]	Percentage of I_{max}	Current [A]	Solder temperature [°C]
1%	1314	0%	0	50.0
4.0%	5256	5%	10.2	50.2
5.4%	7095.6	8%	16.32	50.5
8.0%	10512	10%	20.4	50.8
4.0%	5256	12.5%	25.5	51.3
2.0%	2628	16%	32.64	52.0
11.8%	15505.2	20%	40.8	53.2
14.0%	18396	25%	51	55
8.1%	10643.4	32%	65.28	58.2
22.1%	29039.4	40%	81.6	62.8
12.4%	16293.6	50%	102	70
3.0%	3942	64%	130.56	82.8
3.6%	4730.4	80%	163.2	101
0.6%	788.4	100%	204	130

formation of brittle intermetallic phases, the focus of our present study was on applications in controlled environments, such as power supply units (PSUs) in enterprise servers, data centers, and telecommunication servers. LLC resonant converters are commonly employed in server PSUs due to their high efficiency characteristics [9]. In the LLC circuit, the current flowing through the synchronous rectifier MOSFETs follows a sinusoidal waveform, as depicted by the black curve in Fig. 3. For the purpose of simplified calculations, we approximated this sinusoidal waveform with a step-like waveform, represented by the red lines in Fig. 3. Throughout the device's operational lifespan, the MOSFETs experience varying loads in the LLC circuit:

- 2% of the lifetime at full load, meaning $I_{peak} = I_{max}$
- 10% of the lifetime at ~80% of full load, meaning $I_{peak} = 0.8 \times I_{max}$
- 40% of the lifetime at ~50% of full load, meaning $I_{peak} = 0.5 \times I_{max}$
- 27% of the lifetime at ~40% of full load, meaning $I_{peak} = 0.4 \times I_{max}$
- 20% of the lifetime at ~25% of full load, meaning
- 1% of the lifetime at standby, which considered "no load"

To determine the exact current profile, it is crucial to define the maximum current (I_{max}) that the device can handle in the system throughout its entire operating lifetime, which we assume to be 15 years for server applications.

One of the key factors influencing the maximum current rating of a power device is the heat dissipation capability of the system, represented by the thermal resistance-to-ambient (R_{thJA}). A lower R_{thJA} value allows for a higher maximum current rating for the same device. In this study, the focus was on the double-side-cooled (DSC) SSO8 package (Fig. 1c) with liquid cooling on a heatsink to define the I_{max} for the SSO8 package in a power supply unit (PSU) application. The R_{thJA} value was determined through thermal simulation using a 3D model shown in Fig. 4a. The DSC SSO8 package was mounted on a 2s2p JEDEC FR4 board with 70% Cu. A heatsink with dimensions of (15 × 15) mm² was attached to the top of the device using a 100 µm thermal interface material (TIM) layer (thermal conductivity: 3.0 W/(m·K)) between the device and the heatsink (not shown in the drawing). The heat transfer coefficient at the top of the

heatsink was set to 6000 W/(m²·°C), representing liquid cooling. The temperature distribution of the device with 1 W power dissipation is depicted in Fig. 4b, from which the R_{thJA} value was calculated to be 3.85 K/W. In PSU applications, the average ambient temperature is approximately 50°C, and the maximum allowed temperature for the PCB is 130°C due to material constraints and reliability considerations. Considering the low thermal resistance between the chip and the PCB solder, we assumed a maximum allowed operating junction temperature (Tj) of 130°C for the device during application. It is important to note that the maximum operating Tj is typically lower than the Tj declared in the product datasheet due to device derating guidelines in IPC9592. The maximum current (I_{max}) is thus calculated using the following equation:

$$I = \sqrt{\frac{\Delta T}{R_{thJA} \times R_{dson}}} \quad (3)$$

Here, ΔT=80K is the temperature differences between the junction and ambient, in this case; R_{dson} represents the resistance of the device when it is fully switched on. For 40V device employed in the PSU, the state-of-the-art R_{dson} of the best-in-class product is ~0.5 mΩ. The maximum allowed current is thus calculated to be 204 A, corresponding to 112 A/mm². The current and temperature profiles are summarized column 2, 4 and 5 in Table 2. Using the provided data, we can calculate the acceleration factors (AF_T/AF_j) for the current EM test at different temperatures, as listed in Table 3. At a test temperature of 150 °C, the AF_T/AF_j ratio is determined to be 22.5, indicating that temperature has a dominant effect on the acceleration. At temperatures of 125°C and 110°C, the AF_T/AF_j ratios are 4 and 1.2, respectively, indicating a more balanced contribution from temperature and current in the acceleration. Considering the longer required stress time at 110 °C, the EM test was conducted at 125 °C with a current density of 1.8×10^4 A/cm². This ensures a minimum testing time of 782 hours, which is necessary to cover the 15-year server application.

Table 3. Contribution of the different testing temperatures on the acceleration factors

j [kA/cm²]	T [°C]	AF_{total}	AF_T/AF_j	Required stress time [h]
1.8×10^4	110	53.6	1.2	2453
1.8×10^4	125	168.0	4	782
1.8×10^4	150	943.4	22.5	139

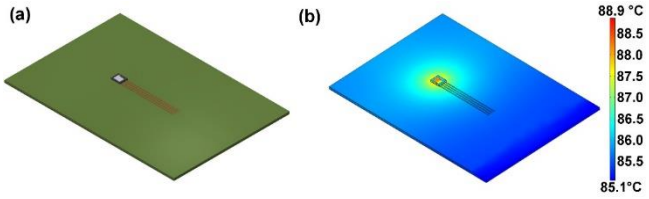

Figure 4. (a) 3D model of the DSC SSO8 on 2s2p JEDEC board; (b) temperature distribution of the system with 1W power dissipation, TIM and heatsink are not shown.

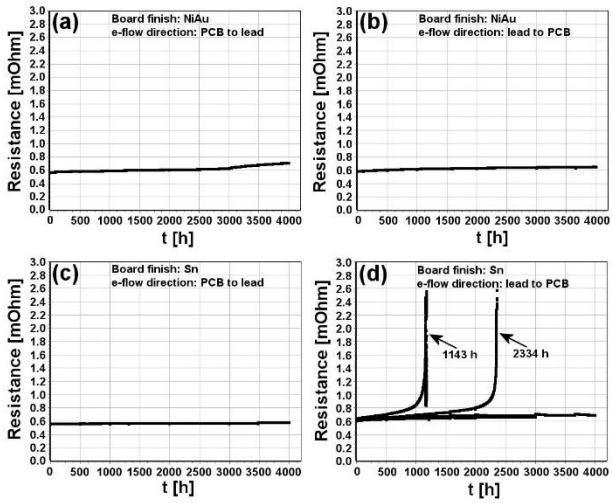

Figure 5. Electrical response of the EM test vehicle at a test condition of 125°C and 40 A. (a) PCB surface finish: NiAu, electron flow direction: PCB to lead; (b) PCB surface finish: NiAu, electron flow direction: lead to PCB; (c) PCB surface finish: Sn, electron flow direction PCB to lead; (d) PCB surface finish: Sn, electron flow direction: lead to PCB

Fig. 5 shows the typical electrical responses of the devices in different groups during a testing period of up to 4,000 hours. For the NiAu plated board, no electrical failures are observed within this timeframe, regardless of the electron flow directions. Similarly, for the Sn plated board, no failures are observed in the group with electron flow from the board to the lead. However, in the group with electron flow from the lead to the board, the first failure occurs at 1,143 hours, followed by a second failure at 2334 hours. No further failures are observed in this group for the remaining devices. As mentioned earlier, a testing duration of approximately 782 hours is required to cover the mission profile of the device in the server applications. Hence, all four groups in the present study meet the requirement for a 15-year lifetime. To examine the microstructure of the solder, cross-sectional inspections were performed on the samples after 2000 hours of testing, as shown in Fig. 6. The arrows indicate the direction of electron flux. In all groups, a significant growth of the IMC is observed in the solder under the source leads (referred to as 'source solder'), while the solder under the drain pad (referred to as 'drain solder') shows less

pronounced growth. This finding is expected since the source and drain solders experience different current densities: 1.82 × 10^4 A/cm^2 for the source solder and 2.33 × 10^2 A/cm^2 for the drain solder. The higher current density in the source solder leads to more prominent electromigration-induced diffusion in that region.

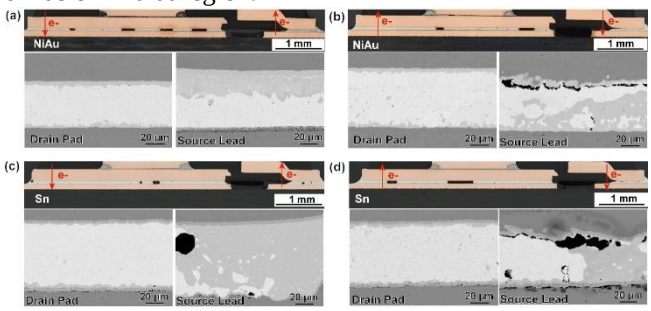

Figure 6. SEM images of different groups after 2000 h EM test @125°C and 1.82×10^4 A/cm^2: a) NiAu plated board, electron flow from board to source lead; b) NiAu plated board, electron flow from source lead to board; c) Sn plated board, electron flow from board to source lead; d) Sn plated board, electron flow from source lead to board.

A comparison of Fig. 6a and 6b allows for the study of the influence of electron flux direction on the Ni plated board. In the case of the drain solder, which primarily experiences high-temperature-induced diffusion due to the low applied current density, no significant differences are observed between the two electron flow directions. However, for the source solder in Figure 6a, extended formation of the intermetallic phase near the leads is observed, while the intermetallic phase forms closer to the board in Figure 6b. To identify the composition of the intermetallic phase in the solder joint, elemental mapping of Cu, Ni, and Sn using Energy Dispersive X-ray spectroscopy (EDX) was conducted, and the results are presented in Fig. 7. Different regions with distinct elemental distributions are observed. In the case of electrons flowing from the board to the lead (Fig. 7a), a Cu-Sn intermetallic phase forms directly adjacent to the Cu lead, followed by the Ni-Sn intermetallic phase. A clear boundary between the Cu-Sn and Ni-Sn phases is shown with the dashed line. On the board side, a porous Ni layer and a thin Ni-Sn IMC are present. The Ni layer acts as a barrier to prevent Cu diffusion into the solder, and during the current EM test, the electron flux primarily drives the diffusion of Ni atoms from the Ni layer into the solder. The dissolved Ni migrates towards the Cu lead under the continuous electron flux, leading to the formation of the Ni-Sn intermetallic phase. Consequently, the Ni coating becomes porous. In the case of electrons flowing from the lead to the board (Fig. 7b), enhanced formation of the Cu-Sn intermetallic phase is observed near the board surface. Additionally, regions with different Cu and Sn contents exist, allowing for the identification of the intermetallic phase composition. The region directly adjacent to the lead is identified as Cu_3Sn, exhibiting the highest Cu content. Next to this region, the Cu_6Sn_5 IMC is present, followed by voids known as Kirkendall voids [10]. Kirkendall voids form due to the high concentration of vacancies at the Cu/Cu_3Sn interfaces, which leads to different diffusion rate of the present elements. The diffusion of Cu leads to the coalescence of these vacancies, resulting in void formation [10]. On the board side, Cu_6Sn_5 IMC is identified, and no voids are observed in the Ni layer. This observation is expected since the electron flux drives Cu diffusion from the leads to the board.

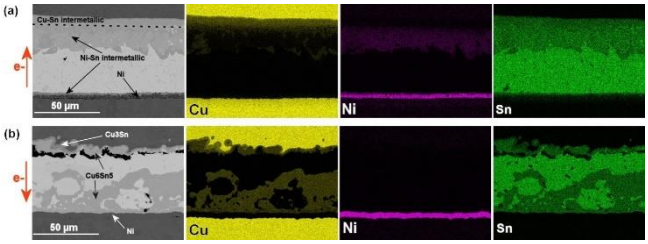

Figure 7. EDX mapping of the source solder on NiAu plated board. The direction of the electron flux is indicated by the arrows.

comparing Figure 6c and 6d, the influence of electron flow direction on the Sn plated board can be examined. Similar to the Ni plated board, no significant differences are observed in the drain solder. However, Kirkendall voids are observed in the Cu-Sn IMC in the drain solder adjacent to the board, while no voids are observed in the interface next to the drain pad. This is in contrast to the Ni plated board (Fig.6a and 6b), where no Kirkendall voids are observed at either interface in the drain solder. The presence of organic impurities introduced during the PCB Sn plating process is responsible for this phenomenon. These impurities can serve as nucleation sites for voids when Cu diffuses into the solder, resulting in the formation of Kirkendall voids [11]. This occurs even under thermal aging conditions alone. Consequently, Kirkendall voids are observed in the drain solder near the board, regardless of the direction of electron flux. In addition to the observation of Kirkendall voids, differences in the thickness of the intermetallic phase below the drain pad are noticed, with Figure 6d showing a slightly thicker Cu_6Sn_5 phase. This can be attributed to the slightly enhanced Cu diffusion induced by electromigration. However, the effect of electromigration on the IMC thickness is minimal due to the low current density, as expected.

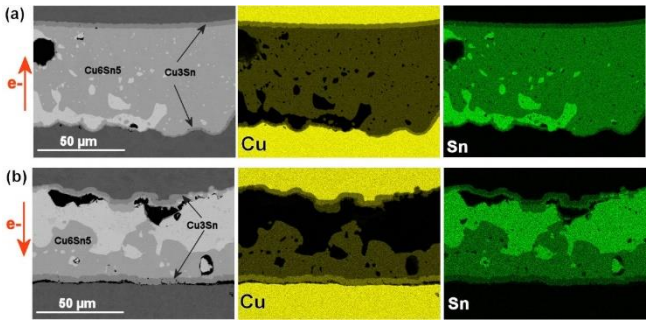

Figure 8. EDX mapping of the source solder on Sn plated board. The direction of the electron flux is indicated by the arrows.

Similar to the Ni plated board, the source solder also exhibits extended formation of intermetallic phases. EDX elemental mapping in Figure 8 shows the presence of Cu_3Sn and Cu_6Sn_5 intermetallic phases in the solder, along with Kirkendall voids. In Fig. 8a, the voids are located at the solder/board interface, aligning with the direction of electron flux. Since there is no Ni plating on the board acting as a diffusion barrier, a significant amount of Cu metal has diffused from the board into the solder, following the direction of electron flux. In the case of electron flux from the lead to the board (Fig. 8b), a substantial amount of Cu has migrated from the lead to the board, resulting in the formation of Cu_6Sn_5 intermetallic phase near the board Cu. Additionally, voids are observed at both the solder/lead and solder/board interfaces. The Kirkendall voids at the solder/lead interface can be attributed to the electromigration of Cu into the solder. However, the formation of voids at the solder/board interface is a consequence of thermal diffusion when impurities are incorporated during Sn plating, as discussed in the previous section. It is known that the formation of voids leads to a locally increased current density due to the reduction in the cross-section of the current flow path. The damage observed on both sides of the source solder (Fig. 8b) further enhances these processes compared to the other three cases. As a result, the tested parts in this group exhibit a shorter lifetime in the test, with the first failure occurring at 1,143 hours. It should be noted that in the previous section, the lifetime calculation was performed with the assumption of water cooling on the SSO8 package with an exposed clip, used as the boundary condition to calculate the maximum current the product experiences during application. With a calculated R_{thJA} of 3.85 K/W, the maximum operating current of 204 A is determined. The current EM test demonstrates that electromigration-induced failure would not occur within the designed 15-year lifetime of the device, even under the worst-case scenario which is a Sn plated surface finish. However, if the product is subjected to a worse cooling condition, such as forced air cooling, free convection, or even free convection without a heatsink, the maximum operating current of the device needs to be significantly reduced. In such cases, the role of electromigration during application becomes less significant. For example, for an SSO8 on a 2s2p board with a simulated R_{thJA} of 26.5 K/W under free convection without a heatsink, the maximum operating current is only 78 A. In this scenario, electromigration plays a minimal role, if any, in device failure during application. Therefore, the maximum current the power device can handle during application is predominantly limited by the cooling capacity of the system rather than electromigration-related failures.

IV. Conclusion

This study focuses on the electromigration (EM) behavior of a power device in applications with a controlled environment. Two different the surface finishes, namely Ni-plated and Sn-plated, are used, and the two directions of electron flux are studied on each board. The test conditions involve a temperature of 125°C and a current density of 1.82×10^4 A/cm^2. For the Ni-plated board, no electrical failures are observed within the 4,000-hour testing period. In contrast, the lifetime of the Sn-plated surface finish is influenced by the direction of the electron flux. When the electron flux is from the board to the lead, the first failure occurs at 1,143 hours, followed by a second failure at 2,234 hours. However, no electrical failures are observed for the devices with electron flux from the lead to the board within the 4000-hour testing time. microstructural analysis reveals the formation of Kirkendall voids at the solder/board interface in the Sn-plated board groups, regardless of the direction of electron flux and the current density. These voids result from impurities incorporated during the Sn plating process. Consequently, the damage to the both solder/lead and solder/board interfaces during the EM test leads to a shorter testing lifetime for the Sn-plated surface finish combined with electron flux from the board to the lead. Nonetheless, this lifetime is still 1.5 times longer than the required testing time (782 hours) to cover the 15-year device lifetime in a server PSU application. It should be noted that the acceleration factor of the current test is calculated based on the maximum operating current of the SSO8 device, which is 204 A. This current can only be achieved with a thermal resistance (R_{thJA}) of 3.85 K/W when forced water cooling is applied. If the product is subjected to a worse cooling condition, the maximum operating current of the device needs to be significantly reduced. As a result, the role of electromigration during application becomes less significant. Thus, the maximum current the power device can handle in a controlled environment is primarily limited by the cooling capacity of the system rather than electromigration-related device failures.

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