Cost Analysis of Fan-out Processes for Chiplet Packaging

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Abstract

When building a design around chiplets, there are many factors to consider: industry standards, availability of chiplets within the supply chain, size requirements, and cost, to name a few. The cost of chiplet packaging is a particularly important factor that must be understood, because even if all design requirements can be met, the chiplet package will not come to fruition if the total cost is too high.

The basic tradeoff between a monolithic die and a series of chiplets is a reduction in silicon costs countered by an increase in packaging costs. This analysis will compare a monolithic die flip chip package to two fan-out processes that support chiplet packaging. In the first scenario, a two-chiplet chip-last fan-out on substrate package will be compared to a standard flip chip package. For the second comparison, a monolithic flip chip package will be compared to a four-chiplet fan-out package that utilizes embedded silicon for additional interconnect. For both scenarios, a detailed cost comparison will be provided.

Activity based cost modeling will be used for this analysis. In addition to looking at the direct costs of the substrate and assembly processes, yield considerations and the price of the incoming silicon (which varies by node) will be included. The goal of this analysis is to evaluate the cost of a monolithic flip chip package versus a chiplet scenario for two designs, and to highlight the cost drivers of the fan-out chiplet packaging processes.

Key words

Chiplets, cost comparison, fan-out wafer-level packaging, flip-chip packaging, WLP

I. Introduction

When building a design around chiplets, there are many factors to consider, such as industry standards, availability of chiplets within the supply chain, size requirements, and cost [1]. Even if all design requirements can be met by a particular technology, a chiplet package will not come to fruition if the total cost is too high.

The basic tradeoff between a monolithic die and a series of chiplets is a reduction in silicon costs countered by an increase in packaging costs [2]. This analysis compares a monolithic die flip chip package to two fan-out processes that support chiplet packaging.

In the first scenario, a two-chiplet chip-last fan-out on substrate package is compared to a standard flip chip package. For the second comparison, a monolithic flip chip package is compared to a four-chiplet fan-out package that utilizes embedded silicon for additional interconnect.

II. Process Flows

Two fan-out technologies that support chiplets are the focus of this analysis [3]. In the two scenarios analyzed, a fan-out technology is compared against a monolithic die that is packaged with flip chip technology. A generic flip chip process flow is shown in Fig. 1.

A. Fan-out on Substrate Process Flow

The first comparison focuses on packaging chiplets using a fan-out on substrate style process flow. This process flow is shown in Fig. 2. It is like a standard chip-last fan-out flow, in which the RDLs are built up first and then the incoming die or chiplets are flip chip bonded to the RDLs. At that point, a standard fan-out package would proceed to molding and debonding from the temporary carrier before singulation so that the diced fan-out package would be ready to be placed on a PCB. However, in the case of fan-out on substrate, the fan-out module is designed to be

placed on a flip chip substrate prior to PCB placement to support higher density designs.

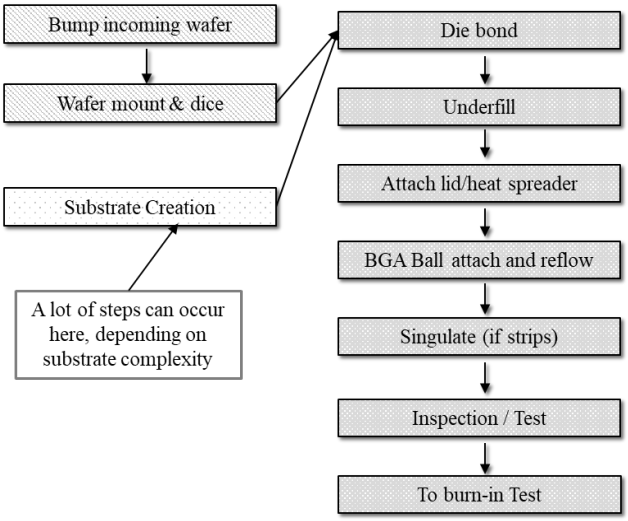

Figure 1. Generic Flip Chip Process Flow

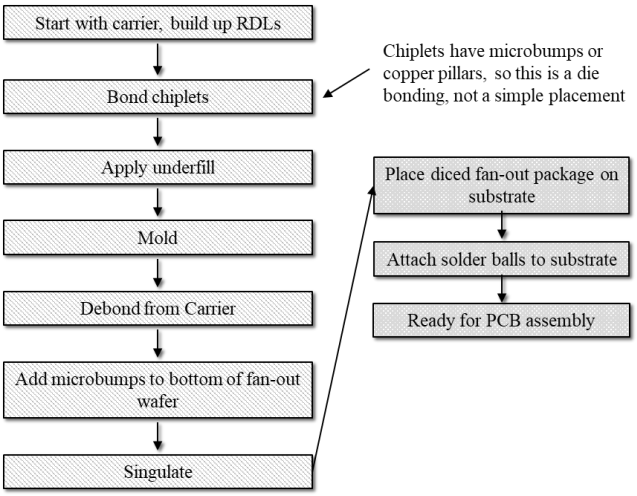

Figure 2. Fan-out on Substrate Style Process Flow

B. Fan-out with Embedded Silicon Process Flow

The second comparison focuses on a design that packages chiplets using a fan-out process flow that utilizes embedded silicon before mounting the chiplets on top of the fan-out module. This fan-out flow begins as a chip-first face-up process. Rather than placing the chiplets early in the process when the fan-out module is being created, pieces of silicon, called silicon bridges, are placed in the fan-out module to create additional routing.

The fan-out module has RDLs on the top and the bottom, as well as large copper vias to connect the topside and bottom side of the fan-out module. Once the fan-out module is complete, the chiplets are assembled on the top RDLs, molded, and then the chiplet-on-fan-out-stack is diced and ready for placement on a substrate.

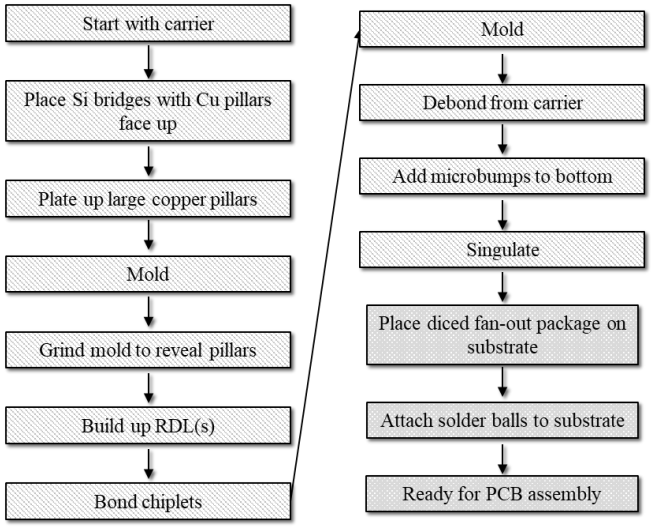

Figure 3. Fan-out with Embedded Silicon Process Flow

III. Activity Based Cost Modeling

Activity based cost modeling was used to construct generic flip chip and FOWLP models. With activity based cost modeling, a process flow is divided into a series of activities, and the total cost of each activity is calculated. The cost of each activity is determined by analyzing the following attributes: time required, amount of labor required, cost of material required (consumable and permanent), tooling cost, all capital costs, and yield loss associated with the activity.

IV. Cost Comparison

A. Fan-out on Substrate vs. Standard Flip Chip Packaging

The first analysis compares packaging a single 10nm die in a flip chip package to breaking the silicon into two chiplets that are packaged with fan-out on substrate technology.

Table I. Fan-out on Substrate vs. FC Design Details

	FC Design	**Fan-out on Substrate**
Die Size (mmxmm)	9x9 10nm die	4x4 10nm die, 8x8 28nm die
Fan-out Module Size (mmxmm)		15x10
Substrate Size (mmxmm)	20x20	25x20
BOM Items	1 die	2 die
RDLs		2

The total area of silicon is approximately the same in both designs. Key design details are shown in Table I. The same

substrate structure is assumed for both cases, the same factory location is assumed to keep the labor rate stable across designs, and only direct costs are considered (no overhead or profit margin assumptions). Focusing on direct cost is useful for understanding key cost differences between technologies. It is not useful when the user must consider price; the topic of price versus cost will be reviewed briefly later in the analysis.

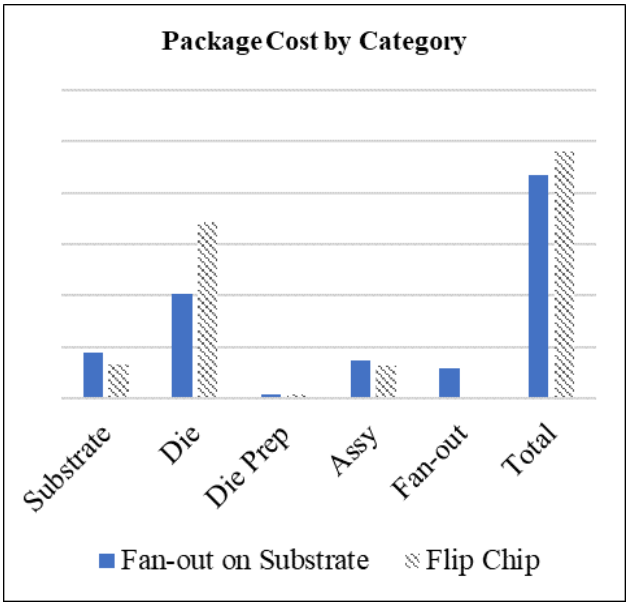

Figure 4. Fan-out on Substrate vs. FC Costs by Category

The chart in Fig. 4 shows the direct cost per package broken up into five categories.

- Substrate: The substrate cost is higher in the fan-out scenario because a larger substrate size was assumed for this design.
- Die: This represents the incoming cost of the single die for the flip chip package, and the two incoming chiplets for the fan-out on substrate scenario. As discussed, the trade-off when pursuing a chiplet option is a reduced silicon cost that drives increased packaging cost. This bar clearly shows that breaking one large 10nm die into a smaller 10nm die and using a 28nm die for other functionality creates a cost benefit.
- Die prep: This is very low cost, and represents the activities associated with taking a wafer and thinning, bumping, and dicing it for placement in a package.
- Assembly: These are the activities of placing the flip chip die or diced fan-out package onto a substrate. This is a higher cost for the fan-out scenario because a 9x9mm die is being bonded in the flip chip scenario versus a 10x15mm fan-out module. The cost of the activities of die bonding and applying underfill are driven by area.
- Fan-out: This category only exists for the fan-out package. This category captures all fan-out activities, from carrier through RDLs to chiplet placement and molding.

The higher packaging costs of the fan-out package, evident in the substrate, assembly, and fan-out categories, are offset by the reduced silicon cost, resulting in a total package cost that is higher for the flip chip package than for the fan-out chiplet scenario.

The key takeaway here is not that all chiplets should be packaged with fan-out on substrate technology, however. The design shown is cost-effective with fan-out packaging using the given set of assumptions, but the results are heavily dependent on many factors, such as fan-out module size, die size, which node is necessary for each die, how much larger the substrate must be, how many RDLs are needed, and more.

In the baseline example shown in Fig. 4, the fan-out scenario is about 10% less expensive than the flip chip scenario. The table below shows how that cost savings shrinks with a single assumption change.

Table II. Impact of Changing One Variable in Fan-out on Substrate vs. FC

Scenario	Fan-out Cost relative to FC
Baseline Scenario	-10%
Fan-out module extended by 1mm in each direction	-7%
3 RDLs	-7%
1% yield drop for fan-out	-9%
16nm instead of 10nm	12%

B. Fan-out with Embedded Silicon vs. Standard Flip Chip

A second comparison was carried out, this time breaking a monolithic die into four chiplets for fan-out packaging utilizing embedded silicon.

Table III. Fan-out on Substrate vs. FC Design Details

	FC Design	Fan-out on Substrate
Die Size (mmxmm)	20x20 10nm die	All die 10x10 Two 28nm, One 45nm, One 10nm
Fan-out Module Size (mmxmm)		25x25
Substrate Size (mmxmm)	30x30	40x40
BOM Items	1 die	4 die, 2 silicon bridges costing 50 cents each
RDLs		1 topside, 1 bottom side, both fine l/s

The results across the five categories are similar. There are a few additional notes for this fan-out with embedded silicon scenario versus the way the results came out with the fan-out on substrate design.

- Die: In the previous comparison, this category was only a comparison of the original large flip chip die versus the cost of the various chiplets. In this case, this bar also includes the cost of the embedded silicon bridges.
- Fan-out: It is worth noting that this category stacks up differently in this design versus the last one. In the results chart for fan-out on substrate, the fan-out bar and assembly bars were approximately the same height, meaning the activities in aggregate were a similar cost per package. In this scenario of fan-out with embedded silicon, the fan-out bar is visibly higher than the assembly bar. That's because there are activities for fan-out with embedded silicon that aren't needed for fan-out on substrate: topside RDL creation, placement of the chiplets on top of the fan-out module, and molding those chiplets.

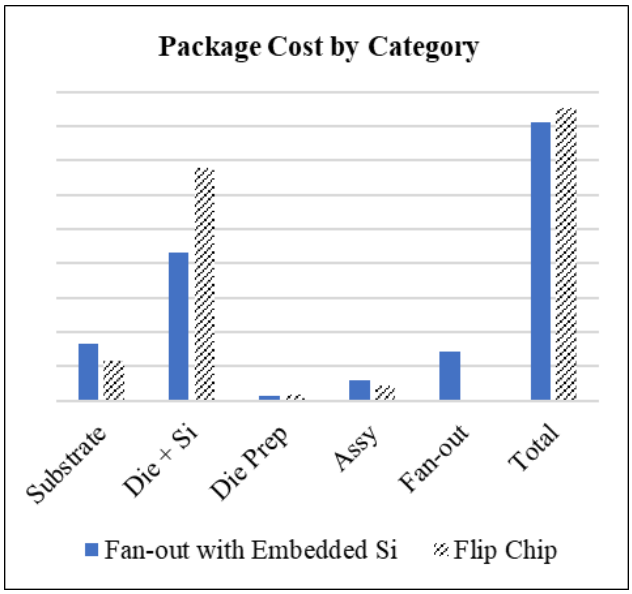

Figure 5. Fan-out with Embedded Si vs. FC Costs by Category

Even with the increased fan-out processing costs in this style of packaging, there is still an overall cost savings when looking at the total cost per package.

As with the previous technology, this single comparison does not mean it will always make sense to package chiplets in a fan-out with embedded silicon design. Table II shows how the baseline results change with different assumptions. In the previous design, the results were based on how much more cost-effective the fan-out design was on a percentage basis. In this design, the results show absolute cost: the numbers in the table show how much more the flip chip package costs versus the fan-out package.

Table IV. Impact of Changing One Variable in Fan-out with Embedded Silicon vs. FC

Scenario	How much more expensive is FC per pkg?
Baseline Scenario	$2.17
2% yield drop for fan-out	$1.82
Fan-out module extended by 1mm in each direction	$1.79
One 20nm die instead of a 28nm die	$1.21
2 topside and 2 bottom RDLs	$0.28

C. Direct Cost vs. Price

As previously mentioned, the focus of this technology comparison is direct cost. This is a valuable way to understand the cost drivers of disparate technologies. However, in a real-world scenario, a designer would want to consider the final price of a product, not just its direct costs.

Price is complicated, and there are many factors that will impact price that are not represented in this analysis. Factory utilization and the volume of the package being built will impact price. Indirect costs must also be considered for any product [4]; this category captures factory costs not directly associated with a specific activity like support, quality, manufacturing engineering, utilities, and clean room. There are also overhead costs, which are company costs that need to be covered, such as marketing and engineering. Profit margin must certainly be factored in as well.

The comparisons shown in this analysis are an excellent starting point to understand how newer technologies like fan-out may compete with a mature process like flip chip, but real world pricing may ultimately drive very different results at this point in time.

V. Conclusion

This analysis explored two fan-out technologies that support the packaging of chiplets. When breaking a monolithic die into chiplets, the basic tradeoff is a reduction in silicon costs and an increase in packaging costs.

The first fan-out packaging technology compared to standard flip chip packaging was a fan-out process that places the fan-out module on a substrate prior to PCB placement. This is the simpler of the two fan-out processes analyzed. For the two-chiplet design selected, it was shown that some categories of direct cost were more expensive with the fan-out package—substrate costs, assembly costs, and fan-out costs—but the silicon savings were enough to

make the final package cost less with fan-out than with a monolithic flip chip package.

The second fan-out technology analyzed was a fan-out technology that utilizes embedded pieces of silicon in the fan-out module, with chiplets placed on top of the completed fan-out module. Although the fan-out processing costs for this technology are higher than for fan-out on substrate, it was still shown that for the four-chiplet design analyzed, the fan-out solution was more cost-effective than the monolithic flip chip die package from a direct cost perspective.

In both cases, the selected design and assumptions showed that fan-out packaging of chiplets was more cost-effective than flip chip packaging, but that will not always be the case. Many design factors must be considered, such as substrate size, fan-out size, number of RDLs, and yield. Changing the assumption for even one variable can shift the results to show flip chip packaging of one large monolithic die as the most cost-effective choice. Furthermore, direct costs are only one part of the equation, and pricing must be considered as well. Chiplet packaging is complex, and every scenario should be evaluated in detail before committing to a packaging method.

References

[1] M. Lapedus, “The Good and Bad of Chiplets,” Semiconductor Engineering, May 2020.
[2] M. Lapedus, “Paving the Way to Chiplets,” Semiconductor Engineering, April 2022.
[3] L. Peters, “Improving Redistribution Layers for Fan-out Packages and SIPs,” Semiconductor Engineering, September 2022.
[4] K. De Backer, et al, “Reducing indirect labor costs at semiconductor companies,” McKinsey & Company, August 2019.