The impact of Al on contact resistance and its suitability in fine pitch interconnects

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Abstract

Integration issues for a three-dimensional (3D) interconnect in a Face-to Face (F2F) configuration are discussed. In particular, the effect of Al and organic dielectrics under the bump and their effect in chip-package-interaction (CPI) stresses as well as Al contact resistance issues that arise as the interconnection pitch is decreased. This paper will present a finite-element model created to study the stresses in advanced 3D microelectronic package. To assess the reliability of the 3D packages a submodeling approach is used to capture the CPI stresses. The modeling study presented indicates that it is beneficial to continue using Al pads as it has significantly lower stresses compared to copper pads/vias. In the second portion of the paper, the effect of PBO developer on Al corrosion is presented. Reactive ion etching (RIE) chemistries and wet chemistries were optimized using contact resistance as the success metric. Process robustness was achieved by decoupling the hard dielectric opening from the PBO via opening. Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS), Scanning Electron Microscopy (SEM), X-ray Photoelectron Spectroscopy (XPS) analysis were used to add clarity to the bump contact resistance values.

Key words

3D chiplet packaging, Fine pitch, CPI modeling, advanced packaging, assembly stresses, Al corrosion

I. Introduction

Advanced 3D chiplet packaging is converging into a F2F integration approach either via Die to die (D2D) and Die-to-wafer (D2W). As the interconnection pitch decreases, a closer look is needed on the use of Al and the organic dielectric under the bump and their effect in CPI stresses as well as bump contact resistance. Experimental data pertaining to the Al surface integrity impacted by corrosion-related issues during downstream processing and mitigation techniques are studied.

To safeguard the Al interconnects, silicon nitride (SiN) and silicon dioxide (SiO_2) dielectric films are deposited, creating a protective barrier. Additionally, as the interconnection pitch is decreased, photosensitive polymeric benzoxazole (PBO) is preferred due to its improved resolution. Since the PBO is a positive tone resist, it uses Tetramethylammonium Hydroxide (TMAH) as the developer. Careful process integration is needed to avoid Al corrosion when exposed to TMAH, and the RIE fluorine-based chemistries used to etch the SiN/SiO_2.

This paper also delves into the role of Al in redistributing stress and the intricacies of Al integration in semiconductor packaging. Fig. 1 shows the two areas of interest which were modeled: chip-to-chip and chip-to-laminate.

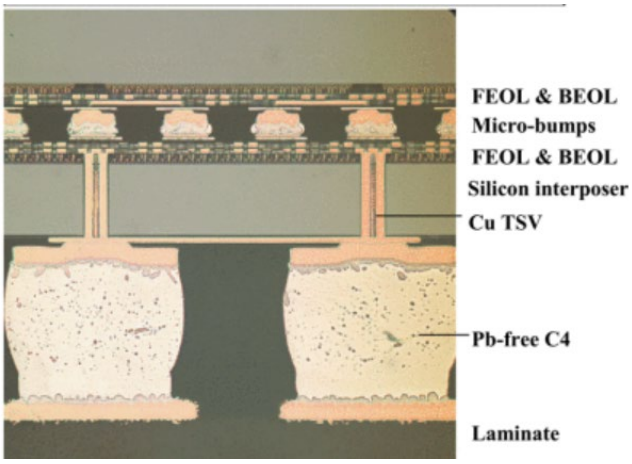

Fig 1. Cross section of a 2.5D structure [1]

The fine pitch configuration, characterized by closely spaced interconnects, exacerbates challenges related to thermal expansion mismatch, stress concentration, and fatigue. A robust finite-element model is essential to comprehensively

assess the package's response to these challenges and guide design improvements. The relative stresses when Al pads in the bottom chip at top chip/bottom chip interface are replaced with Cu and the effect of removing PI layer present in the top chip in a 3D fine pitch microelectronic package is quantified using a high-fidelity finite-element model. The model aims to provide insights into the thermo-mechanical stresses in the package during thermal cycling.

II. Modeling result and discussion

Finite-Element Model Description

A three-dimensional finite-element model is created to study the stresses in advanced 3D microelectronic package. A submodeling approach is used to capture the stresses in the chips due to chip-package-interaction effects. The global model shown in Fig. 2, captures the overall warpage of the package. Effective material properties are used for the interconnect layers between top/bottom chip and bottom chip/substrate interfaces in the global model. The local model is shown in Fig. 3, wherein all the parts are explicitly modeled and used to capture the stresses in the regions of interest. This study focuses on the maximum principal stresses at the BEOL region in top/bottom chip and bottom chip/substrate interfaces. The region is of high interest as porous ultra-low k layers used in BEOL are prone to failure during reliability cycling [2].

Temperature dependent linear elastic isotropic material is used to simulate all materials except for the substrate and the solder. Orthotropic material properties are used to simulate the substrate and viscoplastic material properties are used to simulate the Pb-free solder. For the sake of brevity and due to proprietary reasons, material properties are not listed.

A quarter model of the 3D package shown in Fig. 2 is constructed taking advantage of the symmetry in design and material properties. The model assumes a top-down assembly during bond and assembly process. In other words, the model assumes that the two chips are joined first and then the chip assembly is joined to the organic substrate. Since the initial chip join does not involve any differential coefficient of thermal expansion between the bodies joined together, it is not simulated as a separate loadstep.

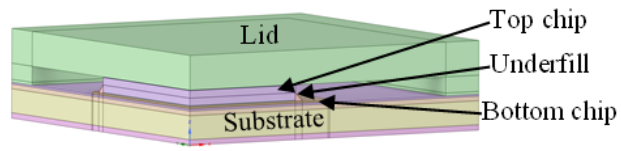

Fig. 2. Global Finite Element model

In the first loadstep, the chip-substrate global model interconnected with solder-bumps and underfilled is cooled down from reflow temperature to room temperature.

Then the global model is heated to sealband curing temperature. In the third loadstep, the sealband, thermal interface material (TIM) and lid are activated and the model is cooled to -40 °C. The stress-free temperature for the lid, sealband and TIM is assumed to be the sealband curing temperature. The stress-free temperature for the other components is assumed to be the Pb-free solder reflow temperature.

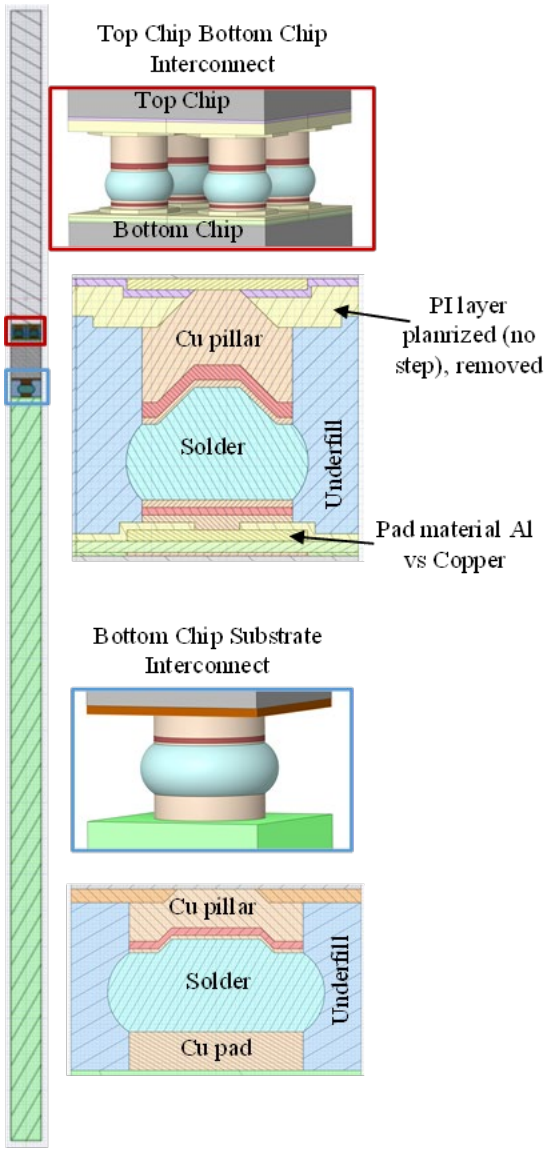

Fig. 3. Local model for chip-to-chip and chip-to-laminate.

The cross-section of the local model is shown in Fig. 3. It is placed at the critical location where the stresses are to be extracted. In this case, it is placed at the corner of the top die where BEOL failures typically occur during reliability cycling due to the longer distance from neutral point. The displacement boundary conditions are mapped from the global model to the local model at each loadstep on the outside faces of the local model. The same temperature

profile and loadstep profile like the global model is applied to the local model as well.

Local Model Results

The model described above is used to perform what-if analyses for understanding the effect of changing the pad material of the bottom chip at the top/bottom chip interface, changing the material of vias between the bottom chip pad to the line underneath and removing the PI layer from the top die. The PI layer and the pad are highlighted in Fig. 3. Maximum principal stress at the end of reliability cycle (last loadstep) in top die/bottom die interface and in the bottom die/substrate interface is studied.

Fig. 4 shows the typical stress contours at the top chip and bottom chip interfaces. As seen, stresses are concentrated under the copper pillar. One side of the pillar is under tensile stresses (red / orange) while the other side is under compression (green / blue), similar to previous 2D package studies. In the bottom chip similar tensile / compressive stress contours underneath the copper pillar are observed, as shown in Fig. 4b.

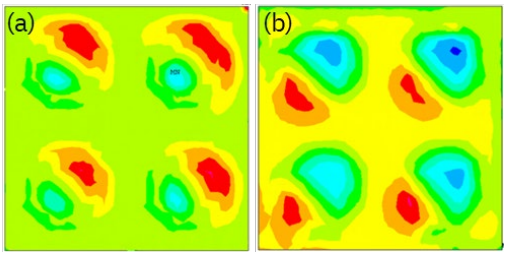

Fig. 4. Local model max principal stress contour between top chip and bottom chip, a) top chip BEOL region b) bottom chip BEOL region.

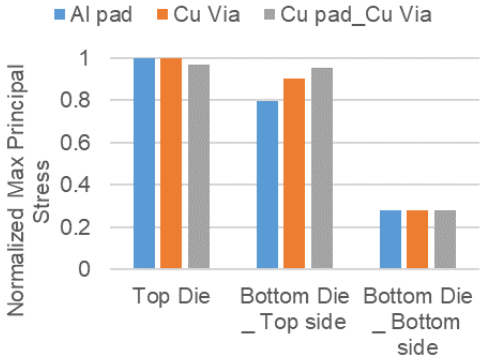

Fig. 5. Normalized max principal stresses for pad/via material changes.

In this study, the maximum tensile principal stresses are compared for various cases as tensile principal stresses cause failures in brittle BEOL layers [3]. Since the model is yet to be validated using experiments, the model with the Al pad is treated as the baseline and all other results are normalized based on that data. As shown in Fig. 5, changing the material of the via from Al to Cu in the bottom chip increases the stresses by 10% and changing the pad material to Cu also increases the stresses by 15% compared to the baseline. As shown in Fig. 6, removing the PI layer increases the stresses by 60%. However, the changes have a local impact and effect of changes is not felt at other locations. In other words, removing PI layer in the top die does not have an impact on stresses in bottom die. It can also be seen that the stresses in the bottom side (bottom chip / laminate interface) of the bottom chip is significantly lower than the stresses in the top side of the bottom chip. This indicates that from a mechanical perspective, face to back configuration is preferred.

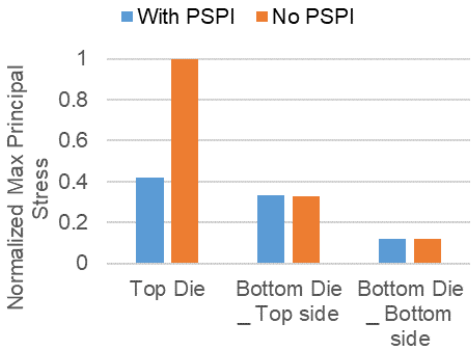

Fig. 6. Normalized max principal stresses with & without PI

Modern microelectronic packages demand enhanced mechanical and thermal performance due to the continual miniaturization and integration of components. The fine pitch configuration, characterized by closely spaced interconnects, exacerbates challenges related to thermal expansion mismatch, stress concentration, and fatigue. To improve the reliability of advanced packages, the modeling study presented in this section indicates that it is beneficial to continue using Al pads as it has significantly lower stresses compared to copper pads/vias. The rest of this paper walks through process integration challenges for Al and potential solutions as we move towards advanced fine-pitch microelectronic packages.

III. Experiment for a Clean Al Surface

In a chip fabrication flow with Al wiring and pad as terminal layer, wafers typically exit the Si fab either with the wafer encapsulated by hard dielectric such as SiO_2/SiN or with the Al pad exposed after the hard dielectric patterning (Fig. 7). In both flow A and B, process steps which influence Al surface integrity and contact resistance are: RIE and post RIE clean of the hard dielectric opening, as well as under bump metal (UBM) liner seed pre-clean and deposition. Meanwhile, specifically for flow A, the Al surface integrity is also influenced by the organic dielectric patterning process.

A. Impact of RIE and post RIE clean to Al surface integrity

Al corrosion post RIE has been reported and it can be

chemical or galvanic in nature [4]. Chemical corrosion typically manifests as growth on sidewall or pad due to residual halogen mainly from etch byproduct reacting with moisture in ambient. Galvanic corrosion manifests as voids or pitting in the Al due to galvanic cell formed between Al and TiN cap or presence of Cu in the Al alloy, with residual halogen dissolved in water acting as the electrolyte. In both cases, it is critical to minimize halogen residue on Al pad by optimizing the RIE and post RIE clean processes.

Hard dielectric RIE mainly consists of SiO_2/SiN etch, post etch treatment, and resist strip steps. In structures where Al pad is capped with TiN. Table I. showed representative steps and corresponding chemistries in four RIE recipes investigated to optimize F and Cl residue on Al surface.

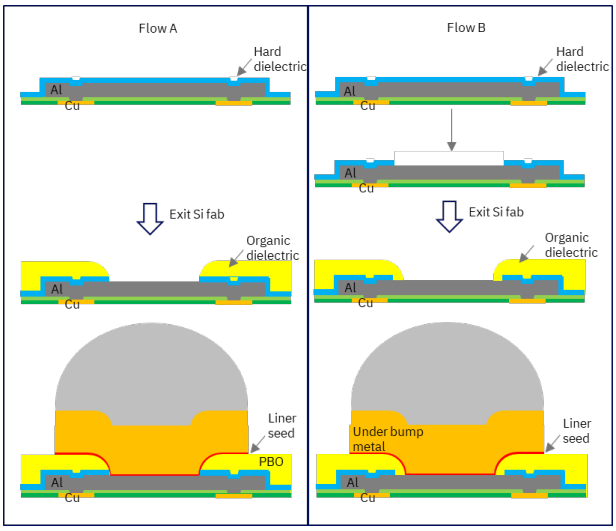

Fig. 7. Illustrated processing flow with Al wiring and pad as terminal layer.

Table I. Hard dielectric RIE recipes investigated. o and x denote step being used or not in the corresponding recipes.

Step	Chemistry	RIE recipe			
		v0	v1	v2	v3
SiO2/SiN etch	CF4/CHF3/He/Ar	o	o	o	o
O2 flash	O2	x	x	o	o
TiN etch	BCl3/CF4/He/Ar	o	x	o	x
Post etch treatment	BCl3/He	o	o	o	o
O2 flash	O2	o	o	o	x
Resist strip	water vapor	o	o	o	o

Defect morphology was characterized using SEM. Depth profiling of the Al surface was done using ToF-SIMS. Analysis beam was unbunched 30kV, Bi_3+, 50x50um and sputter beam was 250-500eV Cs^+, 400x400um. Samples were floated on glass for uniform charge compensation. Sputter rates were calibrated to SiO_2 reference and as such sputter depth shown is an estimate. Surface analysis was done using XPS with monochromatic Al Kα source on 5 sites/wafer and the Binding Energy is calibrated to Al 2p metal peak at 73 eV.

Comparison of Al pad SEM images taken 4 days and 47 days after dielectric RIE v0 and dilute sulfuric peroxide (DSP) clean showed pitting mostly along the Al grain boundaries (Fig. 8a, b). ToF-SIMS depth profiling of a sample exposed to air ambient for 28 days after RIE and clean revealed several layers on the Al surface, namely 1: highly fluorinated top surface, 2 and 3: ~30nm of Al oxide with varying degree of F- and Cl- incorporated in it, 4: ~5nm Al oxide, 5: bulk Al metal (Fig. 8c). The Al pad pitting and the presence of 35nm Al oxide with F- and Cl- incorporated through the bulk of the oxide are evidence of galvanic corrosion occurring with RIE v0 and DSP clean.

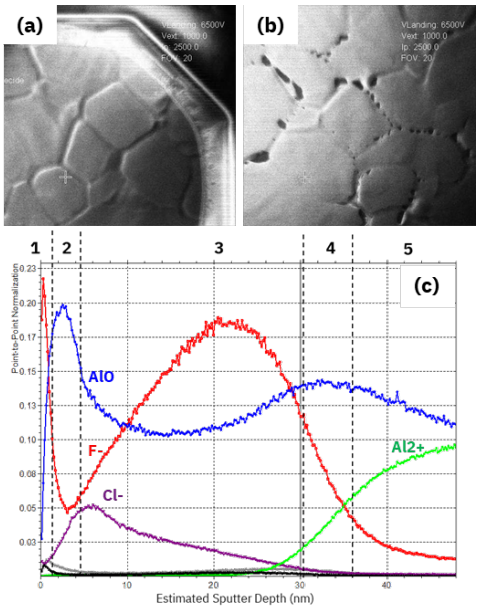

Fig. 8. SEM image of Al pad taken (a) 4 days and (b) 47 days after RIE v0 and DSP clean, (c) ToF-SIMS depth profile of Al pad 28 days in air after RIE v0 and DSP clean.

To investigate the modulation of F and Cl residue post RIE, blanket Al/TiN wafers were subjected to RIE recipes in Table I, followed by DSP clean. Relative to reference RIE v0, TiN etch step was eliminated in RIE v1 to reduce Al surface exposure to a mix Cl/F containing plasma. An O_2 flash step was introduced after the SiO_2/SiN etch in RIE v2 to volatilize surface fluorocarbon film deposited during SiO_2/SiN etch. In the fluorocarbon plasma etch of SiO_2, deposited fluorocarbon on the surface acts as reactants which upon ion bombardment enables etching of the oxide [4]. In addition to combining the removal of TiN step in RIE v1 and addition of O_2 flash in RIE v2, the final O_2 flash step was also removed in RIE v3.

XPS chemical analysis in Fig. 9 revealed decreased F 1s and O 1s peak signal, as well as increased Cl 2p peak signal for the RIE v3 relative to the RIE v0 split. In the Al 2p region,

the Al metal to oxidized Al peak ratio increased in RIE v3. Based on the inelastic mean free path, Al 2p photoelectron is estimated to originate from less than 3nm from. Thus, the higher relative intensity of Al metal to oxidized Al peak indicates that RIE v3 produced thinner oxidized Al layer. Meanwhile, XPS analysis from RIE v1 and v2 were not significantly different to RIE v0 (not shown). This indicates that the removal of fluorocarbon from Al surface through the insertion of O_2 flash step and removal of TiN step which chemistries contains both BCl_3 and CF_4 is critical. The increased Cl 2p peak signal in RIE v3 indicates that the final O2 flash step is necessary to volatilize any Cl residue on the surface.

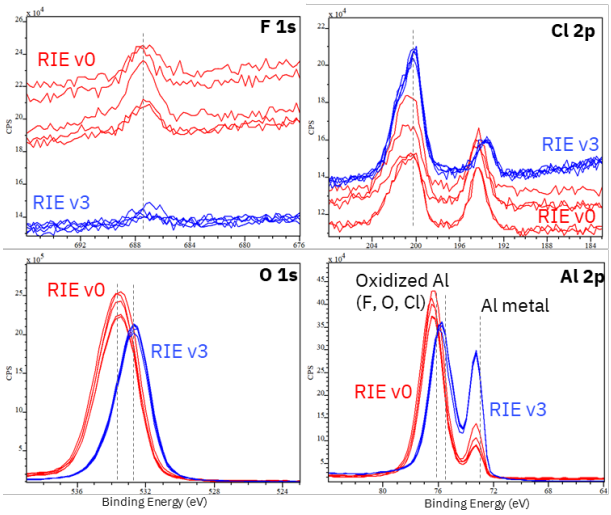

Fig. 9 High resolution XPS in the Al 2p, O 1s, F 1s, Cl 2p regions from blanket Al film subjected to RIE v0 or RIE v3, resist strip and DSP clean.

The learning from blanket wafers was implemented on patterned wafers and quantitative TOF-SIMS analysis performed is shown in Fig. 10. RIE v3 followed by DSP clean showed 54% and 83% reduction in both F and Cl residue on the surface compared to RIE v0, yet with comparable overall oxidized Al thickness. An additional Al etch step was introduced between RIE and DSP clean step to modulate the oxidized Al thickness. From SEM cross section (not shown), the Al etch removed about 70nm of surface Al. The combination of RIE v0 + Al etch + DSP resulted in the least oxidized Al thickness while the combination of RIE v3 + Al etch + DSP resulted in the least surface F and Cl residue.

ToF-SIMS depth profile in Fig. 11 revealed that while the oxidized Al was thinner in the RIE v0 + Al etch + DSP clean combination, F incorporation into the oxidized Al layer was apparent. Meanwhile, F was restricted to topmost surface for the RIE v3 + Al etch + DSP split. An aging experiment was conducted to determine if the oxidized Al with such level of F incorporated is stable with time. TOF-SIMS analysis of a sample stored in air for 5 weeks was compared to that of a sample stored in ultra high vacuum for 5 weeks did not show significant difference in the oxidized Al thickness (Fig. 12). Fluorine content increased with sample stored in air, likely due to contamination limited to the surface.

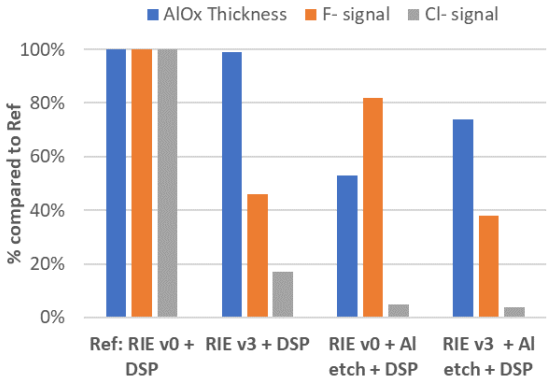

Fig. 10. Oxide thickness, F- and Cl- signal relative to reference first cell from TOF-SIMS analysis of patterned wafers subjected to different etch and clean combination.

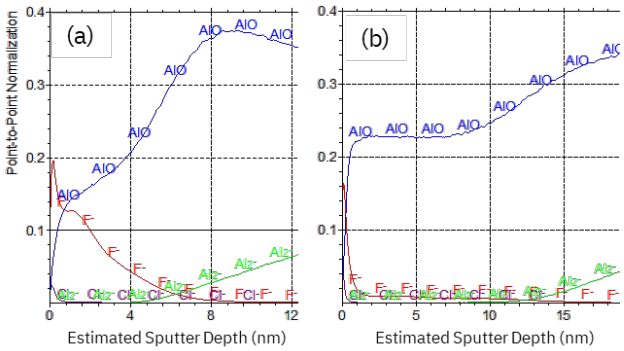

Fig. 11. ToF-SIMS depth profile of Al pad after (a) RIE v0, (b) RIE v3, both were followed by Al etch and DSP clean.

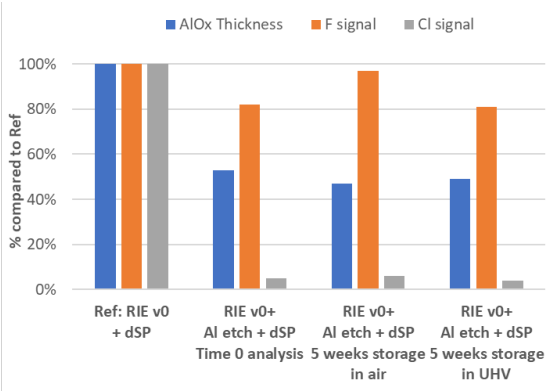

Fig. 12. Oxide thickness, Fluorine and Chlorine signal relative to reference cell from TOF-SIMS analysis taken at different time and storage ambient.

As described by [5], DSP cleaning of Al RIE residue works

based on the dissolution of Al_2O_3 by sulfuric acid and passivation/oxidation of the surface by hydrogen peroxide. Since oxidized Aluminum thickness was reduced only by the introduction of Al etch before DSP clean, this indicates that the etching and passivation mechanism of DSP clean is less efficient on the F- and Cl- contaminated surface. This resulted in the observed galvanic corrosion/pitting and incorporation of Fluorine and Chlorine into the bulk oxide. Thicker oxidized Al on RIE v3 + Al etch + DSP compared to that of RIE v0 is consistent with this hypothesis. As RIE v3 produced less Fluorine and Chlorine on the surface, oxidation/passivation of the surface occurred more readily than RIE v0 surface.

B. Impact of organic dielectric patterning to Al surface integrity

In flow B, after exiting the Si fab, wafers are then subjected to photo-sensitive organic dielectric coat-expose-develop, descum RIE, UBM liner seed pre clean and deposition, after which the Al surface is no longer directly exposed to further processing. In order to assess Al interface quality, four point probes measurements were done on six edge of array bumps at wafer center and edge.

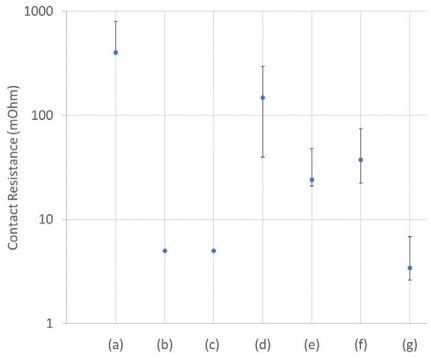

Fig. 13 Bump contact resistance of wafer processed through integration flow B with (a) reference processes described in text, (b)-(c) PBO coat-expose-develop steps removed, (d) inserting Al etch and DSP clean after PBO coat-expose-develop, (e) doubling the liner seed pre clean, (f) combination of (d) and (e), and (f) on wafer processed through integration flow A.

Fig. 13 (a) showed bump contact resistance higher than 400 mOhm for a wafer that went through reference standard processing of PBO coat, expose, and develop in TMAH. Failure analysis using SEM revealed delamination at the UBM liner to Al pad interface (not shown). Contact patterning generally favors positive tone materials to enable larger depth of focus and process latitude. Similarly, positive tone photosensitive organic dielectrics are more attractive than negative tone in achieving smaller via diameters. TMAH as a strong alkali, however, is known to dissolve Al oxide passivation, rendering the surface susceptible to corrosion [6]. As evident in Fig. 13(b)-(c), skipping the PBO coat-expose-develop step reduced contact resistance to <10 mOhm. The same effect is achieved by processing a wafer through flow A in which Al surface is encapsulated by the hard dielectric during PBO coat-expose-develop as shown Fig 8 (g). Attempts to reset the Al surface after TMAH impact using additional clean such as the Al etch and DSP, doubling the liner seed pre clean or its combination thereof while improving the contact resistance, it did not reduce it to below <10 mOhm.

IV. Conclusion

FEA modeling showed that having Al pad/via is critical to maintaining BEOL ULK stresses as it produces significantly lower stresses compared to copper pads/vias. The absence of PI also increased stress albeit limited to the die without PI. The passivation of Al surface and the integrity of that passivation prior to pre liner seed degas/sputter is critical in achieving low resistance interface. Passivation RIE & clean process need to be optimized for minimal F and Cl incorporation into Al surface. Al etch could mitigate the impact of F and Cl from RIE. When using alkaline developer, it is necessary to avoid direct contact of the developer to Al. Direct contact to Al in alkaline developer caused corrosion and increased bump resistance, not mitigated by additional rinse, sputter etch. The findings contribute to a deeper understanding of the complexities involved in designing interconnects for next-generation semiconductor devices.

Acknowledgment

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