Internal Bump Cracking Risk Assessment for Flip Chip Ball Grid Array Package During Board Level Reliability Test Through Finite Element Analysis

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Abstract

The performance of semiconductor devices during board-level reliability (BLR) thermal cycling tests continues to be a concern in different applications. The primary focus of those BLR tests is to evaluate the fatigue life of external solder joints between the package and printed circuit board (PCB). For flip-chip ball grid array (FCBGA) package technology, internal solder bumps can also crack and result in open electrical failure. This type of BLR failure is seldom, if at all, reported in the literature.

This article presents failures due to internal solder bump cracks during the BLR test. Failure analysis (FA) clearly shows the cracking location strongly depends on bump density. Finite Element Analysis (FEA) based simulation is performed to understand the failure mechanism. Unlike the standard BLR modeling approach, which focuses on predicting external solder joint fatigue life with correlated data, simulation here has to capture the entire internal bump pattern in the global BLR model. The need to capture the entirety of the bump scheme poses a significant challenge to managing the global model size with a reasonable meshing count and running time. Therefore, a customized post-process approach is developed to analyze bump density impact and enable design optimization.

Key words

FCBGA, BLR TC, Internal Solder Bump Crack, FEA

I. Introduction

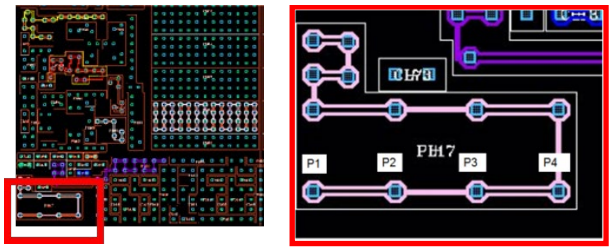
The performance of surface mount semiconductor devices during Board Level Reliability (BLR) Temperature Cycle (TC) testing is a critical reliability metric used in the Integrated Circuit (IC) industry for many applications. The primary goal of BLR testing is to evaluate the mechanical "life" of the solder connections between the IC package and PCB. The IC packages are mounted on PCBs using SMT (Surface Mount Technology), and are subjected to temperature cycles. During the testing, an electrical net ("Daisy-Chain") passing through multiple solder connections is monitored for any electrical opens due to solder joint cracking. The typical failure mode during BLR TC tests is external solder joint cracking and has been reported across different package types (BGA, QFN, Chip on Lead package, WCSP). Extensive work has been done to study this type of failure mode [1-2]. Damage can also occur inside the package and cause BLR failure since Daisy-Chain net goes through die connected to PCB. Actually, any damage on the tested net can cause failure. However, not many cases have been reported in the literature for BLR failure caused by package internal damage. For wire-bonded packages, internal bond wire can be broken and cause BLR failure. Other common failure modes can also occur during the BLR TC test, like substrate trace cracking, back-end-of-line (BEOL) damage, and others. This serves as a cautionary reminder that the BLR TC test is not always associated to external solder joint but also internal bump connectivity.

In a recent publication, we reported on BLR failures due to internal solder interconnect for a FCBGA package [3]. The crack originated at the edge of the die and propagated along the interface between silicon and underfill. Once the crack reached the Cu pillar bump, solder joint cracking occurred and caused open failure in the daisy chain loop. One of the solutions is to replace the Cu pillar bump with conventional solder bump. The question is if the solder bump solution will behave better to meet the qualification requirement, which requires no failure before 1000 cycles. It is always good idea to build the design and do the physical test. However, this requires a new learning cycle, which includes redesign,

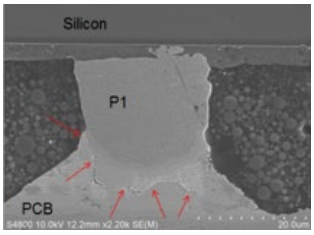
manufacturing, and test. It will take a few months or may be a year or so to get test data and there is also additional cost impact. A quick approach to assess the internal solder joint reliability during the BLR TC test is critical to shorten the package development cycle.

II. Test Vehicles

Test vehicle A is a 17x17mm FCBGA package with copper pillar as the interconnect. During the BLR TC test, very early open failure occurred around 300 cycles. Failure location was identified at areas of lower bump density, as shown in Fig. 1. The cross section shows solder cracking under the pillar inside the package while external solder joints are still in good shape. This confirms that early BLR failure was caused by internal damage, not external solder joint. Test vehicle B is also a 17x17mm FCBGA package with standard solder bump as interconnect. The bump layout under the die is identical between those two test vehicles. Package structures are also quite similar between A and B. There is a slight difference in the assembly process due to different interconnect technologies. One of the common mistakes is to assess BLR performance directly by comparing the stress level between those two designs since they both have solder material. However, different interconnect technologies and assembly processes bring in different solder thicknesses and intermetallic compound (IMC) structures at the solder interface. It is not appropriate to directly compare the stress level between those two structures to assess the BLR performance. A reference design with the same interconnect as design B is needed. Test vehicle C has a very similar package structure and BOM (Bill of material) as vehicle B, and BLR TC data is also available. Now, the focus is to use vehicle C as the reference to assess the BLR performance of vehicle B with the solder bump.



(a) (b)



(c)

Figure 1: (a) Bump map for test vehicle A; (b) Coarse bumps on die corner; (c) Cracks at Cu pillar

III. Finite Element Modeling

Finite element modeling has been widely used to access solder joint reliability during board-level reliability tests [4-8]. The common approach is to generate the package global model with thermal load added and extract plastic work density increment from critical solder joints. Cycles for failure can be predicted based on the correlation between empirical test data and plastic work density increment from the model. However, the current study does not have enough empirical test data to establish a correlation. A quick comparative model will be the primary focus here. In the typical BLR model, detailed die design is not considered in the package global model since it has little impact to stress level at external solder joints. The main driving force to impose stress on the external solder joints is the coefficient of thermal expansion (CTE) mismatch between PCB and package. However, the interesting region in this study is the solder bump inside the package. The model has to capture the entire bump layout, given the damage occurred close to the lower bump density area. Test vehicle B has about 1800 Cu pillar bumps. It is quite challenging to have a model to capture PCB and a significant amount of small internal bumps the same time due to different length scales. A simplified model is needed to manage the global model size with a reasonable meshing count and running time.

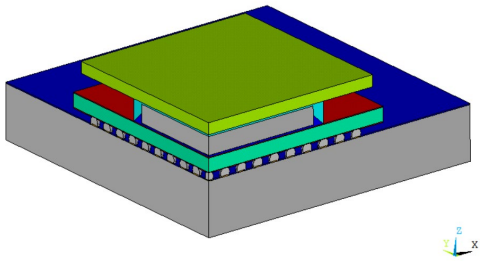
A commercial software was used for the modeling. Fig. 2 shows the generated package model with the cross-section view and simplified bump pattern. To attain good accuracy, all models were meshed with quadratic elements (3D element with 20 nodes). Elastic properties were used for all materials except SAC305 solder connected to the die and PCB. Properties from reference for solder with Anand's viscoplasticity model [3] and PCB [4] were employed in the model. The substrate was treated as a block with effective orthotropic properties considering the metal density in each layer. Cracking can occur at the internal solder joint close to the die side (Bump Top Solder) or substrate side (Bump Bottom Solder). A thin layer of 10um solder at both sides with 2-layer elements were generated for post-process analysis, and details can be seen in Fig. 3.

Instead of simulating a full package model with a long running time, each quadrant of the package with a detailed bump pattern and PCB is run separately to save overall computational time. Bumps on the center lines could not be modeled since simulations were performed for individual quadrants. To simplify the meshing, the circular bump was replaced with a square shape with the same bump area. Models went through 2 temperature cycles with ramp and dwell time following the actual BLR TC temperature profile. Plastic work density increment between 1st and 2nd cycle was used for post-processing in the 10-um thin solder layers discussed before (Both top and bottom side). From a modeling efficiency point of view, two cycles are enough for trend analysis. A volume-averaged technique was used to avoid mesh dependence and stress singularity, as shown in

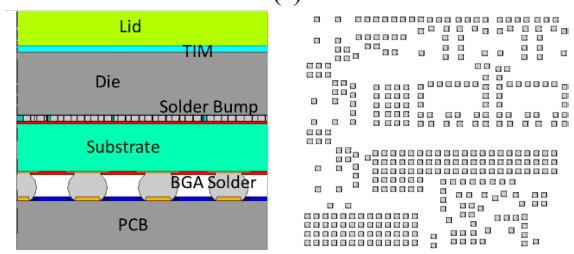
equation (1). Here, W_{avg} is the averaged plastic work density of the solder joint in a controlled volume with 10 µm thickness. W_i and V_i are the plastic work density and volume of each element in that controlled volume respectively.

$$W_{Avg} = \frac{\sum W_i V_i}{\sum V_i} \quad (1)$$

Then, those averaged plastic work density at both bump top and bottom for every solder joint were saved as modeling output. Customized MATLAB scripts were used to read the modeling tool output files and bump pattern location files to plot the damage map. This contour plot is suitable for visualization and highlighting the high-stress bump locations. Fig. 4 and Fig. 5 show the plastic work density increment map at each solder. The damage number for each bump can also be added to the plot, as shown in Fig. 6.



(a)



(b) (c)

Figure 2: (a) A quadrant of package model; (b) Cross section view; (c) Simplified bump pattern used in the quadrant model

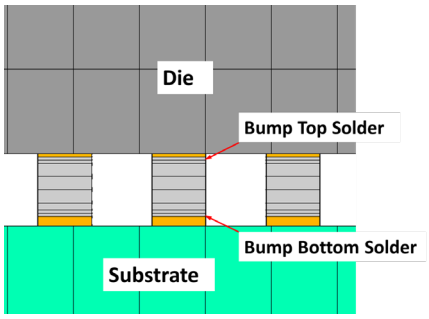
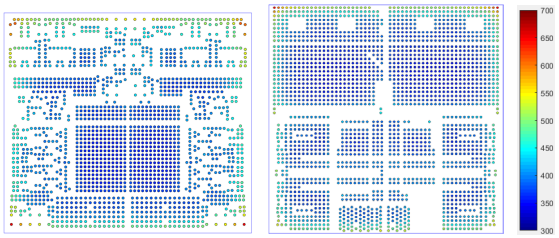


Figure 3: Cross section view of the modeled solder bump with mesh at both bump top and bottom regions

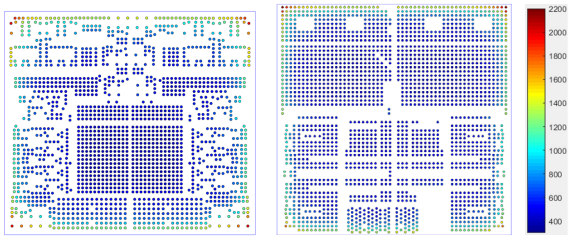
III. Discussion

By comparing all four quadrants, test vehicle B has a slightly higher damage number (Plastic work density increment at solder joint) than the referenced design C, at bump top side. Fig. 8 shows the comparison of modeling results. Since design C has 1st failure around 1000 cycles, design B may need to be more robust to pass 1000 cycles without failure. FA from original test vehicle A shows the most damage at the lower bump density area. This indicates bump density has a strong impact on solder joint cracking risk. Adding more bumps can help to disperse the stress, which has been a common practice to solve bump cracking issue. A new bump pattern is proposed with a few new bumps added at both the lower left and right corners, which are lower bump density regions in original design. By comparing to reference test vehicle C, this new bump pattern design shows all lower damage numbers at both top and bottom locations as plotted in Fig. 7. More detailed comparison can be found in Fig. 8. This gives confidence that switching from copper pillar interconnect to solder bump with new bump pattern design has a good chance to pass 1000 cycles without failure.



(a) (b)

Figure 4: Plastic work density increment map at each individual solder bump top side. (a) Test vehicle B; (b) Test vehicle C



(a) (b)

Figure 5: Plastic work density increment map at each individual solder bump bottom side. (a) Test vehicle B; (b) Test vehicle C

This paper does not intend to develop a predictive model using correlation rather than a rapid modeling approach to assess BLR reliability with limited data. Typical BLR modeling correlation needs extensive empirical test data, meaning tests have already been conducted on similar devices. However, in many cases, especially for new

development, there needs to be more data for references. This requires some non-conventional approach for quick risk assessment. It will only rule out risk partially due to the lack of total correlation but can still guide trend analysis.

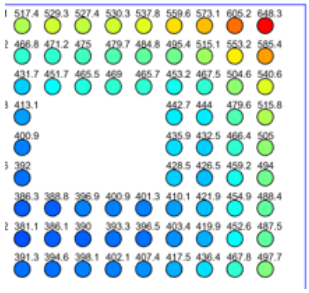
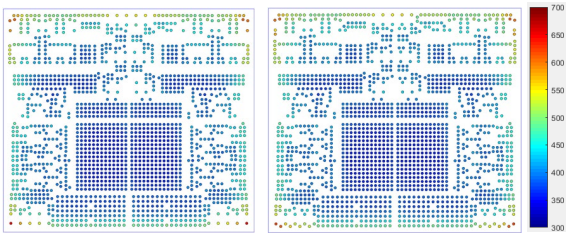
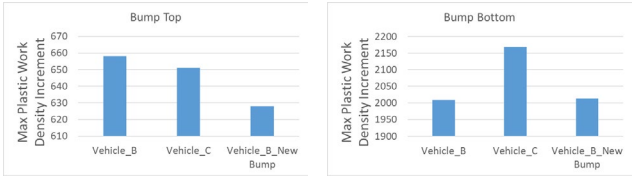


Figure 6: Example of a zoomed in region from top right corner of test vehicle C



(a) (b)

Figure 7: Plastic work density increment map at each individual solder bump top side. (a) Original bump pattern from TV_B; (b) New bump pattern



(a) (b)

Figure 8: Modeling results comparison among vehicle B, vehicle C and vehicle B with new bump pattern

BLR failure due to internal package damage is not frequently reported. One of the reasons is that a component-level reliability test is also needed as part of the reliability testing. Typically, the temperature cycle condition for the component level is harsher than the board level. For example, a component level can be -65^{0}C/ 150^{0}C while a board level will be -40^{0}C/125^{0}C. In many cases, package internal failure can be captured during the component-level test. Design optimization or extra attention may have already been given during the design stage. Thus, it is rare to expect BLR failure due to package internal damage. However, component level tests can never capture the impact of PCB. So, it reminds us that package internal damage during BLR TC test must be addressed.

IIII. Summary

BLR failure can happen at the external solder joint between the package and PCB and inside the package. This paper discussed internal solder cracking, which caused early BLR failure during the BLR TC test. The FEA-based model assessed the reliability performance when replacing the Cu pillar interconnect with a conventional solder bump. Bump density impact was captured in the model to enable design optimization.

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