American Semiconductor®
Reliably Thin Electronics

P-WLCSP: 6-Side Protected WLCSP

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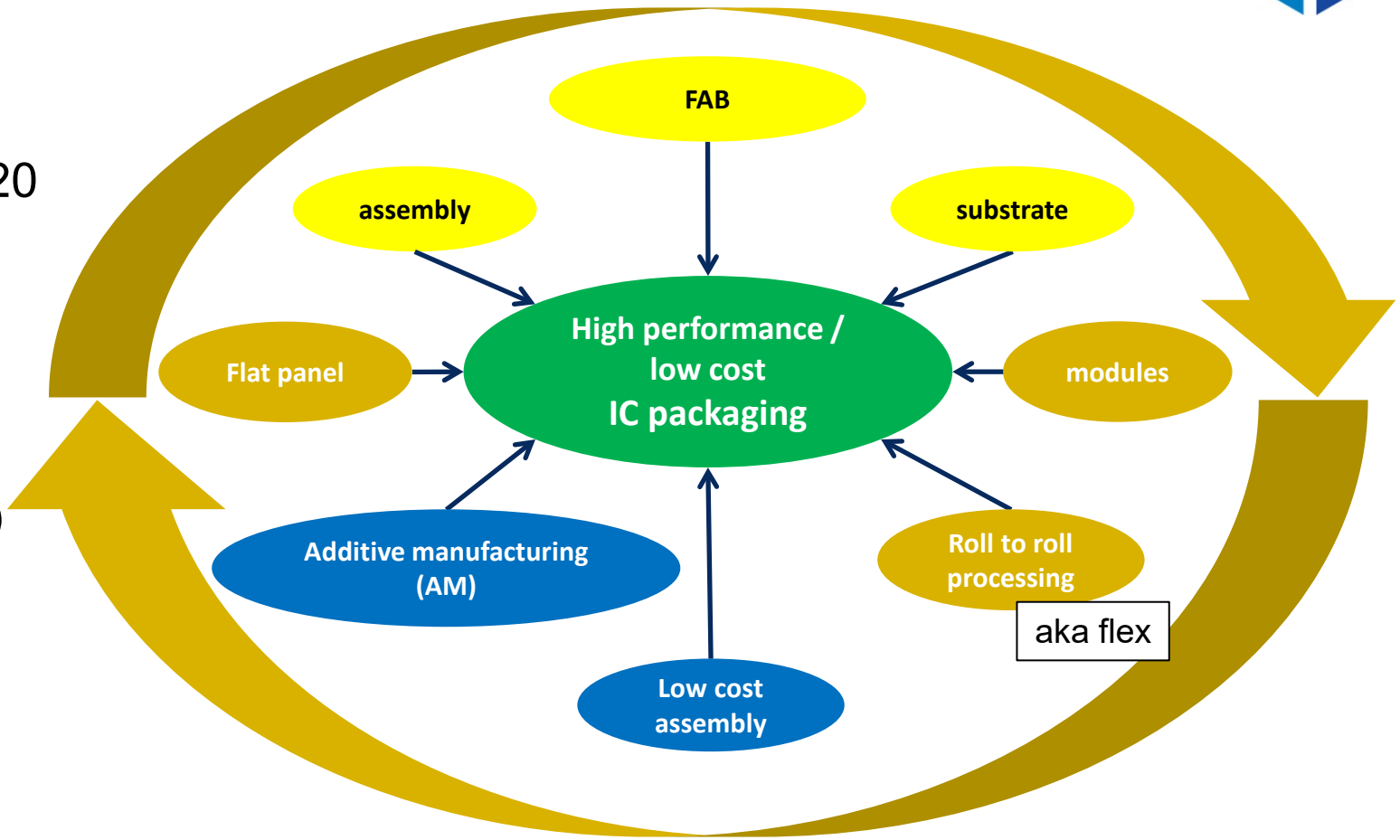
Chip Scale Packaging

- WLCSP
  - With the advent of bumped die, new IC packages evolved
  - Low IO WLCSP, High IO FC (flip chip), CBGA (ceramic ball grid array) and PBGA (plastic BGA)
  - Reliability for bumped die packages evolved differently for high and low IO bumped die
- Active side protection became important with the entry of high IO die
  - Bumps on traditional final passivation resulted in unacceptable reliability
  - Addressed with a BEOL (back end of line) application of PSB (passivation stress buffer)
- As devices became more complex, reliability requirements increased
  - PSB based processes no longer provided the required reliability
  - Higher IO and better reliability evolved with 6-side protected non-WL CSP (aka Fan Out)
  - Example: M-Series, eWLB, etc.
- Low IO CSP (aka Fan In) reliability was improved by using non-WL 6-side protected process
- Non-WL CSP includes die reconstitution, expensive tapes, molding operations, and resolves the reliability issues for FI, but the added cost and process complexity was and is far from optimal

Synergistic approach to address non-WL cost and complexity

Packaging technology needs to improve and evolve faster

- Packaging technologies have a 10-20 yr cycle from concept to HVM (BGA pkg, bumping & FO for example)
- Technologies tend to silo over time (slowed down innovation-less of an issue with long development cycles)
- Learning can be applied from other technology areas to advance, and decrease time to market for new packaging
- Enabling approaches and Process simplification



MASIP synergistic technology approach

Holistic approach to simplify processes

IC packaging: wafer level FI

IC FAB, assembly, substrate silos

Simplified single die pkg enabled by bumped die → PSB for top side protection use standard IC pkg PSB →

- FO full encapsulation for required reliability
- Adaptive patterning to improve yields

The next step in high reliability FI packaging

FHE (flexible hybrid electronics): SoP (FLEX-C)

R2R (flex) & FAB silos

Need for more dense devices enabled by flexible die (SoP) → PSB for top & bottom protection use standard IC pkg PSB →

- Adaptive processing for yield and lower cost
- Full encapsulation with std full wafer FI process

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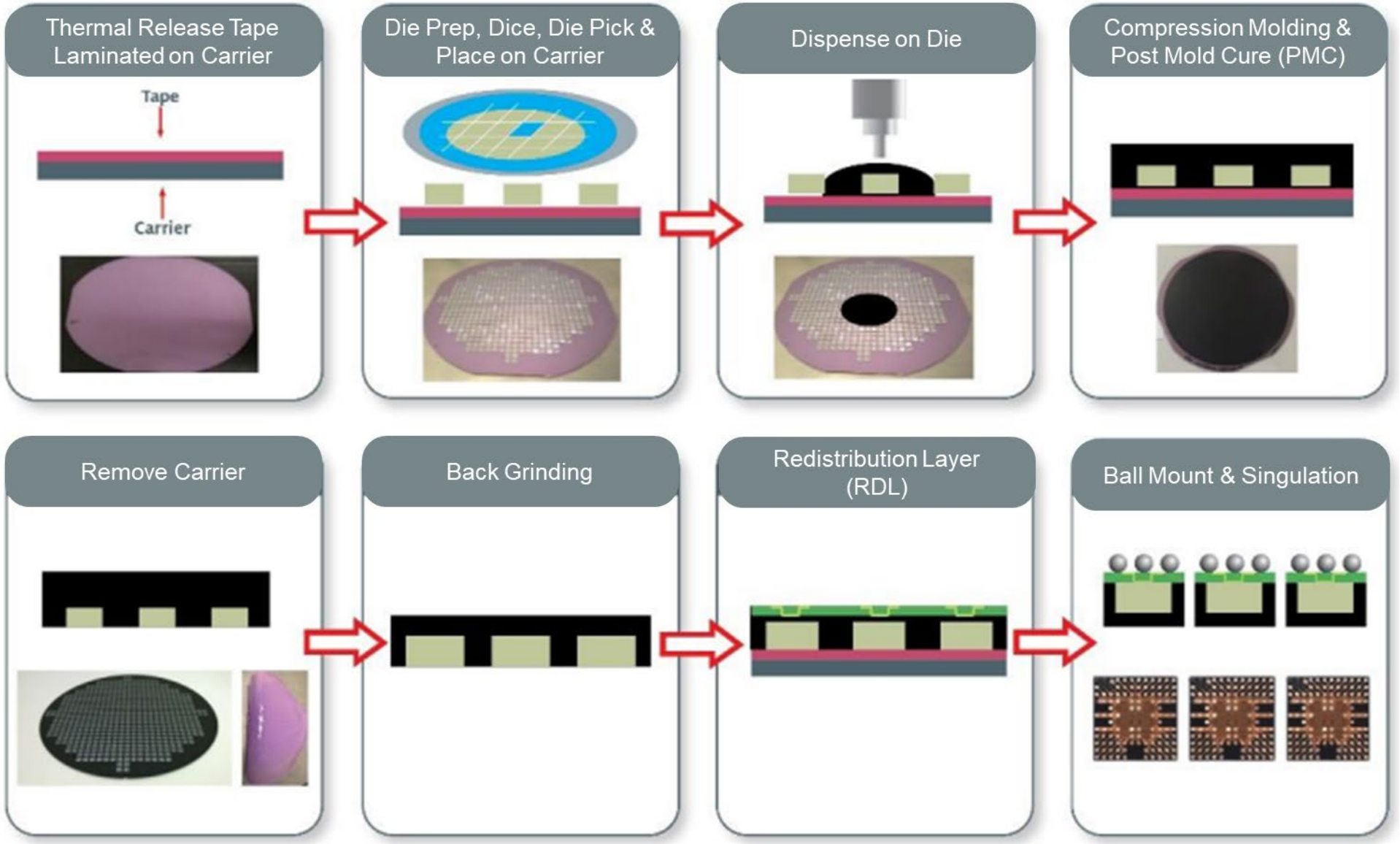
6-side protection: P-WLCSP

- "Protected WLCSP" (P-WLCSP) resolves Cost and Complexity of non-WL for FI
  - 6-side protection without the cost and complexity on non-WL FO type processes
  - P-WLCSP does not require pre-package die thinning, dicing or reconstitution
  - P-WLCSP Substantially reduce the equipment and process steps required for processing
  - Material reductions with the elimination of dicing tape and molding materials
- Example: SoP-TM™ 6-side protected P-WLCSP introduced at IMAPS 2021
  - Full protection, without the cost/complexity of non-WL FO processes used for protected CSP FI
  - 300mm process utilizes polyimide for encasement
  - The process includes maskless processing and high temperature temporary bonding
  - Adaptive processing expands the selection of PIs available for stress balancing
  - Final singulation (dicing) speed enhancement due to P-WLCSP PI scribe streets
- Enabling ultra-thin devices
  - Reduced die thickness improves capability for through silicon via (TSV) size and pitch
  - Enables high-temperature backside RDL (B-RDL) and heat sinks
  - CMOS silicon thicknesses is typically 10-15um, but can be adjusted as needed

CSP – eWLB

eWLB – Embedded Wafer Level BGA (not really a wafer level process)



Source: J. Chao, R. Trichur, "How to Prevent High Wafer Warpage in Fan-in and Fan-out Wafer Level Packaging," 3DInCites, Jan. 19, 2022

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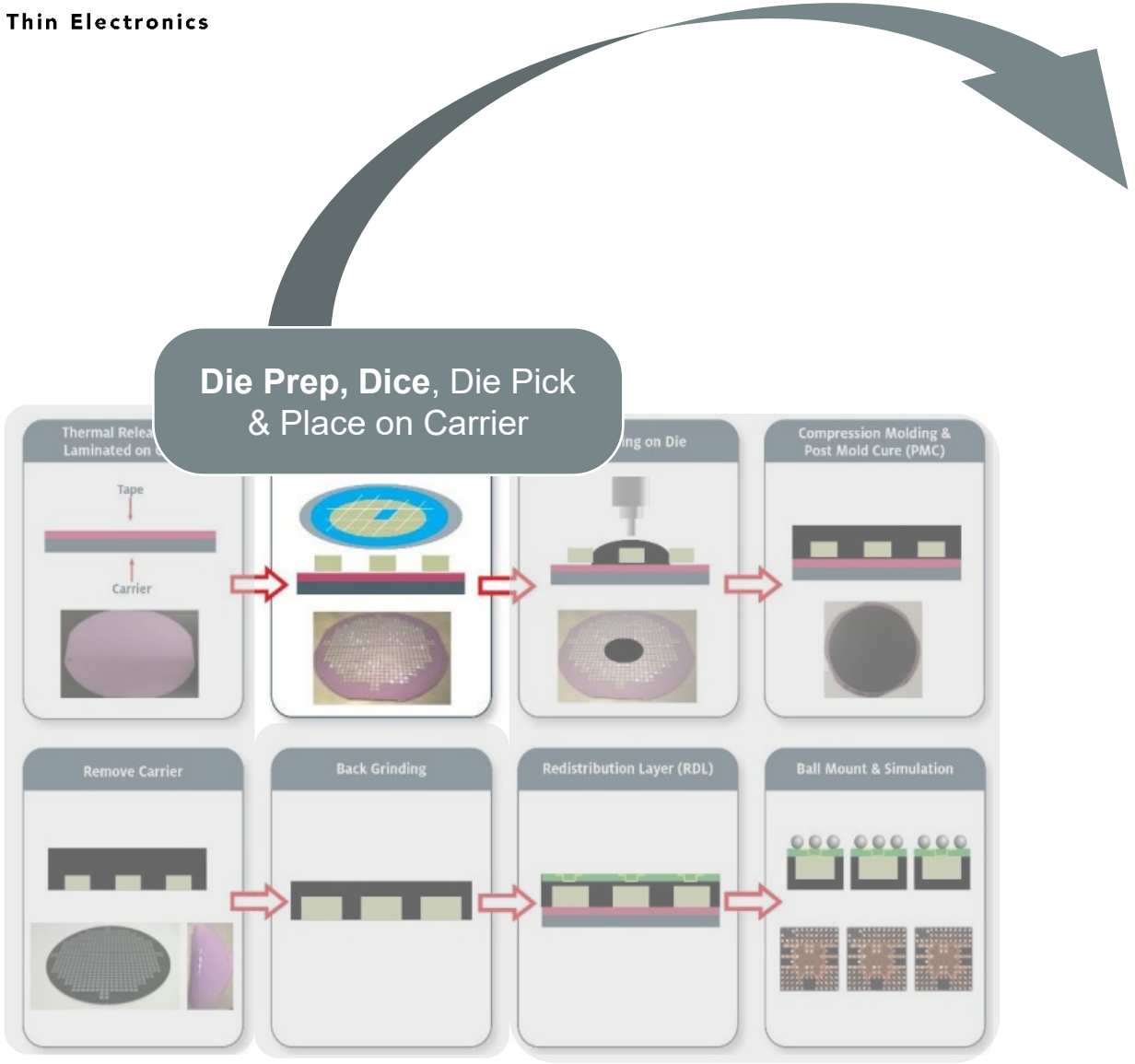


Die Prep Isn't free!

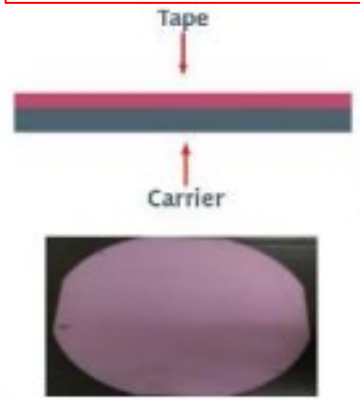
- Tape and Taping
- Grinding
- Singulation

These steps are required and add cost to conventional CSP

SoP-TM vs eWLB

Die Prep
- Tape and Taping
- Grinding
- Singulation

3. Mount on carrier. No Tape.

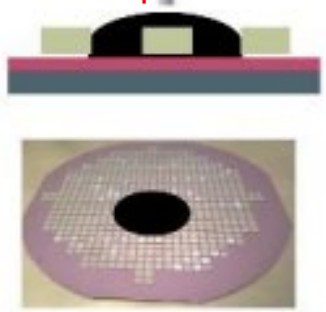


~~Pick & Place on Carrier~~

No Die prep, No Reconstitution

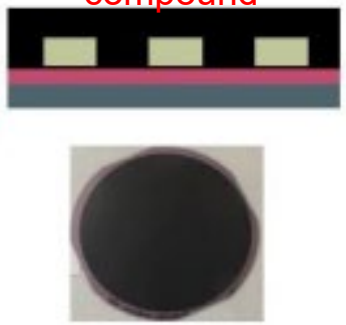
1. Trench and Dispense

eliminate mold compound



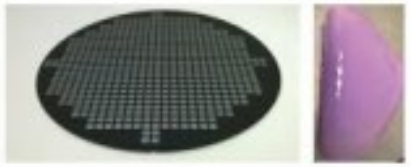
5. Backside Polymerization

eliminate mold compound



6. Demount to Tape

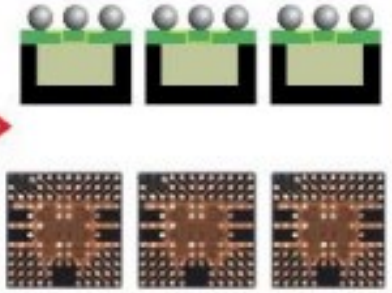
No wet cleans



4. Grind

2. WL-RDL/ uBump

7. Singulate. Ball mount optional



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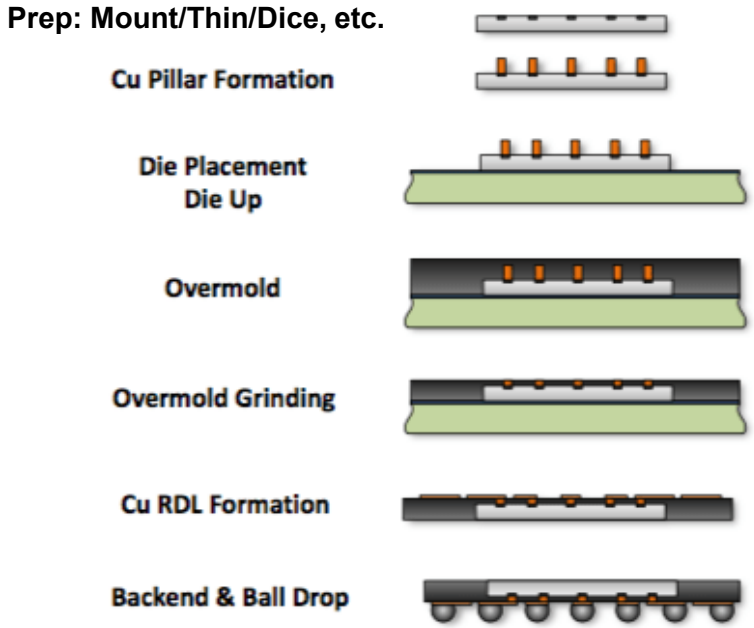
SoP-TM vs non-WL CSP
another example

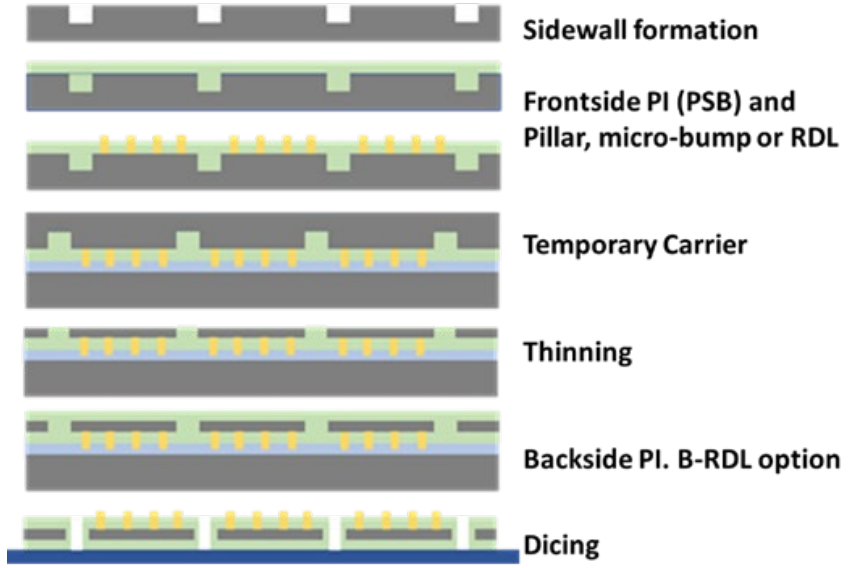
- Comparison of non-WL CSP and P-WLCSP SoP process provides an understanding of cost and complexity of protected packaging technology.

Die Up - M-Series



M-Series CSP FO Process. Source: SemicondcutorEngineering Feb. 2018

P-WLCSP – SoP-TM



FleX-TM Protected WLCSP, U.S. Patent 9,082,881

- P-WLCSP processing provides cost reduction and performance improvement in CSP FI applications
- Produce robust ultra-thin devices for SiP applications - chiplets and heterogeneous integration
- Higher pin-counts and thinner board assemblies are macrotrends in modern electronics
- Reducing layer thicknesses, along with the opportunity to connect on top and bottom of die without any significant cost penalty is significant.

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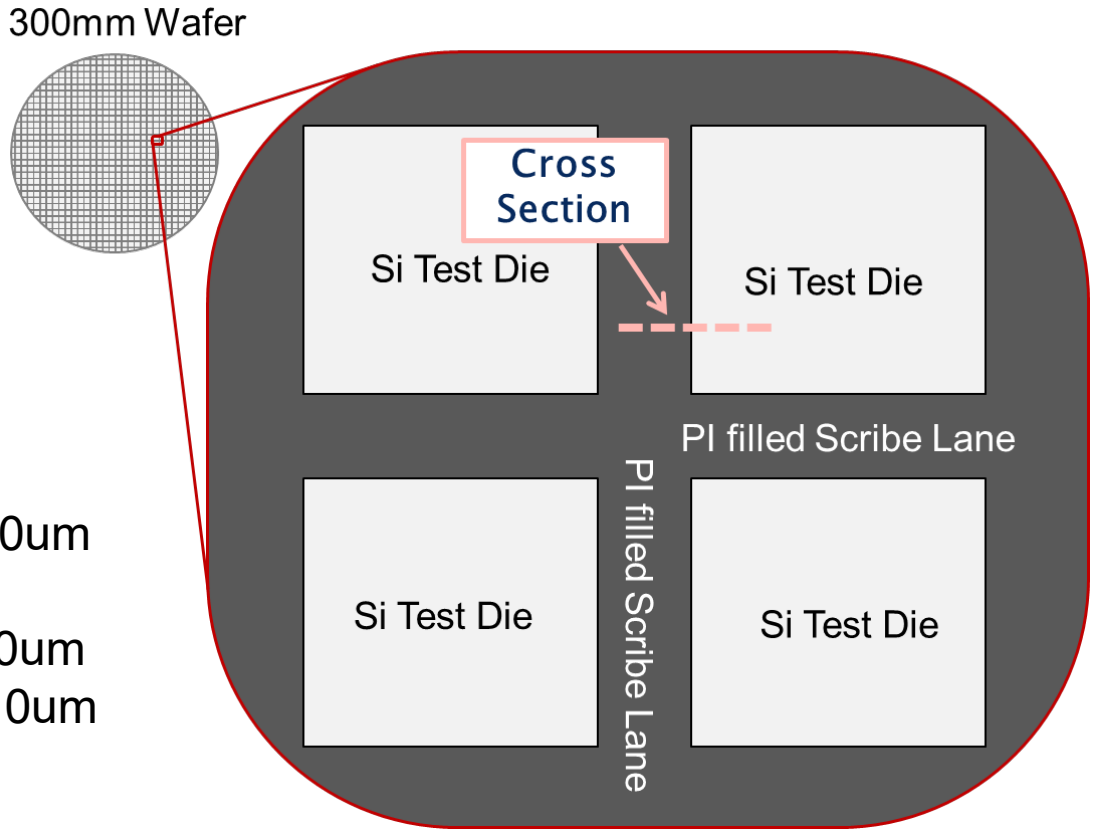
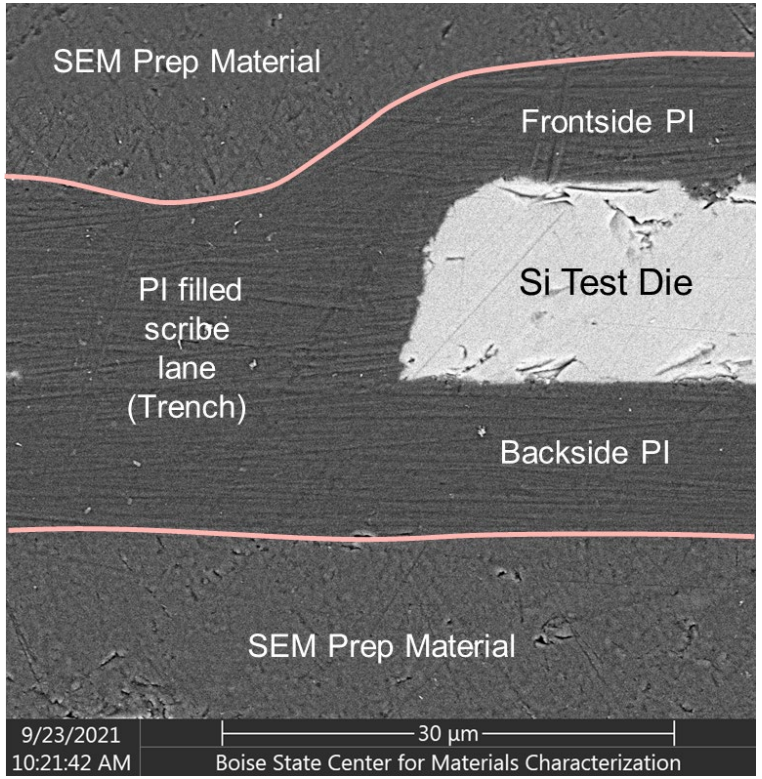
FleX-TM 6-side protected SoP WLCSP

1st Silicon Results announced at IMAPS 2021

SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection utilizes polyimide for encasement. The process includes maskless processing, high temperature temporary bonding, final singulation with extremely fast laser dicing



Trench 45um
Frontside PI 10um
Silicon 11um
Backside PI 10um
Sidewall PI ~10um



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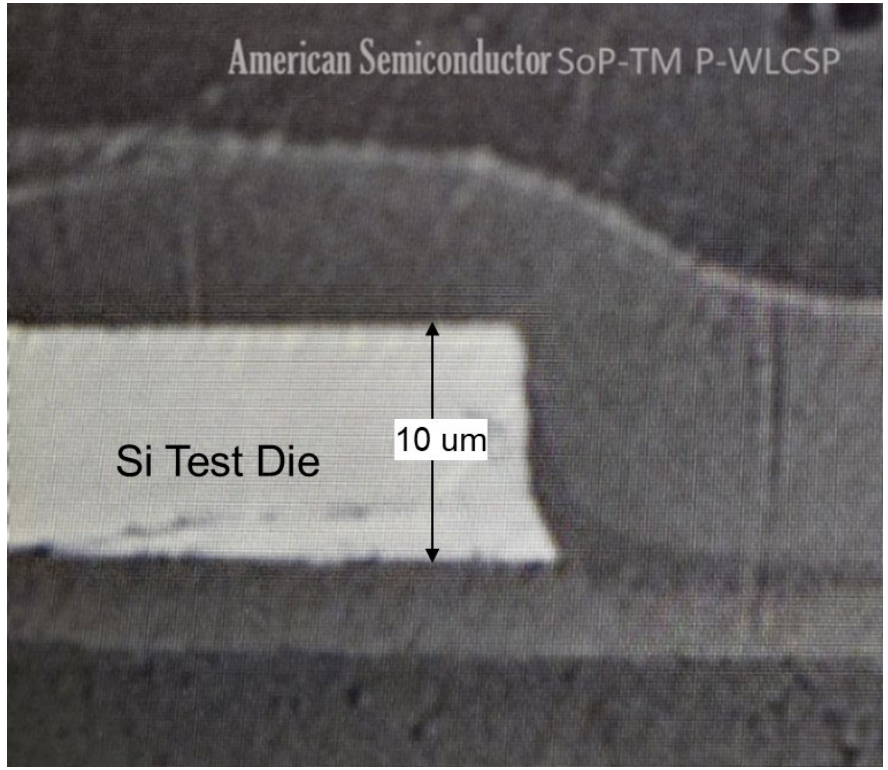
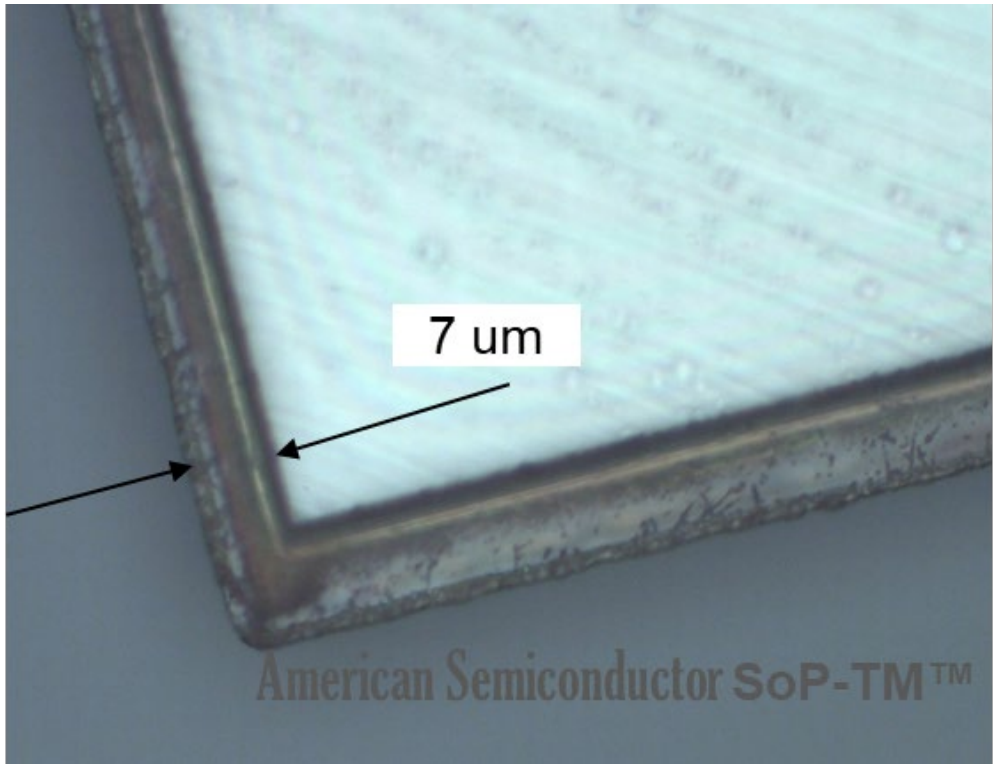
Current Data for SoP-TM

SoP-TM development update

Current progress for SoP-TM high efficiency, low-cost, P-WLCSP with 6-side protection
Improved sidewall formation and demonstration of laser singulation





Trench 45um
Top PI (PSB) 10um
Silicon 10um
Bottom PI (PSB) 4um
Sidewall PI (PSB) ~7um

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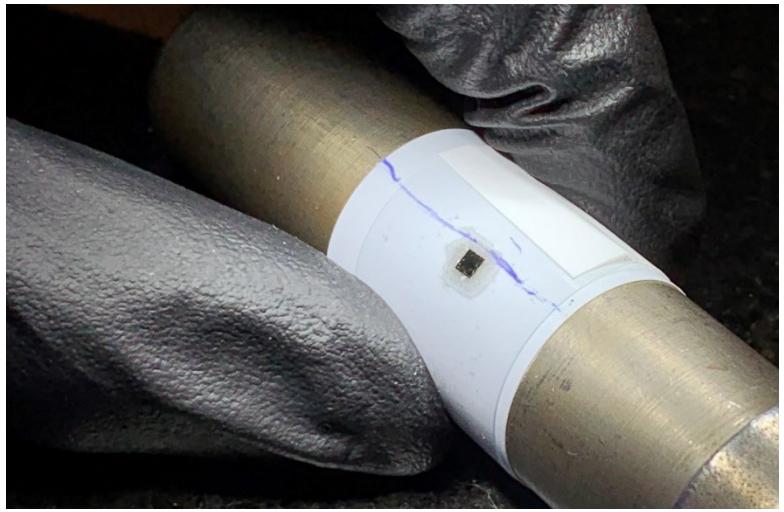
SoP-TM First Mechanical Test



Dynamic Bend Test

- ASI TEST003 derived from ASTM D522-93a
- Chips mounted on flex coupons of PET or PI
- Robotic cycling at specific (RoC) for bend and release in concave and convex orientation
- Test: 10mm RoC, 10,000 cycles

Static RoC Testing

- SoP-TM Test Chip, no coupon
- Manual conformance to RoC mandrel

SoP-TM Mechanical Reliability

Test	Concave	Convex	
ASI TEST003 10mm, 10,000 cycles	PASS	PASS	SoP- TM, ACA FC on PET
Static RoC 12 mm	PASS	PASS	SoP-TM only
Static RoC 10 mm	PASS	PASS	SoP-TM only
Static RoC 8 mm	PASS	PASS	SoP-TM only
Static RoC 7 mm	PASS	PASS	SoP-TM only
Static RoC 6 mm	PASS	PASS	SoP-TM only
Static RoC 5 mm	PASS	PASS	SoP-TM only
Static RoC 4 mm	PASS	PASS	SoP-TM only
Static RoC 3 mm	PASS	PASS	SoP-TM only
Static RoC 2.5 mm	PASS	PASS	SoP-TM only
Static RoC 2 mm	PASS	PASS	SoP-TM only
Static RoC 1.5 mm	Cracked	Cracked	SoP-TM only

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SoP-TM Summary

SoP reduces processing steps and material usage for protected fan-in

- True wafer level CSP process (WLCSP) eliminates pre-packaging wafer prep:
  - No pre-package wafer grind
  - No pre-package dicing tape
  - No pre-package singulation
  - No pick-and-place for reconstitution
- Die reconstitution eliminated
- Maskless PSB
- Only 1 thinning step required – utilizes clean dry release temporary adhesive
- Low cost reusable silicon carrier wafer
- Only 1 singulation step required
- Only 1 tape layer
- Standard wafer level processing for bumps, pillars and/or RDL
- Overmold process eliminated

50% fewer steps –> 50% less capital, or 2X capacity increase

50% Less labor cost –> Cycletime 50% less

30-50% Less material cost –> Improves cash flow

SoP – Lowest Cost Protected Fan-In

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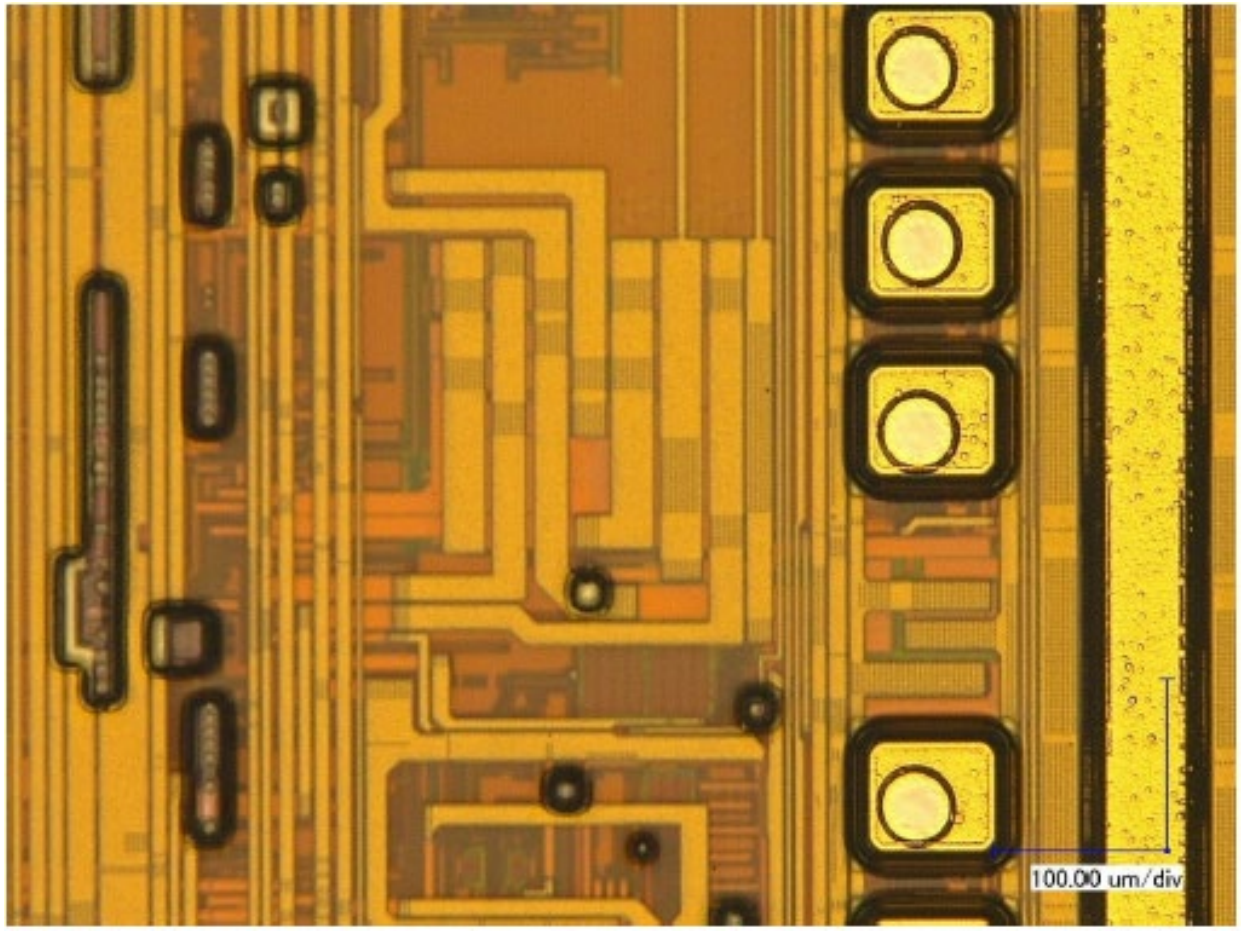
Ex: Synergistic approach applied to SoP-TM

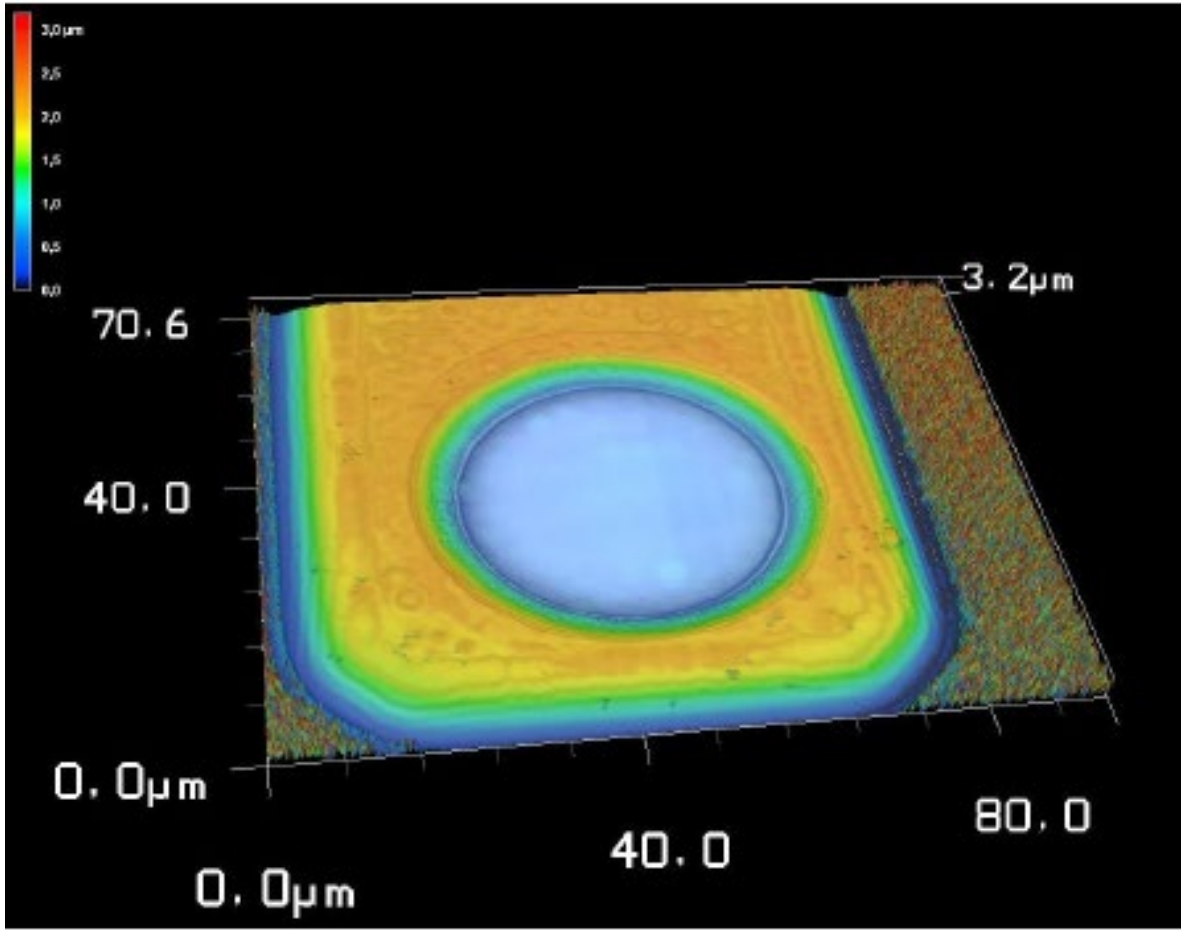
Dry via formation: background (evolution)

Organic dielectric via opening process history						
1.	Non-photo dielectric	Resist	Mask	Wet Open	Wet Clean	Metallization
2.	PSPI	***No Resist***	Mask	Wet Open	Wet Clean	Metallization
		Eliminate resist (dielectric with photopak)				
3.	Adaptive Pattern (M-Series)		***No Mask***	Wet Open	Wet Clean	Metallization
			Eliminate Mask			
4.	Adaptive Process **(SoP-TM)**		***No Mask***	***Dry Open***	***Dry Clean***	Metallization
				Eliminates wet processing (dry process)		
				Restores option for dielectrics (no photopak)		

Initial feasibility evaluation

- Lab feasibility proof: Clean, crisp holes are approximately 40um in diameter
  - Clean pad openings in PI
  - Promising, but pad size and alignment fail to meet requirements





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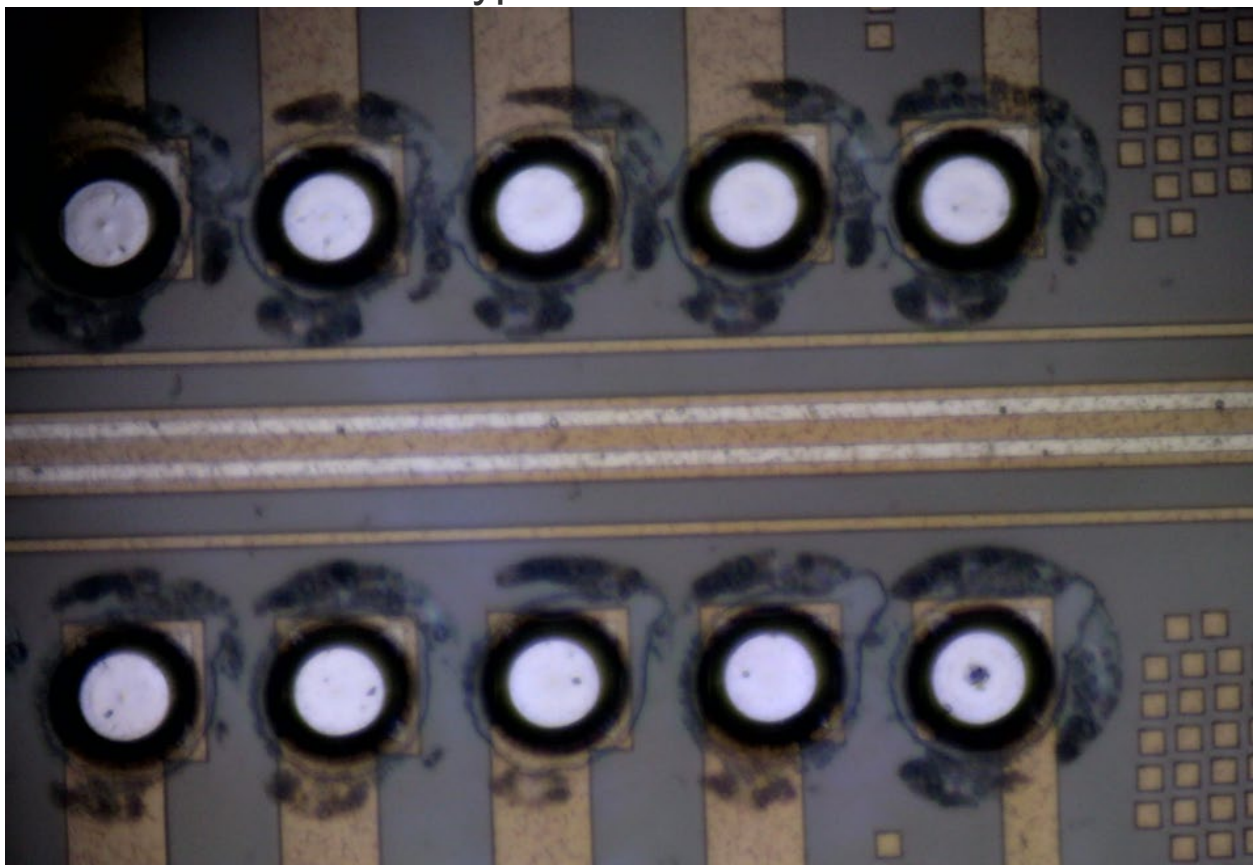
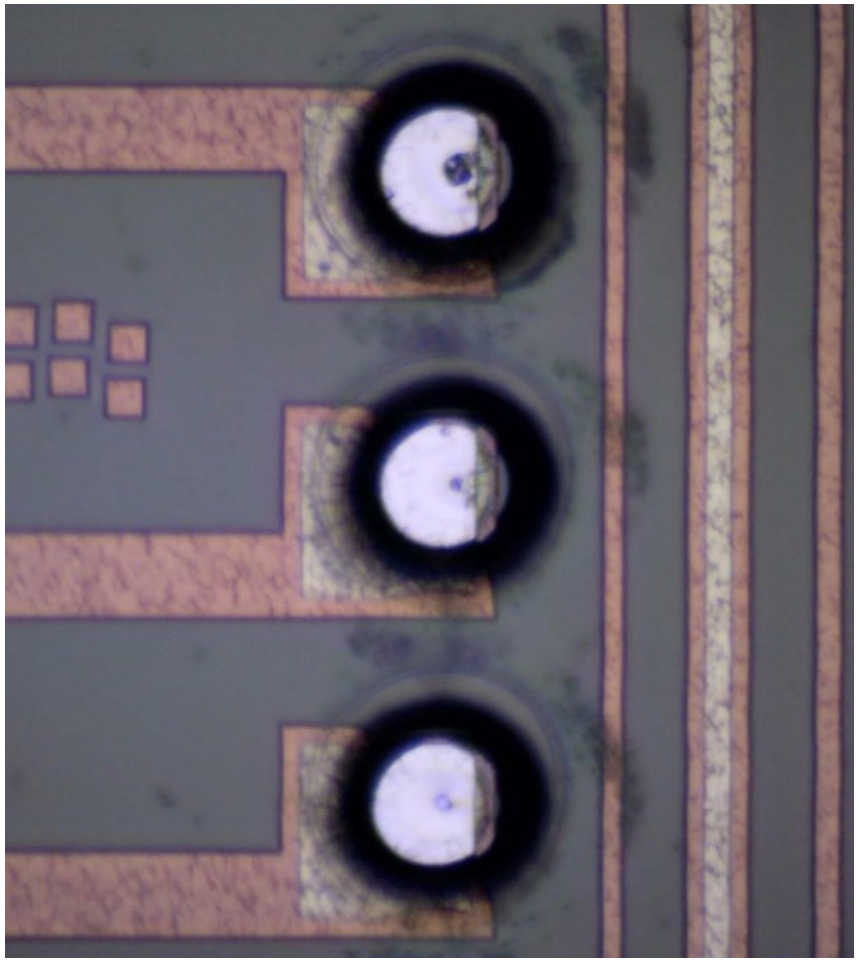
More Process Development

- Test wafers processed onsite at ASI showed limitations for the demo recipes
  - Burn through and other damage
  - Misalignment (Inconsistent placement)
  - Pad contamination typical of what is seen in literature





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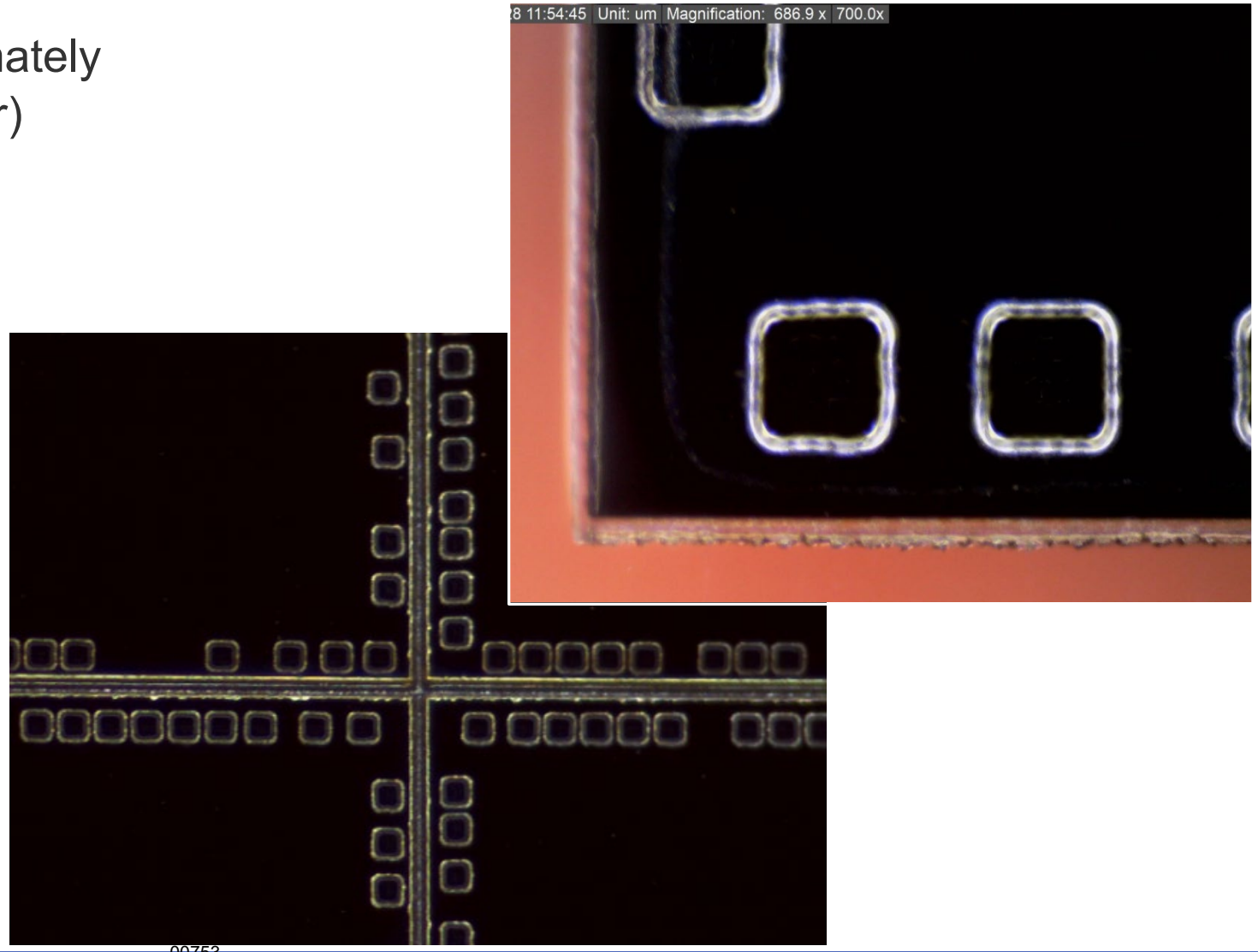
SoP-TM Maskless Processing

SoP-TM process

16x improvement in throughput approximately
4 wph (manual process, with typical wafer)

- Pad openings:
  - Maskless
  - Uniform
  - Accurately placed
  - Exceptionally clean
  - Small and large pad capable
  - More than 25 200mm wafers per shift



All dry processing

not just adaptive patterning…

Adaptive PROCESSING!

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FlexTech Alliance
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Packaging, Assembly Test and Related Services

MASIP LLC- Phoenix, AZ

MASIP LLC holistic approaches to products/markets

- Market and materials/process trends (IC pkg focus)
- Manufacturing optimization (FA and rel assessments)
- Material and process development & implementation
- Specific application materials and process assessment

Wide experience:

- Electronics-FAB, packaging and assembly
  - early publications and patents for FI & FO (RCP)
- **Material and development**
  - Implemented 1st 2 PSPSI materials at Motorola
  - IP on materials/processes for WSS/flux/AM
- **Material/interface experience and Rel modeling**
  - Solving failure mechanisms (surface/interfaces)
  - Appling material principles to key areas
    - Reliability modeling
    - Processing
    - Material development

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Thank You

SoP packaging supported in part through Joint Development with HD MicroSystems

Thanks to Disco for their on-going support of ultra-thin processing requirements

Special thanks to Plasma-Therm for their support of special processing requirements

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