ASE GROUP

18TH INTERNATIONAL CONFERENCE & EXHIBITION ON DEVICE PACKAGING
FOUNTAIN HILLS, AZ · WWW.DEVICEPACKAGING.ORG · MARCH 7-10, 2022

Advanced Fanout Embedded Bridge Packaging Technology for Chiplets Integration

Dr. Lihong Cao
ASE (US) Inc.
Lihong.cao@aseus.com

Outline

- **Introduction**
  - Semiconductor trend and Chiplets Integration
- **Advanced Fanout Embedded Bridge Packaging Technology**
  - Introduction of TVs and process flow
- **Process Development and Discussion**
  - Warpage control and reliability assessment
- **Summary**

Key Semiconductor Growth Drivers

IoT/IoE

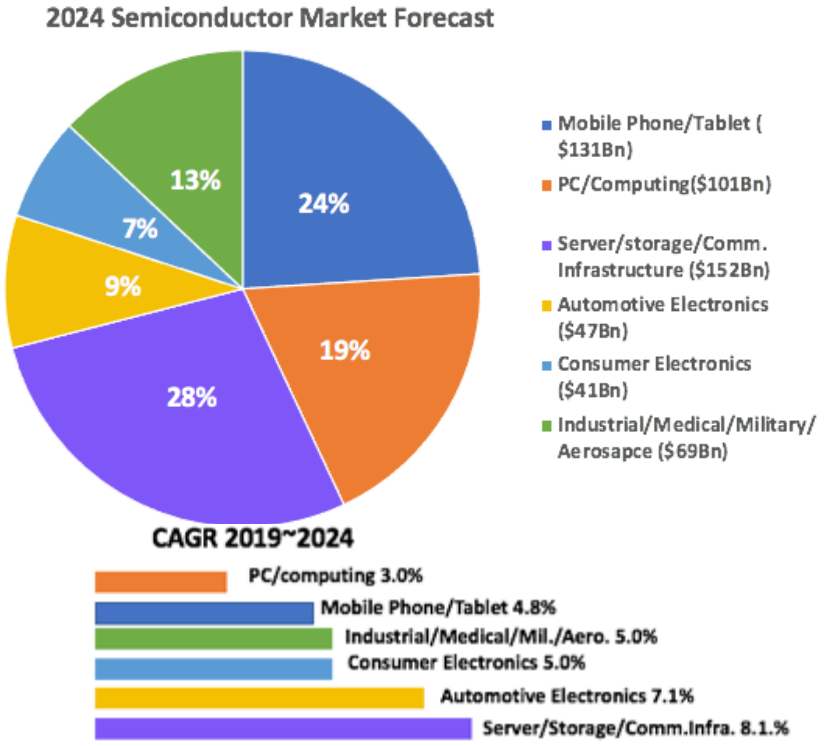
Automation

5G/Edge

HPC

Smart Everything

AI/ML

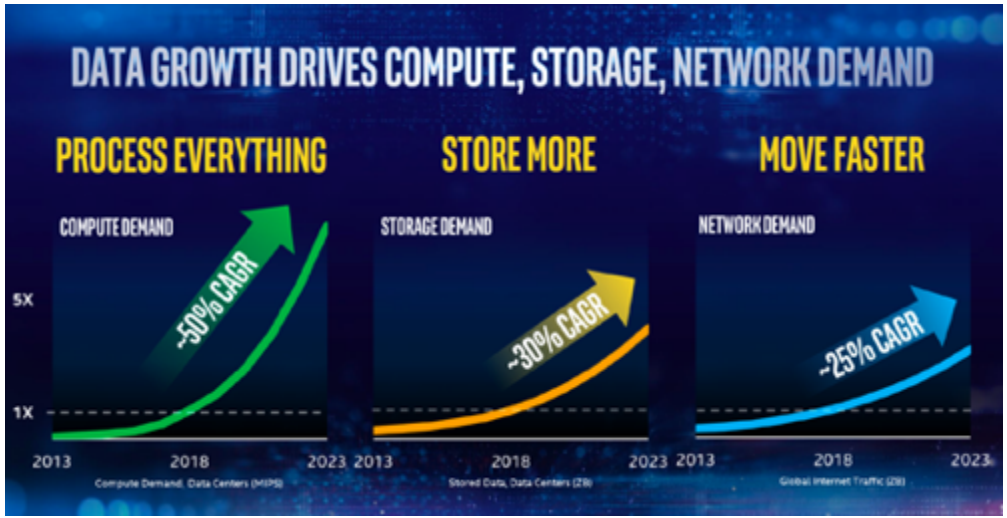


Source Prismark 2020 in IMAPS

Data Growth Drives Demand for High Performance

- ***Worldwide data grow to 175 zettabytes by 2025 (IDC 2020)***
- ***Global mobile data traffic increase to 77EB/M in 2022 exponentially (Statista 2020)***
- ***Server, network, storage growths (+1000 exabyte/M)***

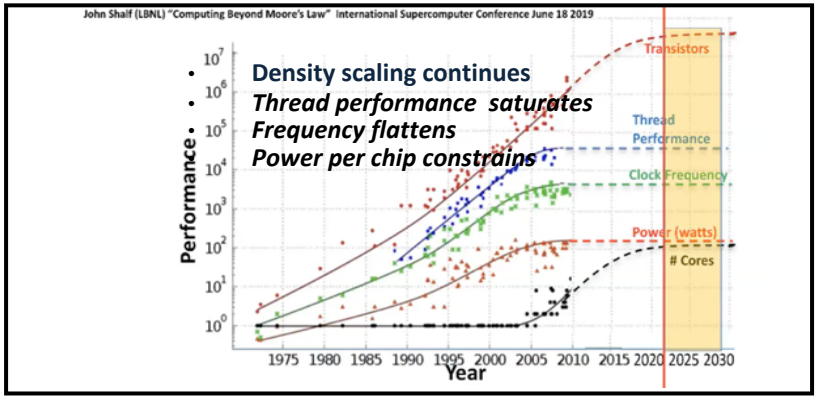
Source IDC 2020



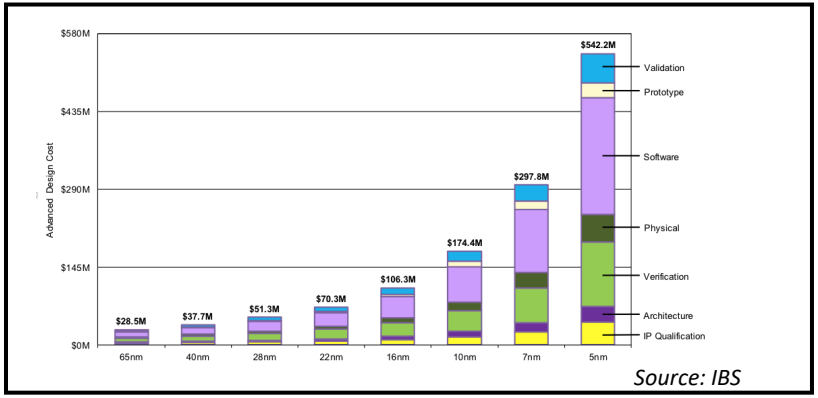
Source: Intel Investor Day 2019

Barriers & New Technology Innovation Drivers

Driver 1- Density Scaling Increase

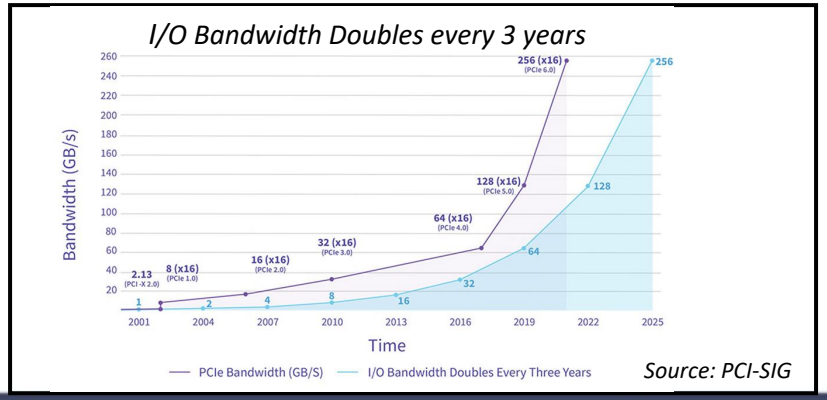


Driver 2- Si Node Dev Cost



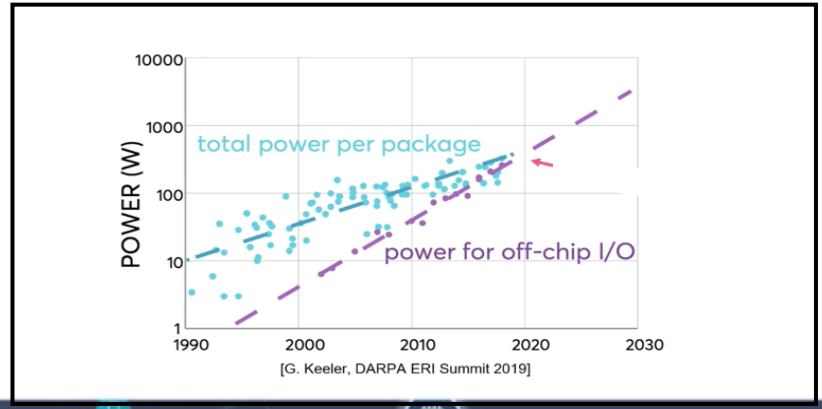
Source: IBS

Driver 3- High performance requirement



Source: PCI-SIG

Driver 4 – High power consumption

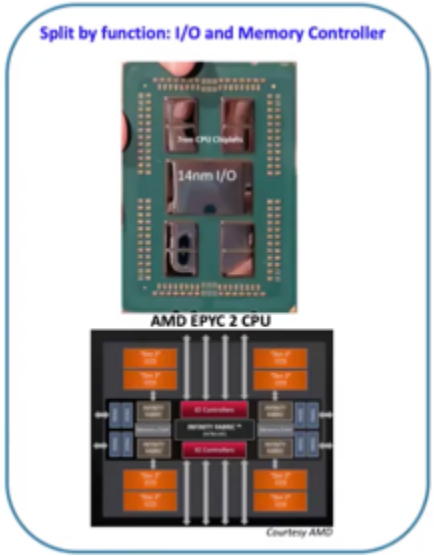


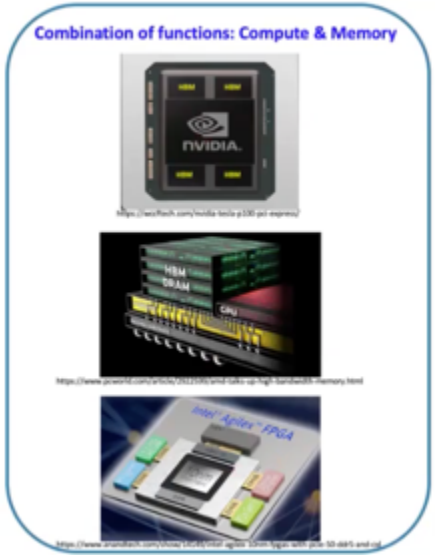
Chiplets and Heterogeneous Integration

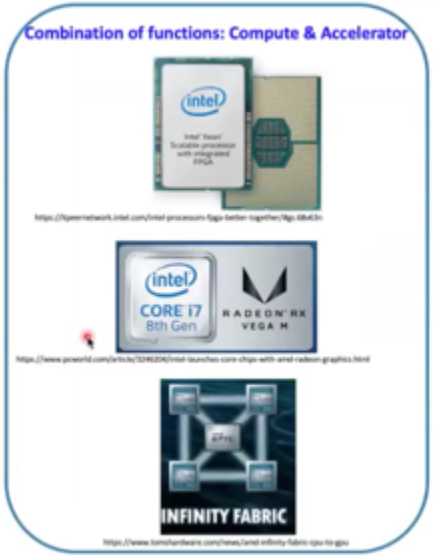
- ***New Logical partitioning and Disaggregated SoC***
- ***Heterogeneous integration offers a solution for performance scaling following Moore's Law***

Drivers & Benefits

- Mix & Match systems
  --Different Si Nodes
- Reuse IPs
- System flexibility
  --Processors, accelerator
- Performance optimization
  --Low latency, high bandwidth
- Time to Market
- Low Cost



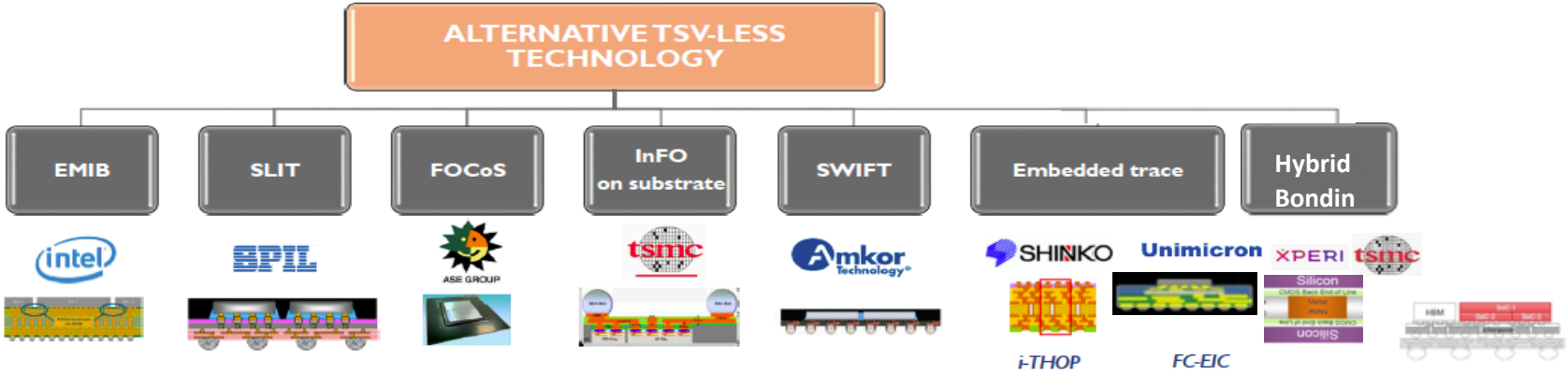




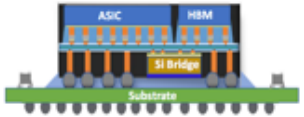
Source: IBM ECTC 2020

Advanced HD Fanout Packaging Technology

- ***Alternative Si TSV-Less solutions to reduce cost***
  - *Embedded Si die to replace large Si interposer*
  - *Fanout RDL interposer with L/S > 1/1um*
  - *Better electrical performance (less insertion loss) due to no Si TSV*



Fanout embedded Si bridge on substrate → **FOCoS-B**

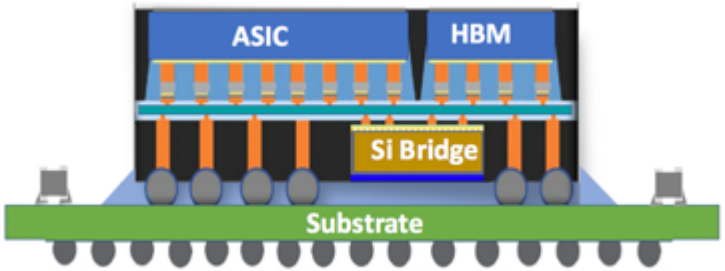


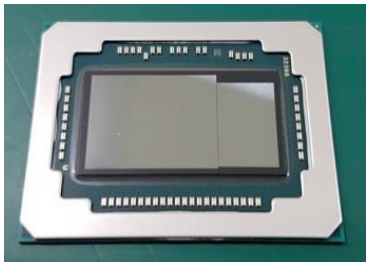
Outline

- Introduction
  - Semiconductor trend and Chiplets Integration
- **Advanced Fanout Embedded Bridge Packaging Technology**
  - Introduction of TVs and process flow
- Process Development and Discussion
  - Warpage control and reliability assessment
- Summary

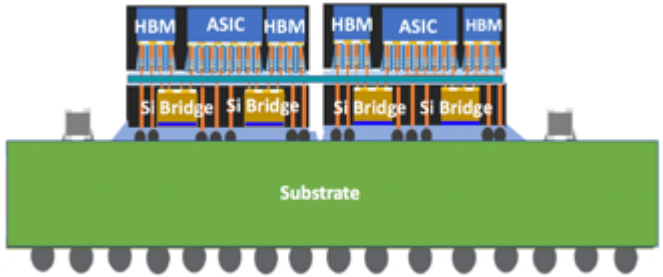
ASE FOCoS-B TV Structure

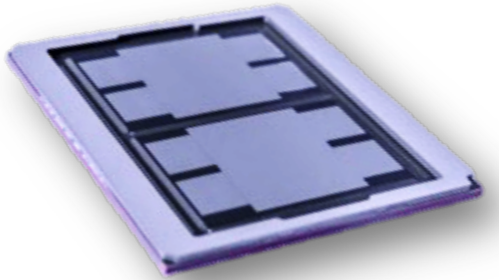
➢ 2 Types of FOCoS-B TVs





- *1ASIC + 1HBM +1 Si Bridge die*
- *Module size: 27x14 mm²*
- *1 RDL, L/S 10/10 um*
- *Si Bridge Die L/S 0.8/0.8um*
- *Package size: 40x30 mm²*

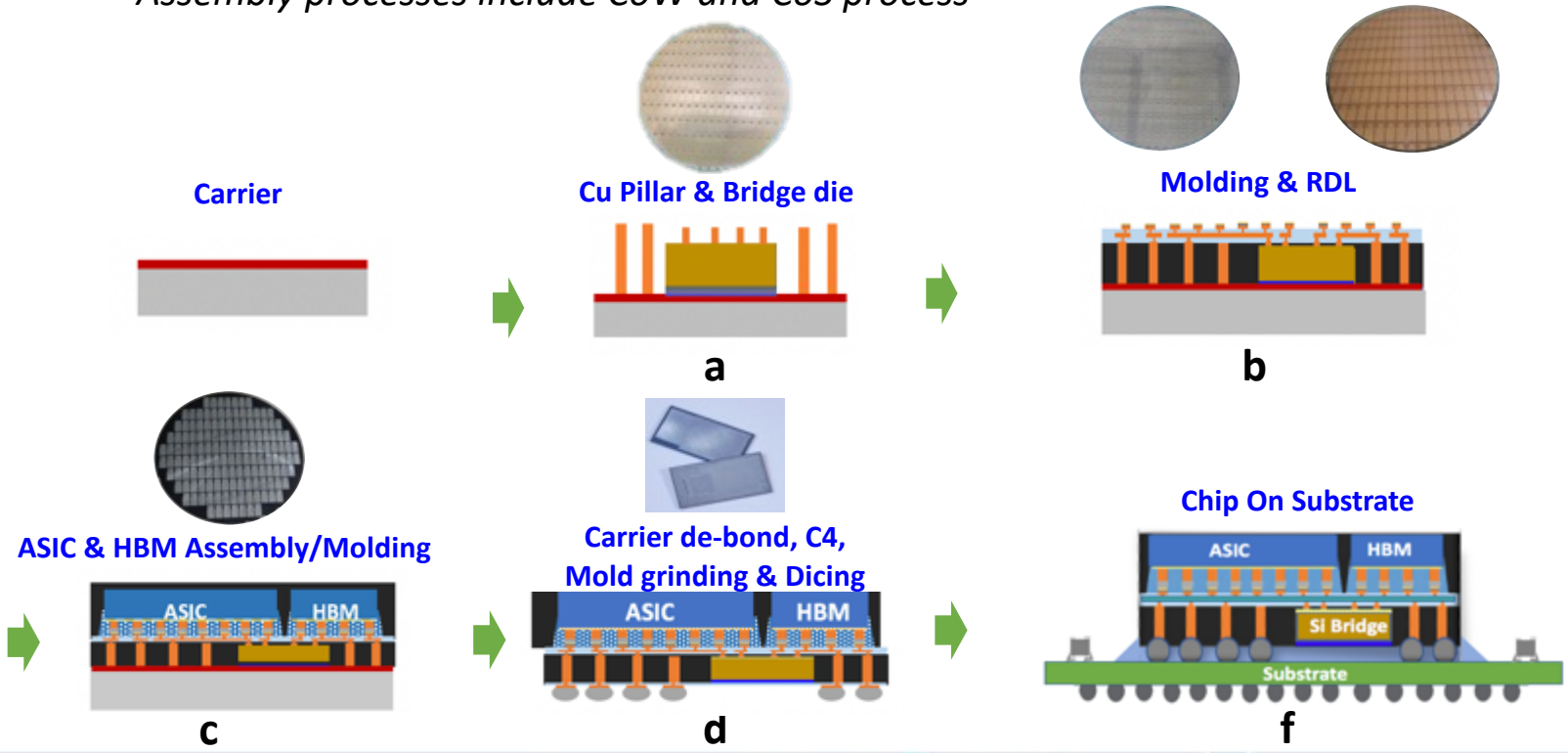




- *2ASIC + 4HBM +4 Si Bridge die*
- *Module size: 47x31 mm²*
- *1 RDL, L/S 10/10 um*
- *Si Bridge Die L/S 0.8/0.8um*
- *Package size: 78x70 mm²*
- *Total 10 chiplets in MCM package*

ASE FOCoS-B Process Flow

- **Key Process steps**
  - *Bumping processes include Cu Pillar, Cu RDL and C4 bump*
  - *Assembly processes include CoW and CoS process*

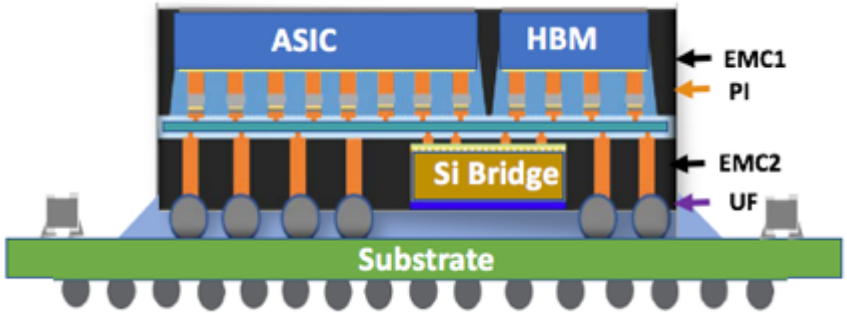


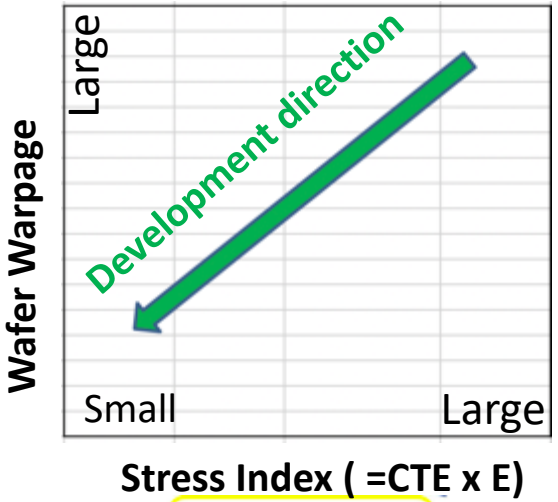
Outline

- **Introduction**
  - Semiconductor trend and Chiplets Integration
- **Advanced Fanout Embedded Bridge Packaging Technology**
  - Introduction of TVs and process flow
- **Process Development and Discussion**
  - Warpage control and reliability assessment
- **Summary**

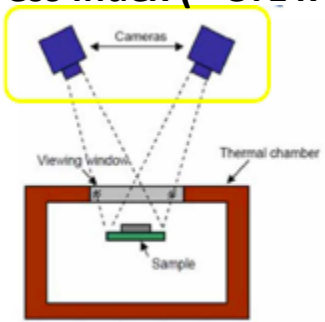
FOCoS-B Material Selection and Warpage Control

- **FOCoS-B process materials impact on warpage**
  - *Various packaging materials (EMC, UF, PI, RDL etc.)*
  - *Key factors CTE, E, Stress Index play important roles*
  - *Stress Index is the key factor for warpage control*





- **Warpage measured by Advanced Metrology Analyzer (aMA) & Shadow Moiré**
  - aMA non-contact three-dimensional digital image correlation

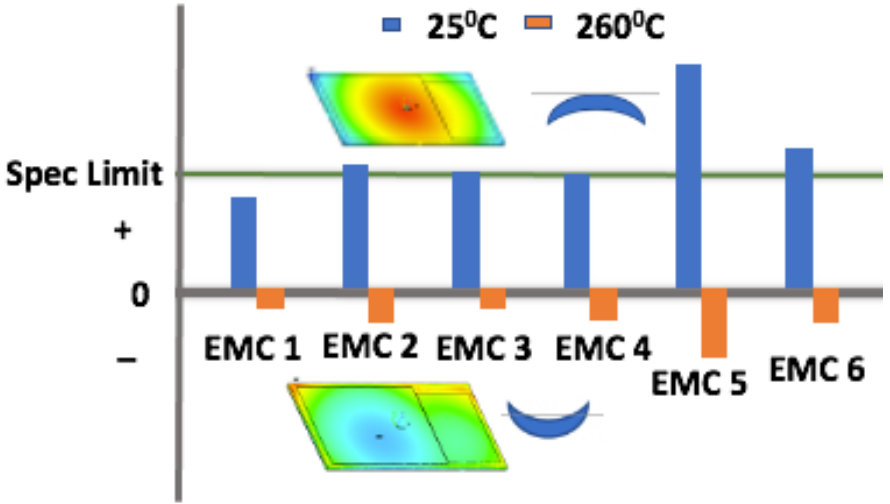


FOCoS-B Molding Material Selection

➢ Mold compound material impact on warpage

- ***Experiments on warpage for different EMCs***
  - EMC with moderated stress index yielded lower warpage (EMC1)
  - EMC with too low or too high CTE or E combinations not good for warpage control

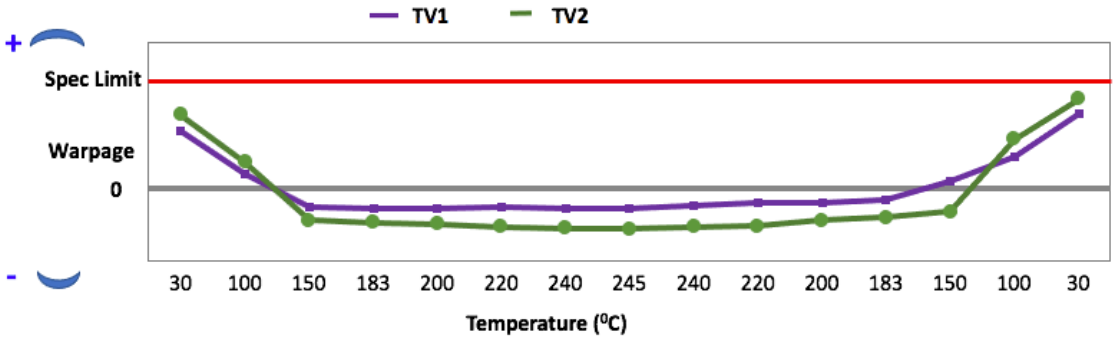
CPD	CTE (ppm/˚C)	Modulus (GPa)	Stress index
Baseline	1.0X	1.0X	1.0X
EMC1	1X	1.3X	1.3X
EMC2	1.2X	2X	2.4X
EMC3	0.8X	0.8X	0.64X
EMC4	0.7X	1X	0.7X
EMC5	2X	0.4X	0.8X
EMC6	1X	1.5X	1.5X



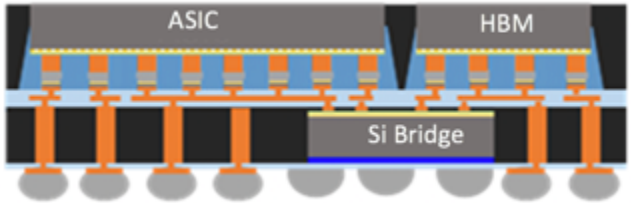
FOCoS-B Fanout module warpage vs different temperatures

FOCoS-B Warpage Control at Fanout Module

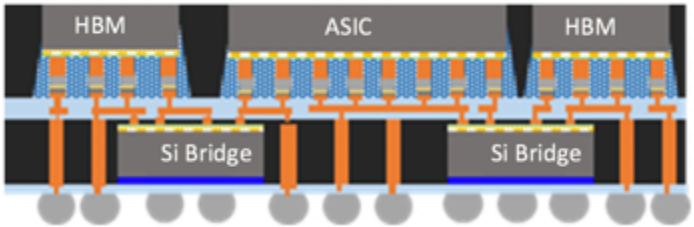
- **Warpage at fanout module level for TV1 & TV2**
  - *Warpage at the fanout module level were similar for TV1 and TV2*
  - *TV2 had slightly higher warpage than TV1*
  - *Both TV1 and TV2 warpage were within the spec.*



Warpage of FOCoS-B TV1 and TV2 at fanout module level vs different temperatures



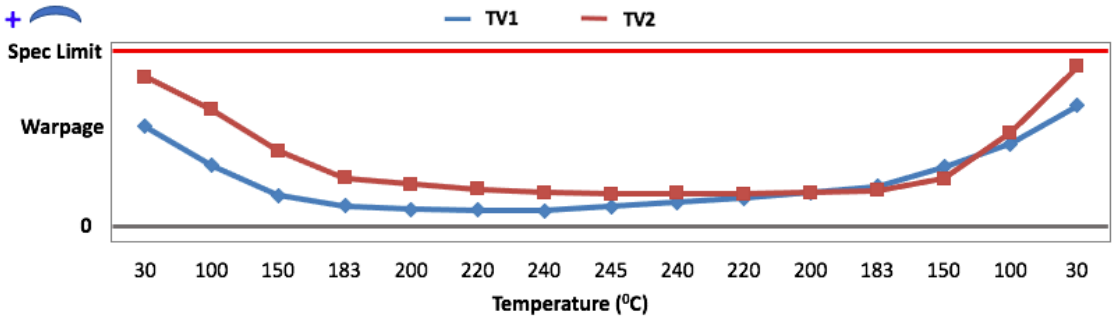
FOCoS-B TV1 fanout module



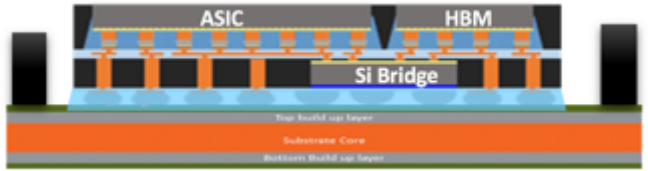
FOCoS-B TV2 fanout module

FOCoS-B Warpage Control at Package Level

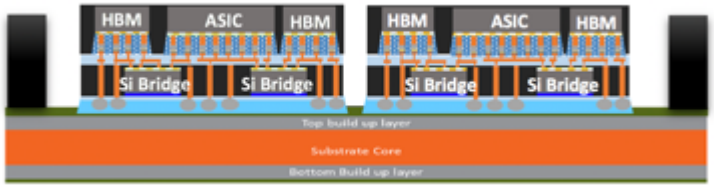
- **Warpage at package level for TV1 & TV2**
  - *TV2 showed larger w*arpage at package level than TV1 due to large package size (78x70mm^2)
  - *Both TV1 and TV2 warpage were within the spec.*



Warpage of FOCoS-B TV1 and TV2 at package level vs different temperatures



FOCoS-B TV1 package

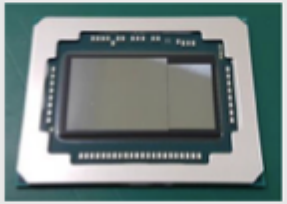
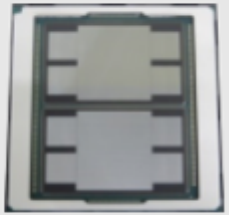


FOCoS-B TV2 package

Reliability of FOCoS-B for Chiplets Integration

➢ Reliability Test

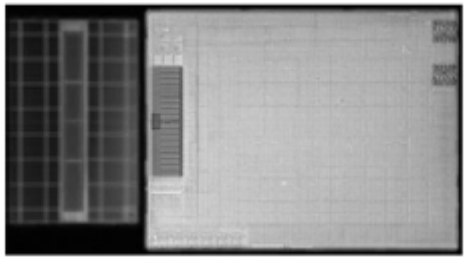
- *Both TV1 & TV2 had passed package level reliability tests*

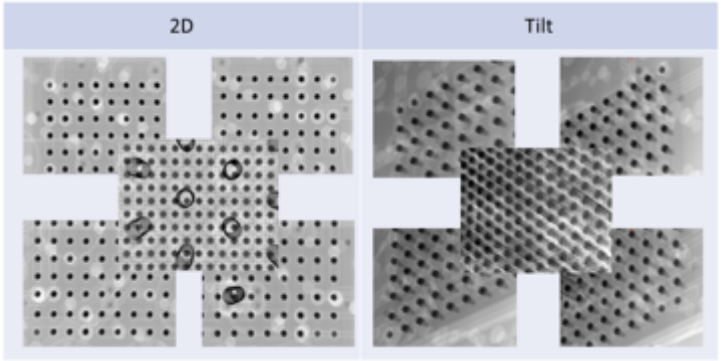
	FOCoS-B TV1	FOCoS-B TV2
Conditions		
MSL4	MSL4	MSL4
TCG (-40°C~125°C)	1200 cycles	1200 cycles
uHAST (130°C/85%RH)	264 hrs	264 hrs
HTST (150°C)	1000 hrs	1000 hrs
Test	O/S + FT+ SAT Pass	O/S + SAT Pass

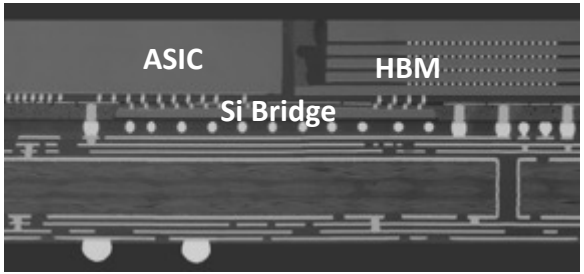
FOCoS-B for Chiplets Integration

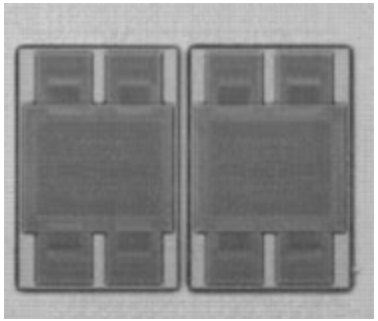
➢ Reliability validation

- *No abnormalities were observed for TV1 and TV2 after reliability tests*
- *Good integrity of FOCoS-B for chiplets integration achieved successfully*

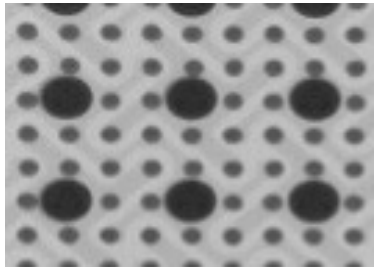




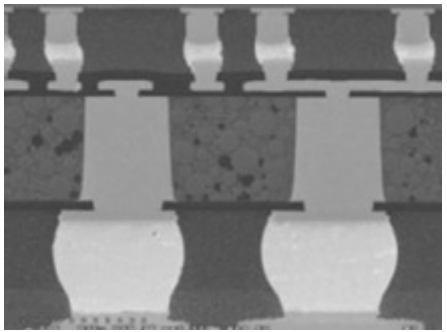




SAM images of TV1 & TV2 after reliability tests



Real time X-ray images of TV1 & TV2 after reliability tests



X-section of FOCoS-B

Summary

- **Chiplets heterogeneous integration optimizes the system performance to continue scaling Moore's law with cost advantage**

- **FOCoS embedded Si bridge technology for chiplets integration have been developed successfully**
  - Enable high density and short reach connections between chiplets through Si bridge that has much finer L/S less than 1/1um for interconnection.
  - Successfully demonstrated FOCoS-B unique advantages including better scalability, high density interconnection; more design flexibility, good thermal stress control and better reliability performance

- **Material selections play critical roles for heterogeneous integration**
  - Compatibilities among various packaging materials (EMC, UF, PI etc..) with Si wafer and substrate
  - Design and material selections enhance yield and performance improvement

Thank You

www.aseglobal.com