From Technologies to Markets

Market & Technology Trends for the Fan-out and 2.5D/3D Packaging Technology

18TH INTERNATIONAL CONFERENCE & EXHIBITION ON DEVICE PACKAGING

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YOLE Développement

NEW TRENDS & DRIVERS: OPPORTUNITY FOR SEMICONDUCTOR PACKAGING

5G

AI/ML

AD/ADAS

Mobile

AR/VR/MR

Data centres

Voice processing

Vehicle electrification

HPC

Cloud computing

IoT/IIoT

Edge computing

Blockchain / cryptocurrency

System requirement

- More computing power
- High speed
- More bandwidth
- Low latency
- Low power
- More functionality
- System integration
- More sensors
- More memory
- Low cost
- Hardware-software compatibility

Opportunity for various devices

Megatrends create business for variety of ICs from high end xPUs to low end discretes

- CPUs, GPUs, SoCs, APUs, FPGAs
- ASICS, DSPs, MCUs
- MEMS/Sensors
- Power ICs/discretes
- Memories
- Optoelectronics

Opportunity for fab/front end

Front end scaling slowdown but continues: Moore's Law keep going but at smaller pace => high end fab business keep growing (5nm & below)

More & more heterogeneous integration to support functionality, faster time to market and low cost : More than Moore's => Resurgence of legacy fabs => Increasing business

8" wafer fabs and related tools demand to remain strong

Require new technology / innovations: Front end design / manufacturing innovations: from von Neuman to neuromorphic computing architecture; new processes: beyond FinFet, nanowires FET, vertical NAND etc; require EUV and new deposition/etching technologies; new interconnect materials, dielectrics etc.

Opportunity for semiconductor packaging

Create business opportunity for both advanced and traditional packaging platforms

Advanced packaging (WLPs, flip-chip, TSV) business opportunity supported by AI/ML, Mobile, AR/VR, 5G, smart automotive

Traditional packaging (wire-bond lead frame based) business opportunity created by IoTs, Industry 4.0, smart automotive

Mega trends like mobile, automotive, IoTs, industry 4.0, require variety of MEMS sensors that create opportunity for both traditional & advanced packaging

Require Back end and assembly innovations: panel level packaging, high accuracy bonders, TCB, CtW/WtW bonding, photonics integration in package. As for materials, there is a desire to develop new dielectric materials, mold compounds, underfill, solder interconnects, and TIMs for fulfilling the stringent performance and reliability requirements demanded by next-generation hardware.

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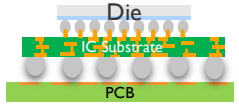
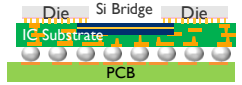
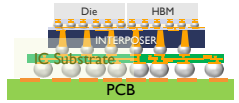
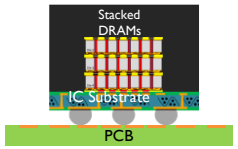
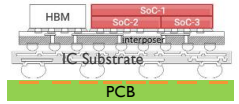
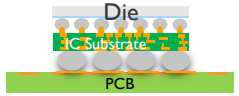
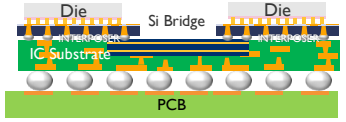
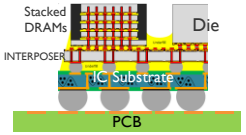
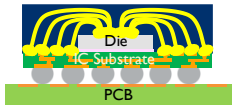
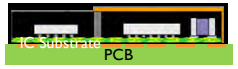
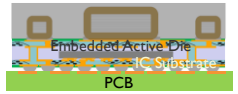
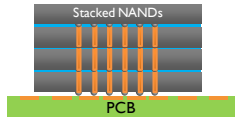
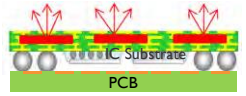
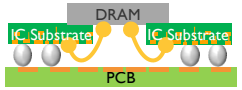
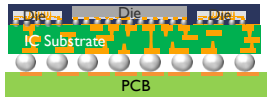
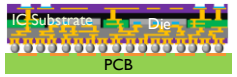
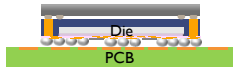
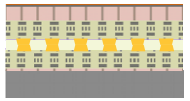
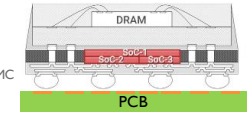
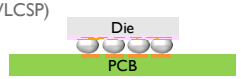
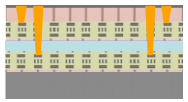
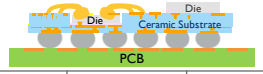
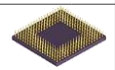
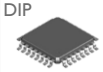
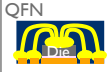
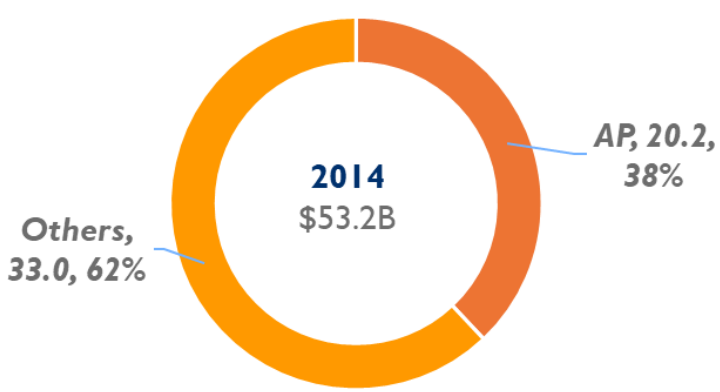
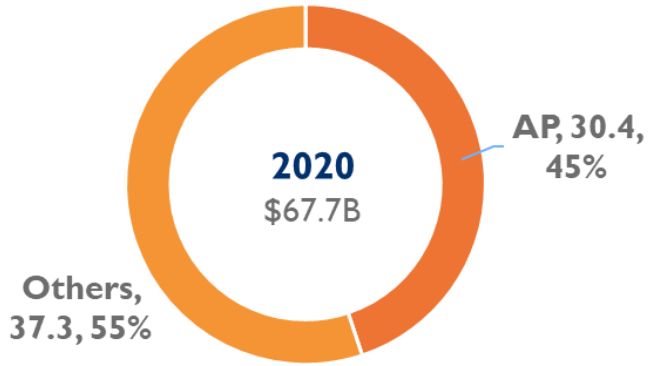
PACKAGING TECHNOLOGIES OVERVIEW

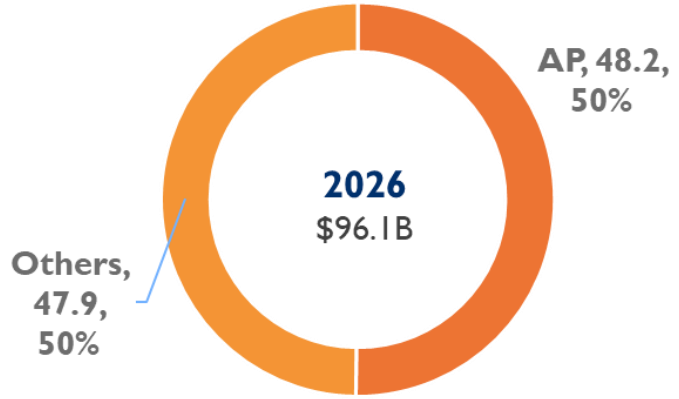
ARCHITECTURE	WIRE BOND	FLIPPED DIE	EMBEDDED DIE	2.5D	3D	EMERGING
	Traditional Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging	Advanced Packaging
SUBSTRATE TYPES: IC Substrate (Organic)		FC BGA 	Embedded Si Bridge 	Si Interposers 	3DS TSV 	Hybrid Bonding - SoC on interposer  SOURCE: TSMC
		FC CSP 	Embedded Si Bridge + Si Interposers 		HBM TSV 	
	WB CSP WB BGA 	FC SiP Metal Shielding 	Embedded Die / Passives 		NAND TSV 	Embedded Multi-Die / Passives  SOURCE: JCET
	BOC 	Fan-Out on Substrate 	FOPLP 			
No Substrate	COB 	Fan-Out PoP 			Cu-Cu Hybrid Bonding – WoW 	Hybrid Bonding - SoC in Fan-Out  SOURCE: TSMC
		Fan-Out 				
		Fan-In (WLCSP) 			TSV, after bonding – WoW 	
Ceramic Substrate	LTCC HTCC 	CPGA 				
Lead frame Substrate	DIP  SOT/TSOP  QFN  QFP, LCC etc.	FC QFN 				

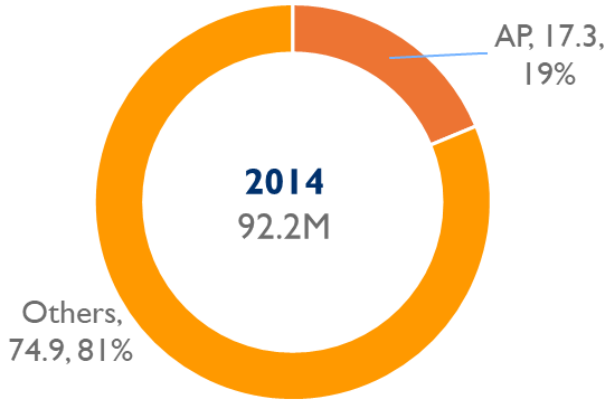
ADVANCED PACKAGING OVERVIEW 2014 to 2026

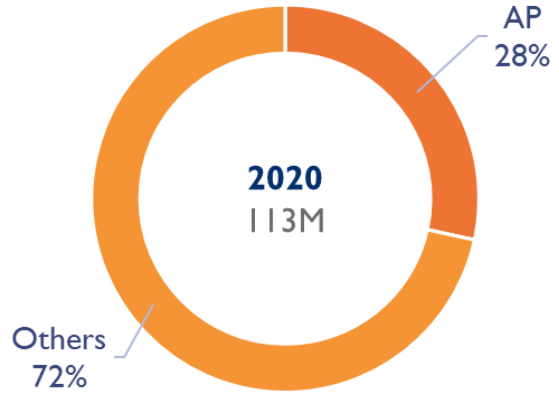
Revenue Split ($B) and wafer starts (300mm eq.) split

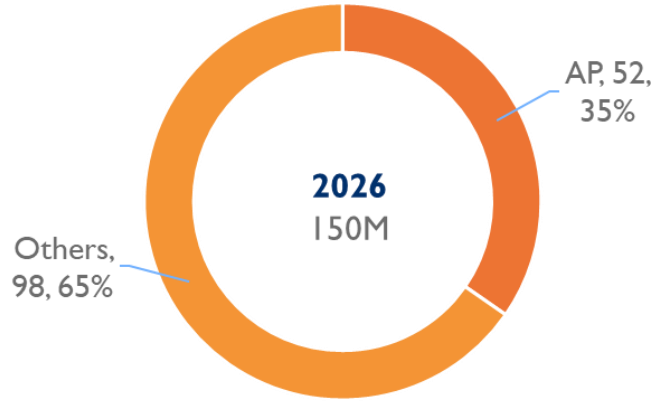






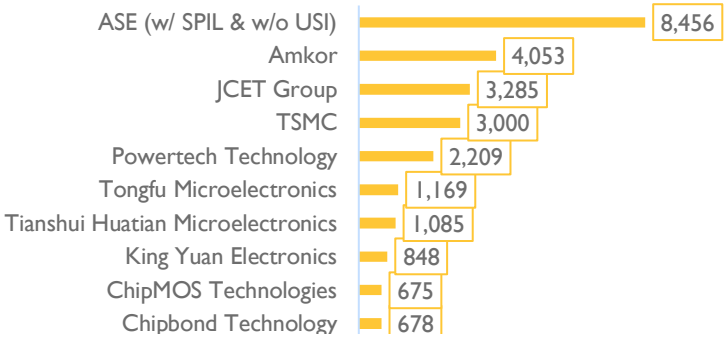




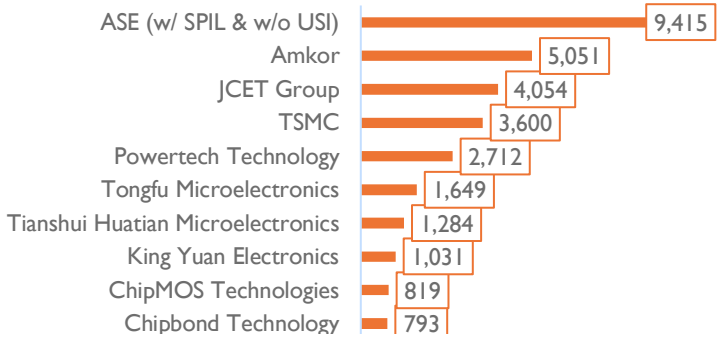


A RECORD YEAR FOR PACKAGING PLAYERS (PACKAGING REVENUE)

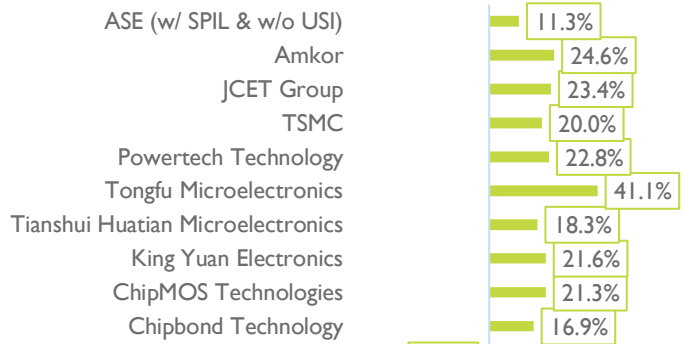
Top Packaging Players Ranking by 2019 Revenue [$M]



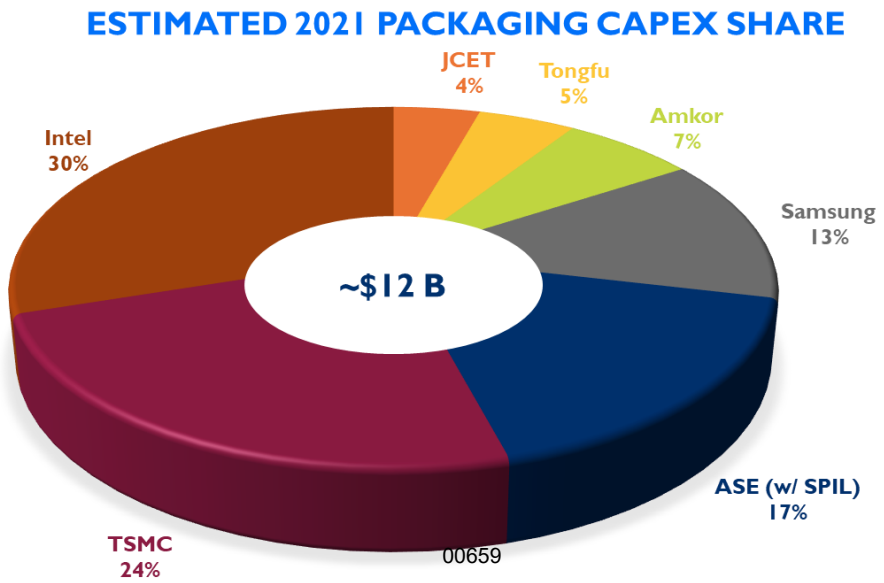
Top Packaging Players Ranking by 2020 Revenue [$M]



YoY Growth [%]



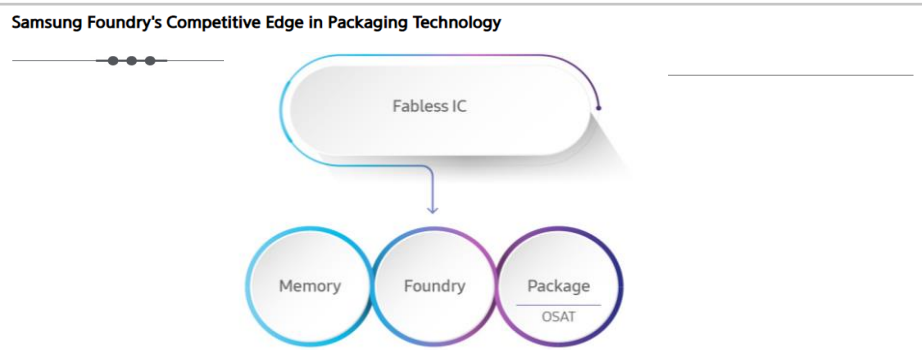
15-20% increase in 2020 revenue compared to 2019, and 2021 is expected to shape up as a "Banner Year" for Packaging Players



ADVANCED PACKAGING IS NOW AN ESSENTIAL TECHNOLOGY

Big players are committing extensively to 3D/2.5D Packaging

At Intel's Architecture Day 2020, **Intel** introduced "**Process and Packaging**" as one of the 6 Technology Pillars

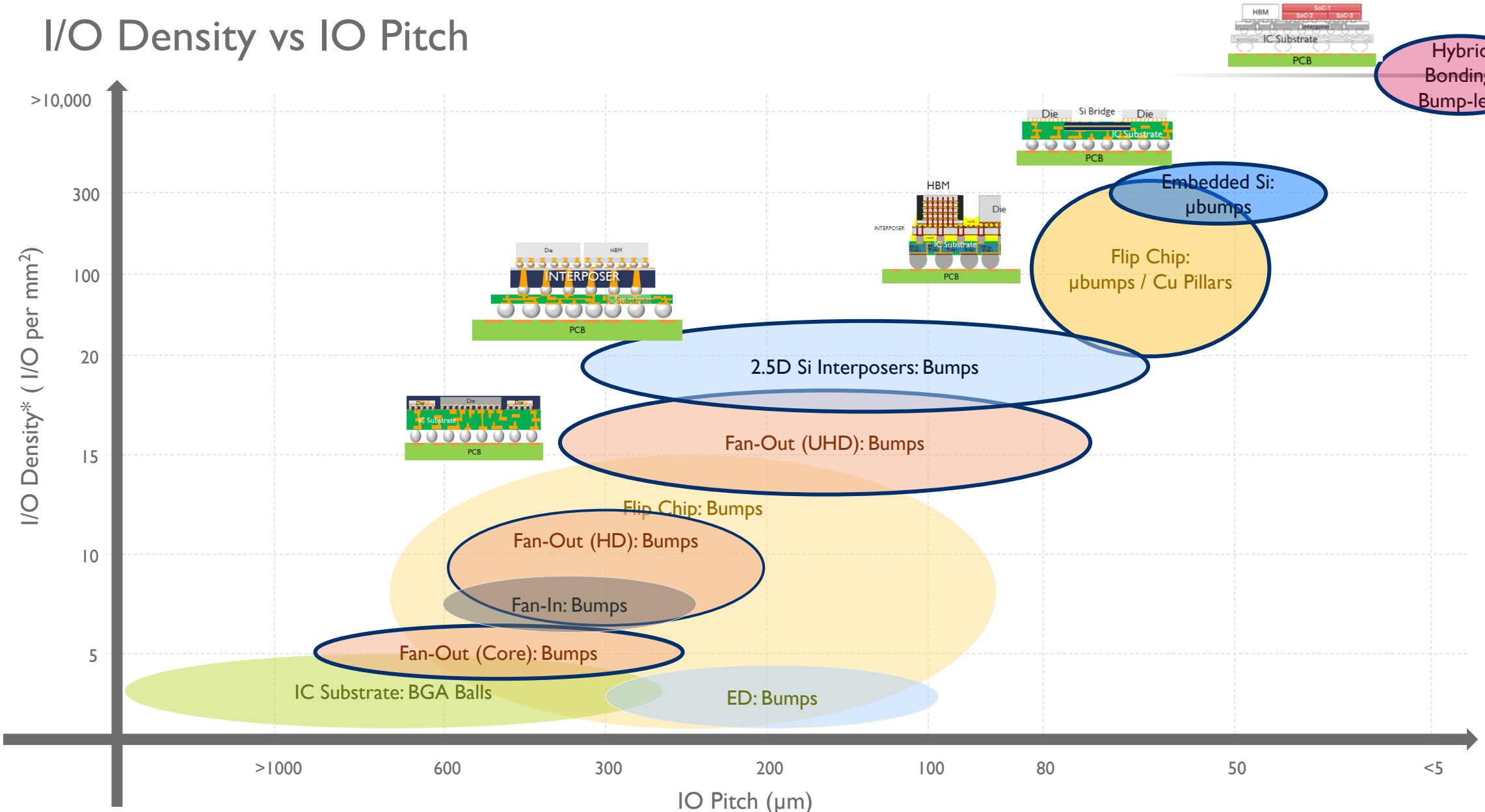


Samsung Foundry is positioning packaging as a **one-stop total solution**; covering design, memory, logic and package.

In 2020, **TSMC** announced a new 3D/2.5D Packaging family called **3DFabric™**, ready to capture high-end performance computing business

ADVANCED PACKAGING TECHNOLOGY ROADMAP

I/O Density vs IO Pitch



*I/O Density refers to total number of IOs per package platform area
Roadmap is based on industry average

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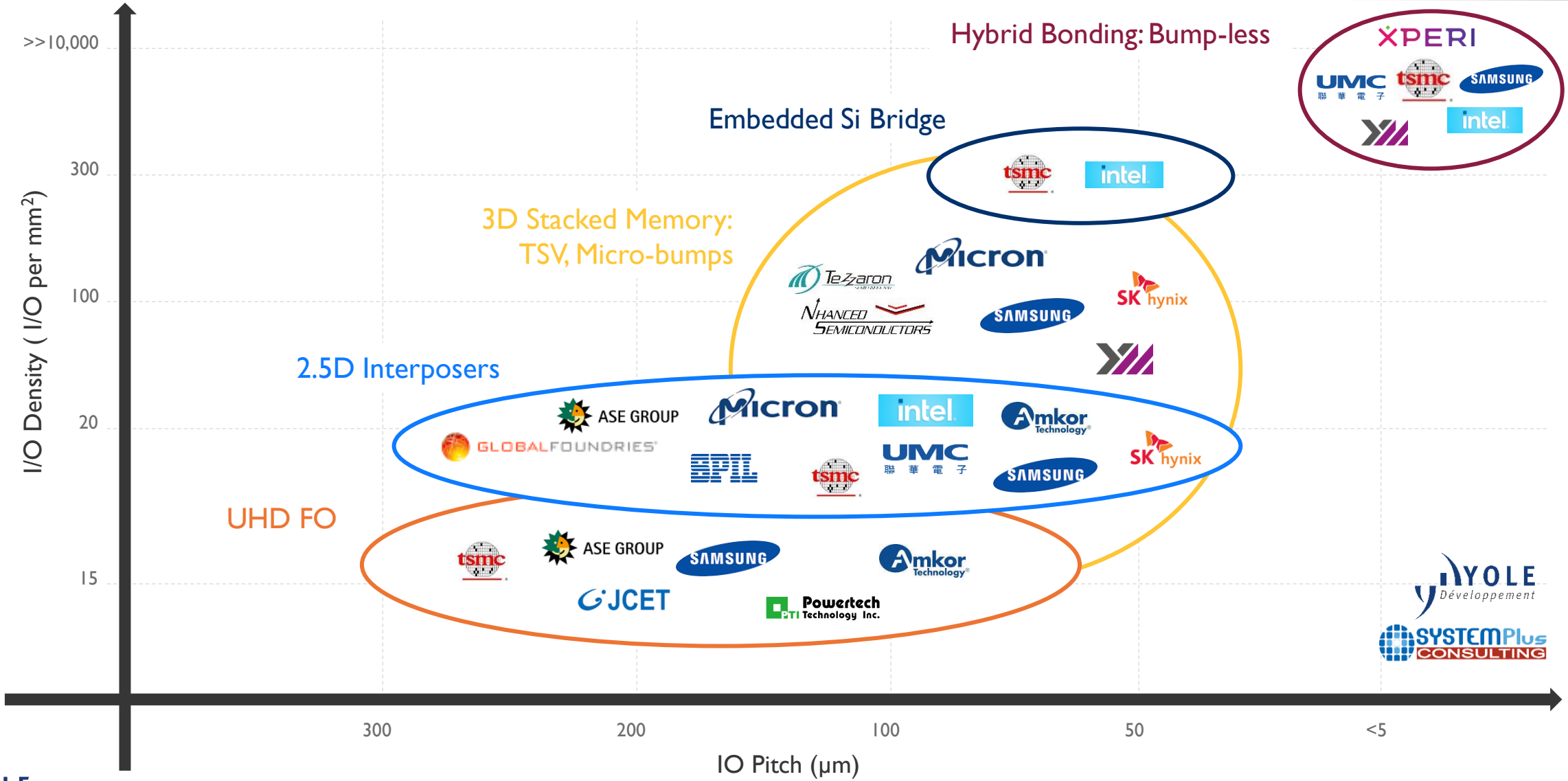
HIGH-END PACKAGING: SUPPLY CHAIN

Mapping of Players based on Technology



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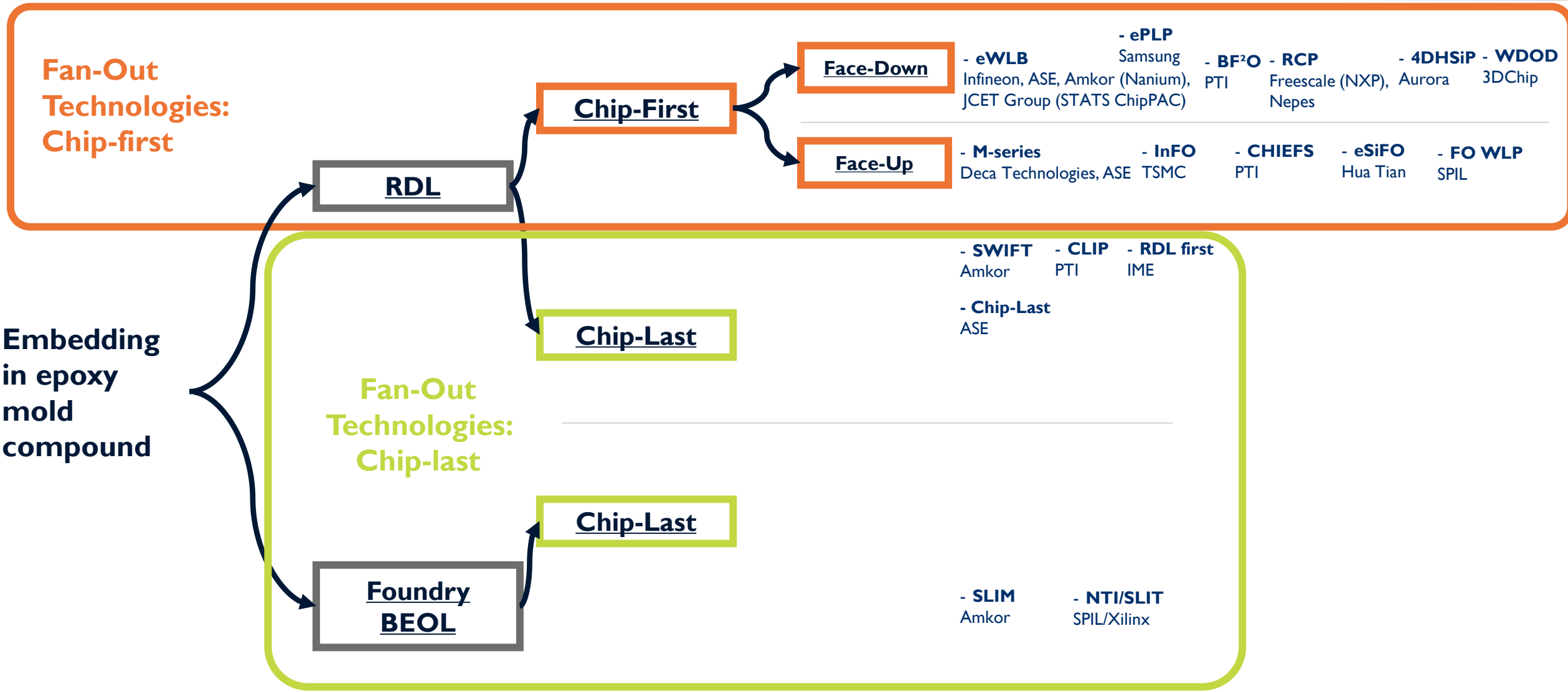
Non-exhaustive List of Players

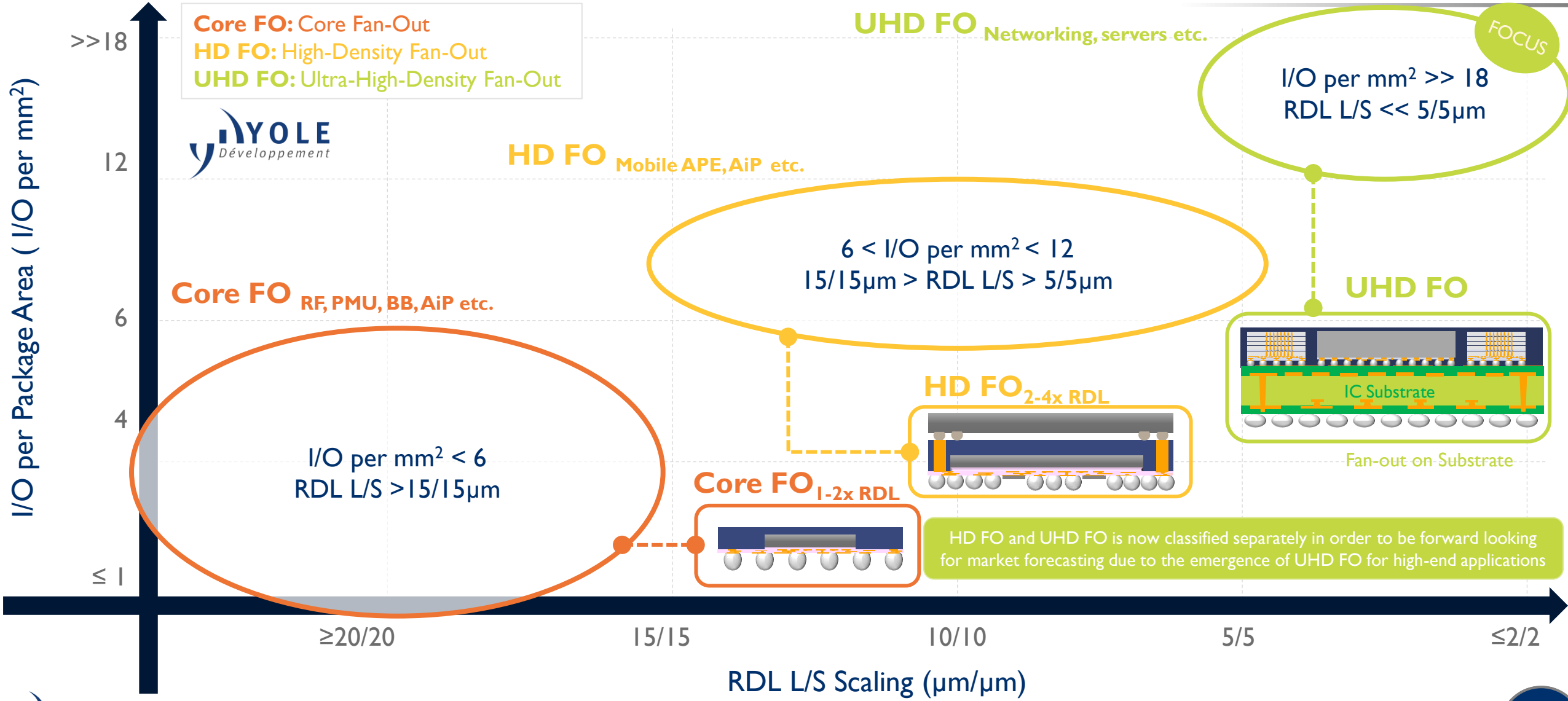
FAN-OUT PACKAGING SEGMENTATION: TECHNOLOGY & PLAYERS



*Non-exhaustive list of technologies

FAN-OUT PACKAGING DEFINITION BY MARKET CLASS

Core FO vs HD FO vs UHD FO



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FAN-OUT PACKAGING SEGMENTATION: MARKET

Manufacturers' Status in 2020 Fan-Out Packaging Landscape

Production

Development

Core FO: Core Fan-Out
HD FO: High-Density Fan-Out
UHD FO: Ultra-High-Density Fan-Out

UHD FO Networking, servers etc.

HD FO Mobile APE, AiP etc.

Core FO RF, PMU, BB, AiP etc.

Core FO 1-2x RDL

HD FO 2-4x RDL

UHD FO

Fan-Out on Substrate

I/O per Package Area (I/O per mm²)

>>18

12

6

4

≤ 1

≥20/20

15/15

10/10

5/5

≤2/2

RDL L/S Scaling (µm/µm)

FAN-OUT PACKAGING MARKET DRIVERS ROADMAP

HPCs

APE

5G*

Radar

RF
Audio Codec
PMIC

Servers

Network Switches

APE
Apple iPhone 7

APE
Apple iPhone 8

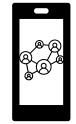
APE
Apple iPhone XS

APE
Apple iPhone 11

APE
Apple iPhone 12

APE | AiP (5G)
Advanced Smartphones

APE | AiP (5G)
Advanced Smartphones



APE & PMIC
Samsung Galaxy Watch

APE
Apple Series 4

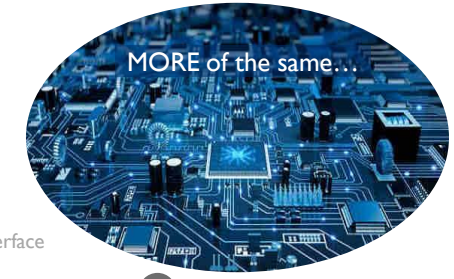
Audio & PMIC
China Mobile Coolpad

PMIC
Onda Aurora 4G

Audio C. & PMIC
Essential 360 Camera

Audio C. & PMIC
Oppo F7

Connectivity: MCU & BT
Fitbit (Google) Charge 3



Basebands
LGE LG325G

RF
Samsung Galaxy S II

Audio Codec
Xiaomi Redmi Note 3

Audio C. & PMIC
Blackberry KEYone

Connectivity
Google Clip

Audio C. & PMIC
AKG Headphones (Samsung)
ARM-based USB-C audio interface

≤2016

2018

2020

2022*

2024*

≥2026*

* From 2021 onwards, market drivers are hypothesized based current trends and interviews with industry players.

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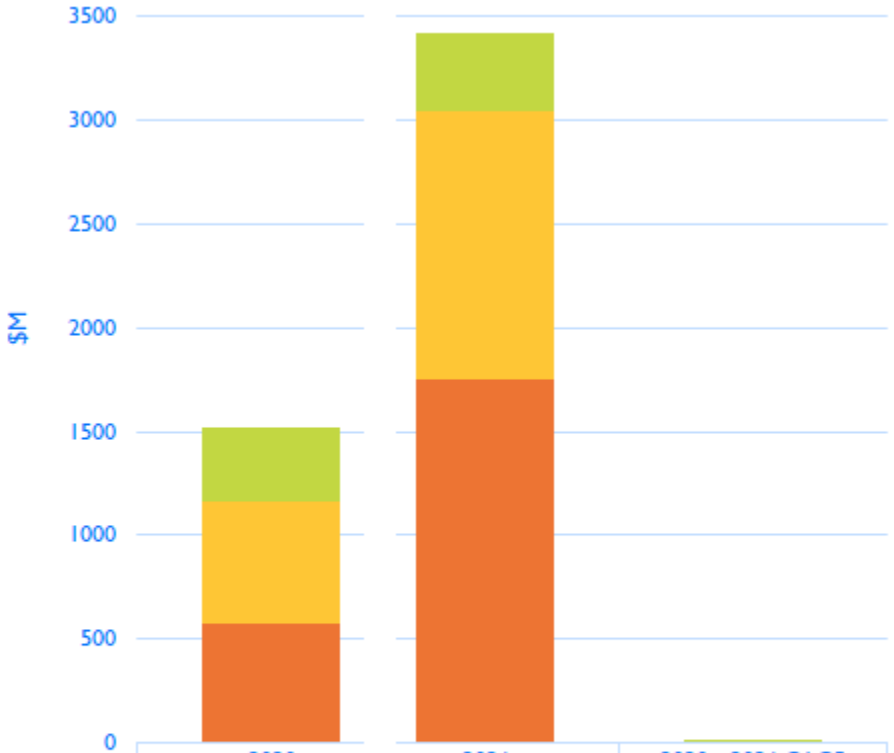
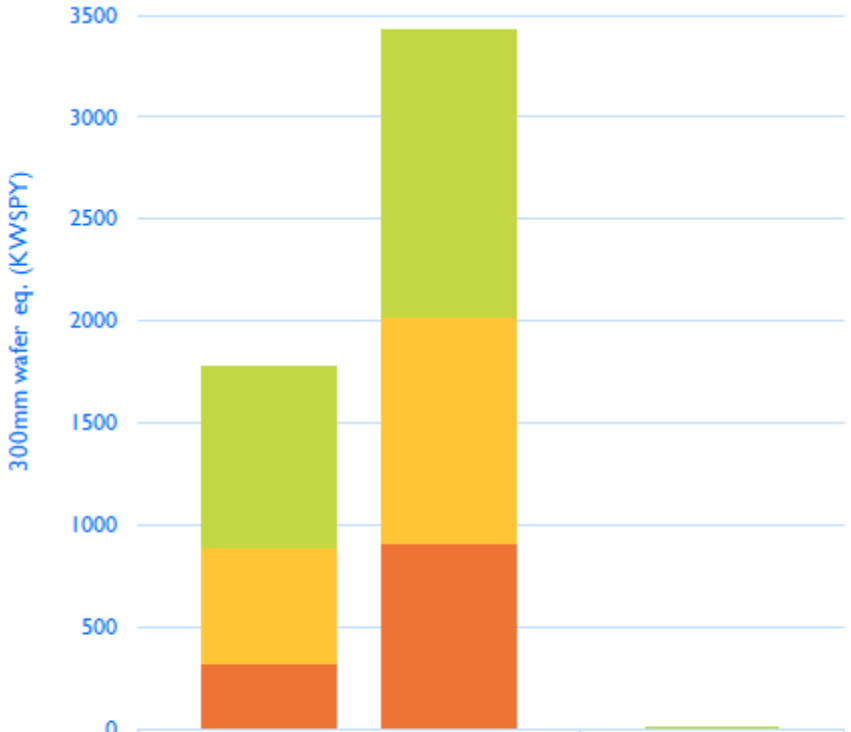
FO PACKAGE MARKET DYNAMICS: UHD, HD, AND CORE FAN-OUT



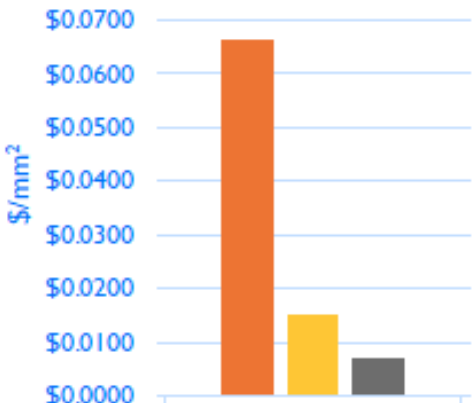
	2020	2026	2020 - 2026 CAGR
Core FO	358	380	1%
HD FO	588	1295	14%
UHD FO	576	1750	20%
Total	1522	3425	14%

Revenue ($B)



	2020	2026	CAGR (2020-2026)
Core FO	888	1422	8.2%
HD FO	573	1109	11.6%
UHD FO	315	904	19.2%
Total	1776	3435	11.6%

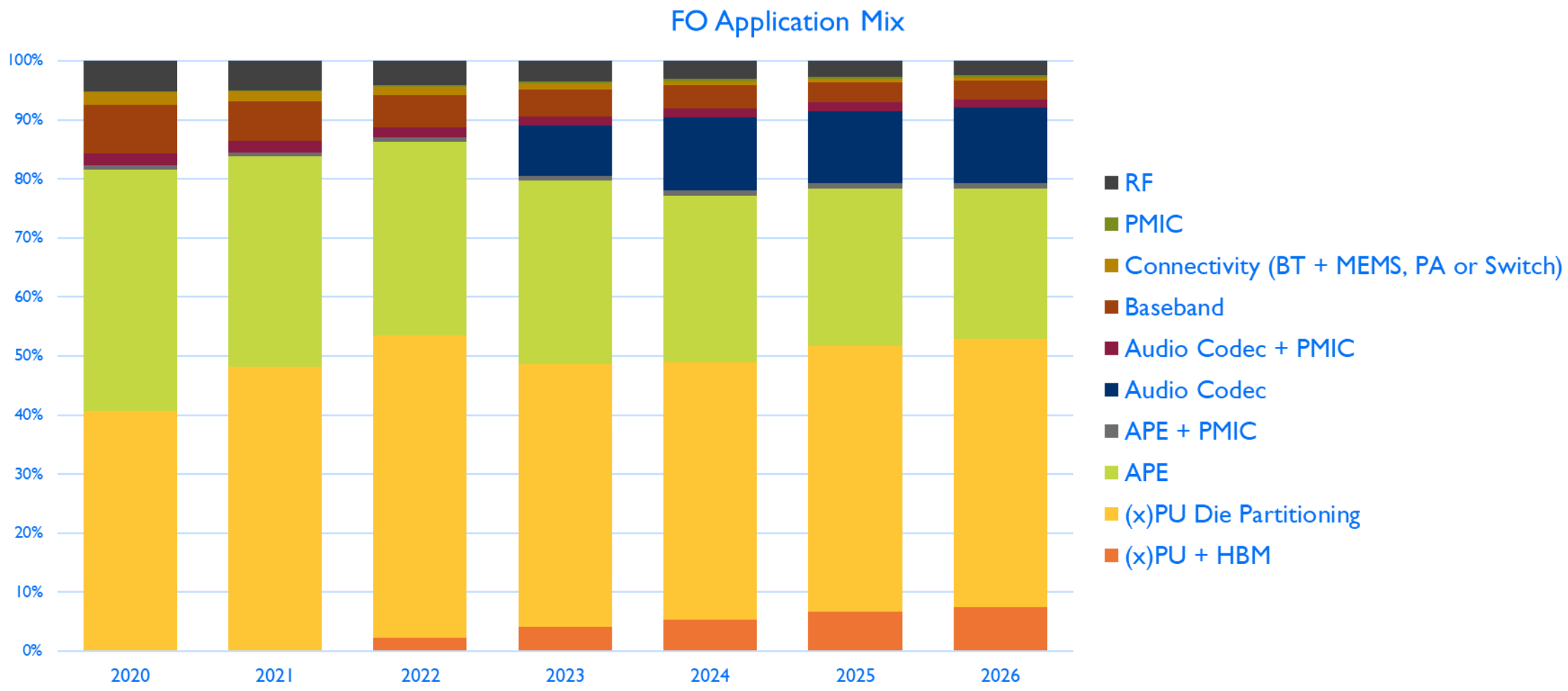
Wafer (KWSPY, 300mm eq.)



	2021
UHD FO	$0.0665
HD FO	$0.0152
Core FO	$0.0070

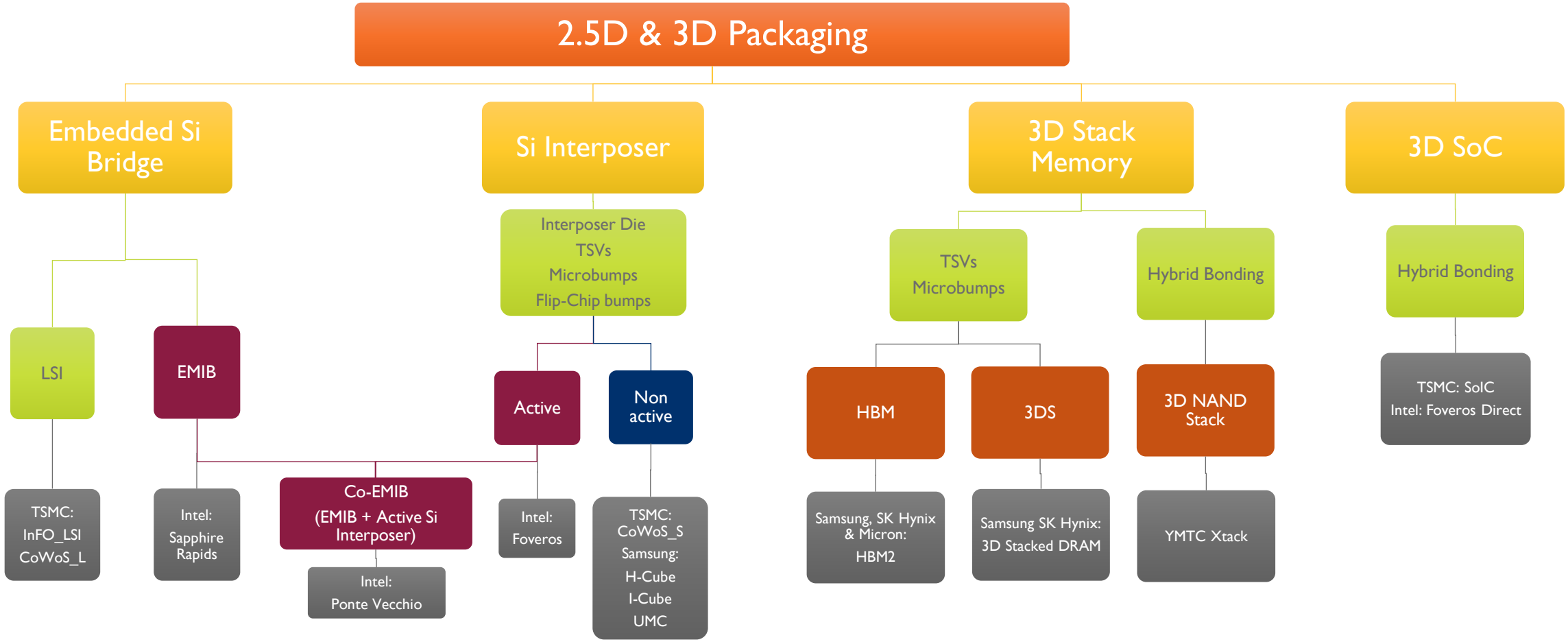
Avg. ASP per package area ($/mm2)

FO PACKAGE APPLICATION MIX



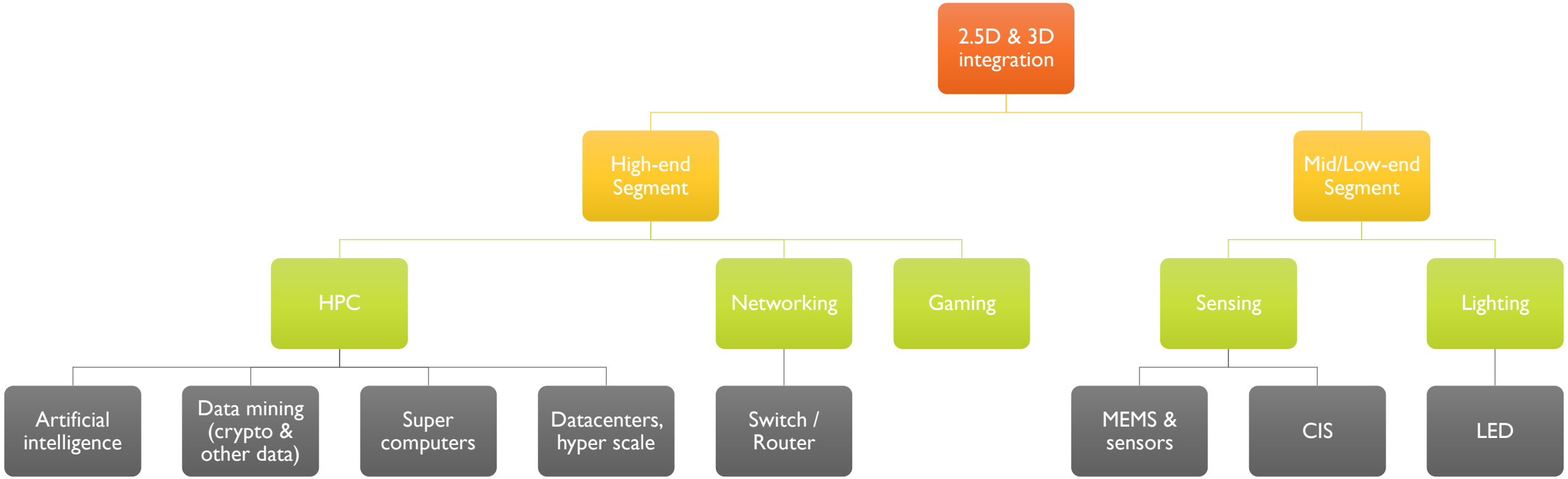
2.5D/3D

HIGH-END PERFORMANCE PACKAGING – ALL PLATFORMS



HIGH-END PERFORMANCE PACKAGING – MARKET SEGMENTATION

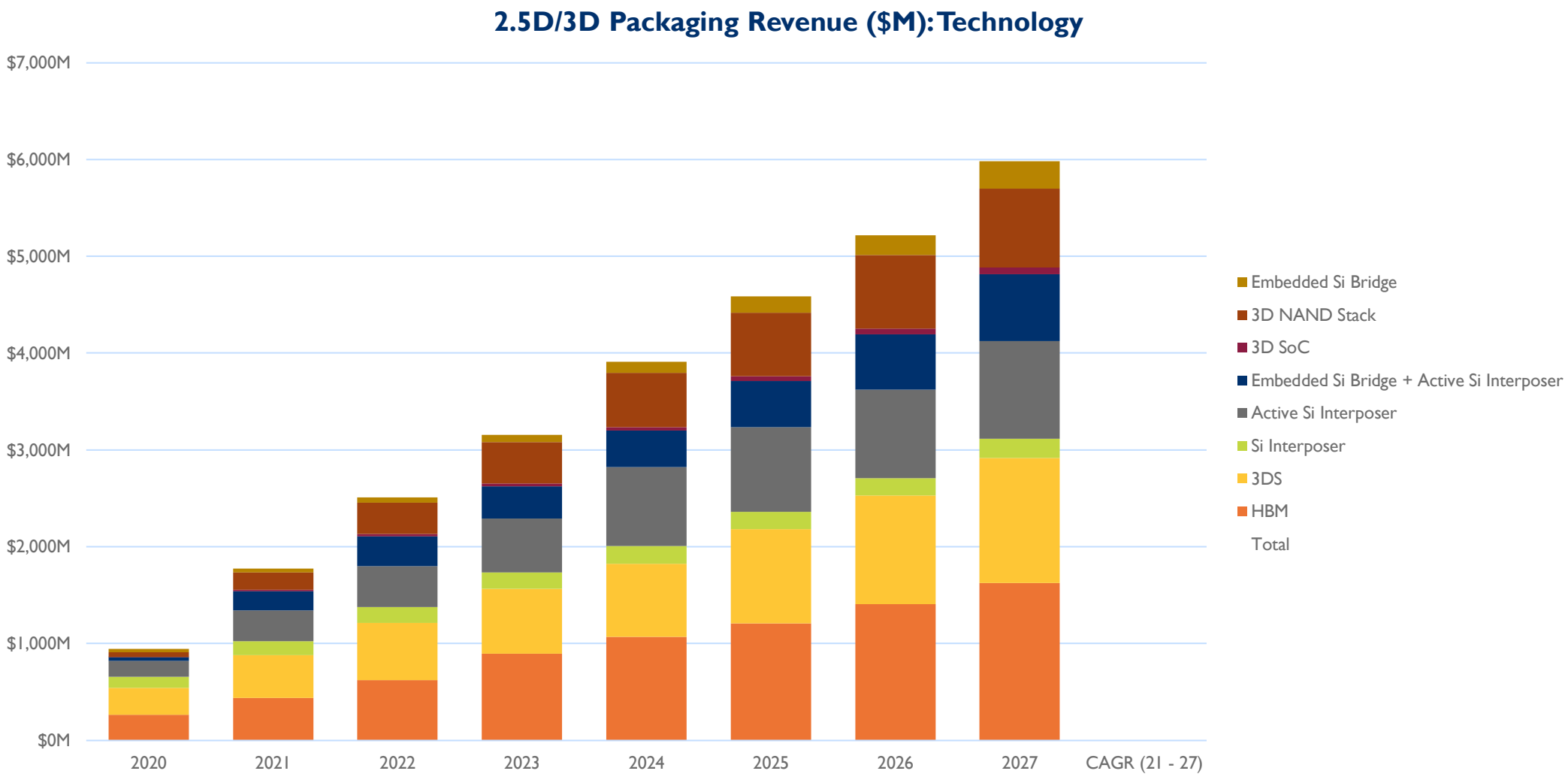
The market is divided into high-end & mid- / low-end segments



High-end segment is defined as the market where an application is less sensitive to the cost, but requires smaller footprint in addition to high performance & reliability

Mid-/low-end segment is defined by a good balance between cost sensitivity & performance

2.5D/3D PACKAGING REVENUE- SPLIT BY TECHNOLOGY

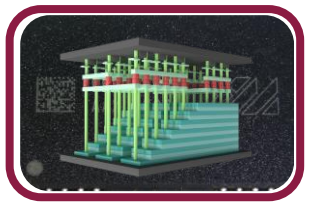


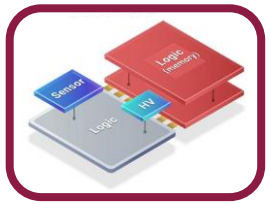
2.5D/3D PACKAGING ROADMAP: APPLICATION-TECHNOLOGY

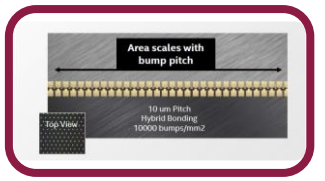
TIMELINE — ≤2019 — 2020* — 2021 — 2022 — 2023 — 2024 — 2025

I/O DENSITY

YMTC Periphery + Array
X-Stacking

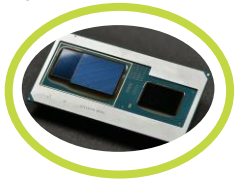






HPC (x)PU in Servers
TSMC & Intel – 3D SoC

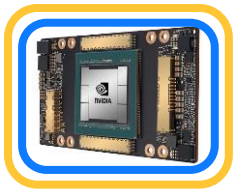
Intel HBM+GPU
Kaby Lake-G

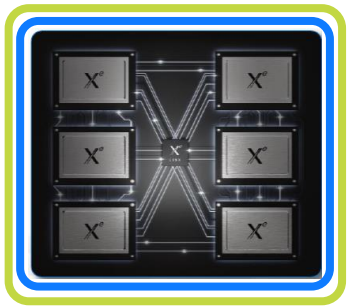


Intel FPGA
Stratix 10

Intel FPGA + Chiplets
Agilex

NVidia GPU Interposer HBM2E
A100





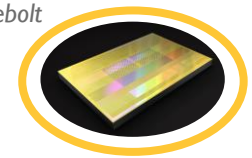
Intel Exascale GPU - HPC
Ponte Vecchio: Co-EMIB

Stacked DRAM
3DS

Google (x)PU
TPU V3

Samsung HBM2E
Flashbolt

Samsung HBM
Flarebolt



Intel CPU + Active Interposer
Intel Lakefield Foveros Core i5-L16G7

Xilinx FPGA
Virtex UltraScale

AMD GPU
Vega Frontier

NVidia GPU
Pascal 100

Broadcom (x)PU + HBM
Jericho2

Intel (x)PU Ethernet Switch
Tofino2

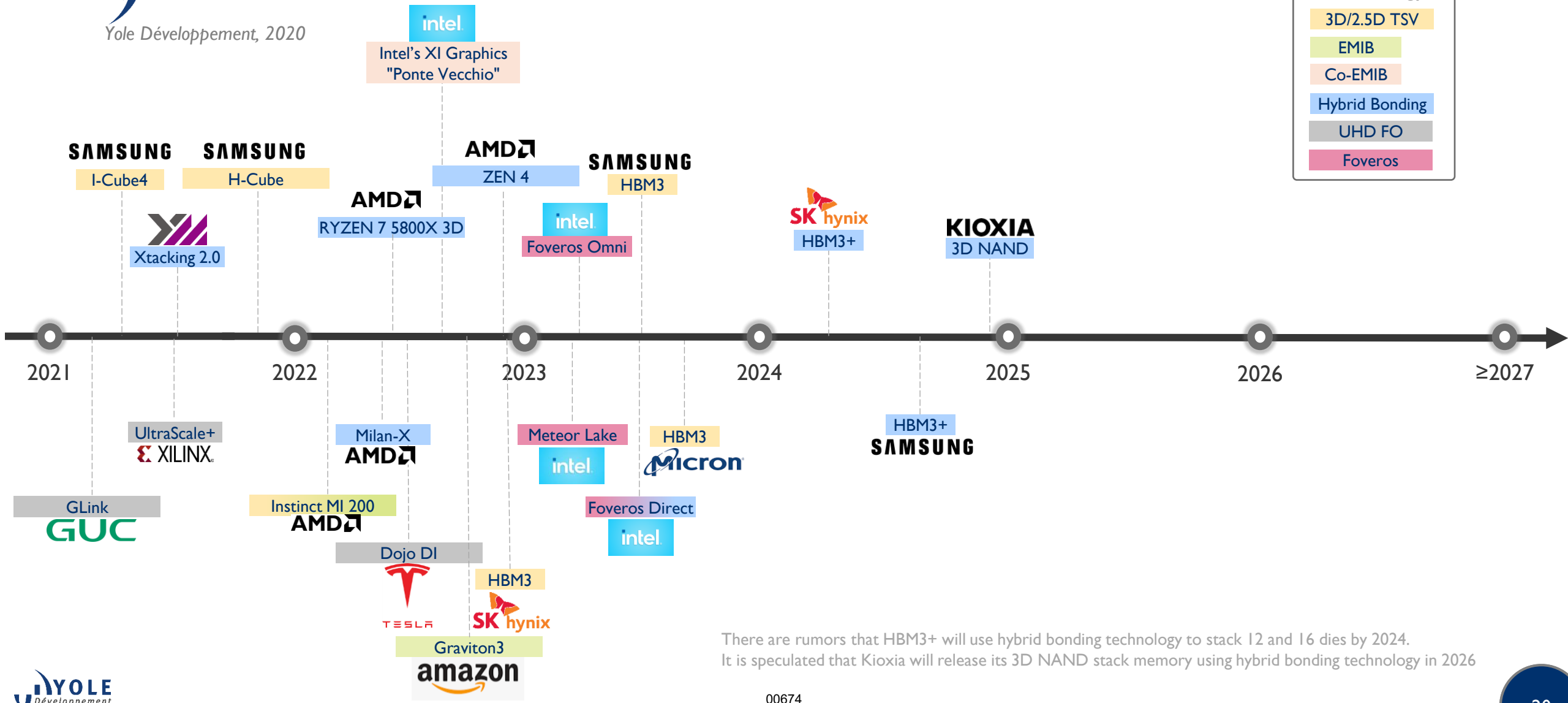
HiSilicon CPU (Storage)
Hi1610 (Now known as Kunpeng)

TYPE OF TECHNOLOGY

- Hybrid Bonding
- Embedded Si bridge
- TSV, Micro-bumps
- 2.5D Interposers

HIGH-END COMMERCIAL PRODUCT LAUNCHES – STACKING TECHNOLOGY

Yole Développement, 2020



There are rumors that HBM3+ will use hybrid bonding technology to stack 12 and 16 dies by 2024.
It is speculated that Kioxia will release its 3D NAND stack memory using hybrid bonding technology in 2026

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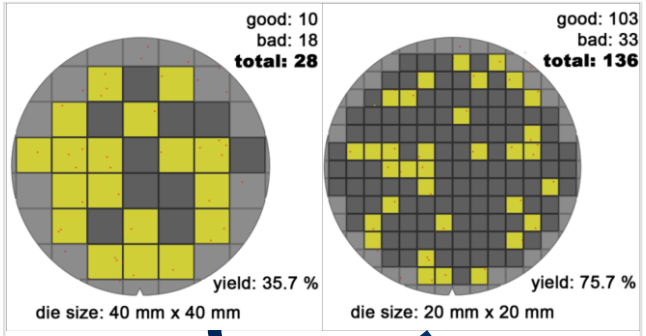
3D SYSTEM ON CHIP (3D SOC)

Advantages of Die Partitioning

Die partitioning consists of splitting a die's functions and redistributing them across two or more dies.

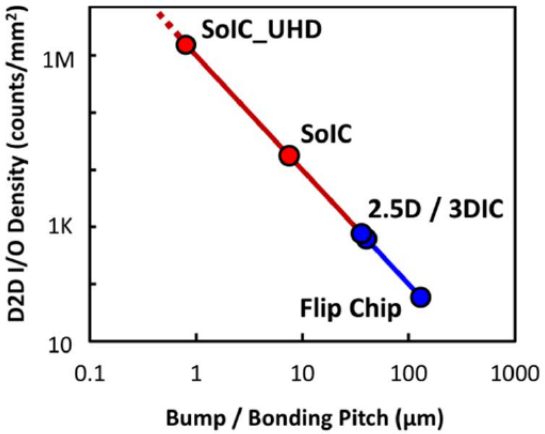


>2X Yield Improvement
>20% Effective Die Quantity Increase

Source: Mediatek

Better Yield (Cost Efficient)

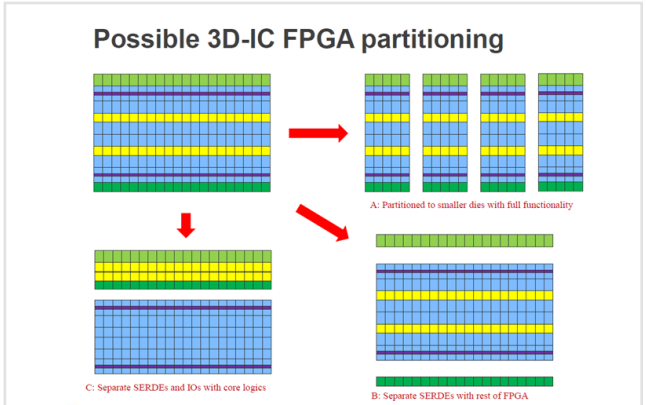
- Footprint reduction enables saving board surface
- Gain yield due to smaller die size



Source: TSMC

Performance

- Better interconnection paths
- Higher IO Density



Source: Xilinx

Smaller Die Footprint

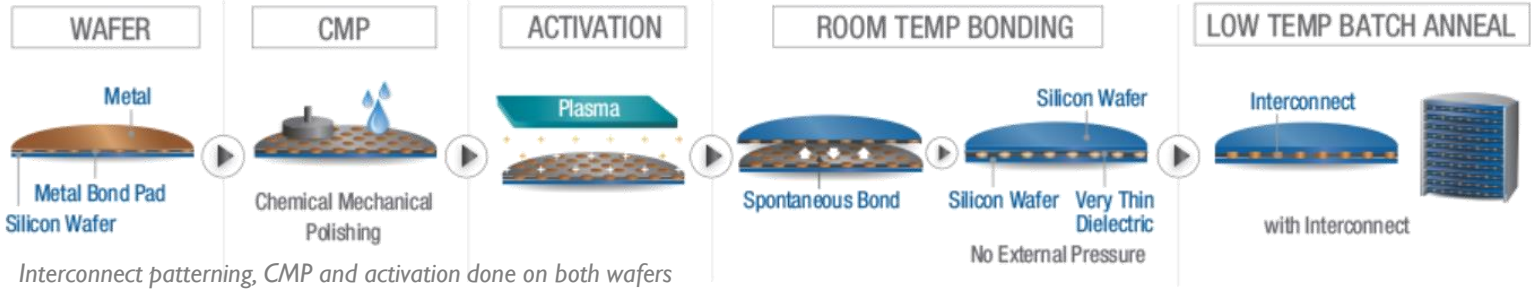
- Solutions to the large die size floor-planning limitation due to lithography reticle size

HYBRID BONDING PROCESS FLOW

Note: Showed is process flow established by XPERI, but other process developments have been also done in parallel, e.g. Leti, Imec, TSMC.

W2W process flow

- Used for CIS, F2F logic, 3D NAND
- IN HVM from 2015/2016
- Specialized CMP tools and W2W bonders are used



Interconnect patterning, CMP and activation done on both wafers

XPERI

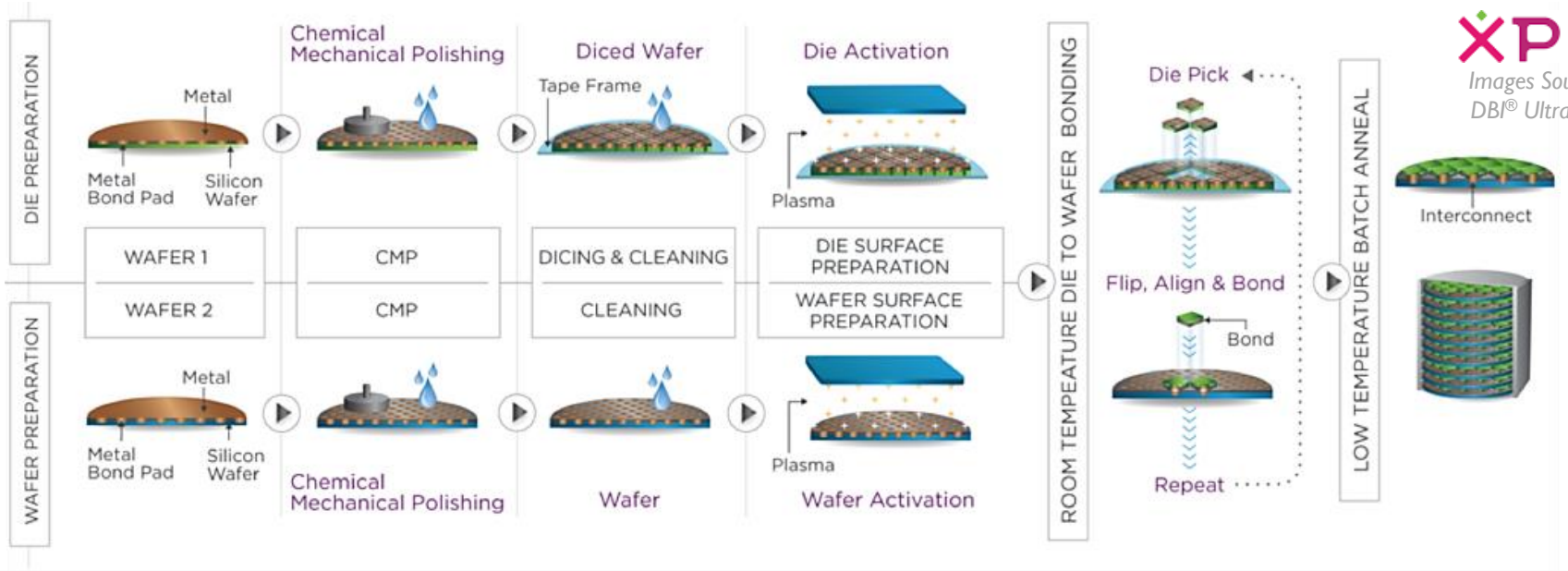
Images Source: Xperi

DBI® process flow

D2W process flow

- Used for heterogenous integration
- LVM expected in 2022
- Specialized CMP tools, singulation tools, and D2W flip chip bonders are used

- Singulated dies from source wafer are cleaned and activated collectively on tape frame (special plasma reactors or atmospheric plasma) are transferred one-by-one to destination wafer



XPERI

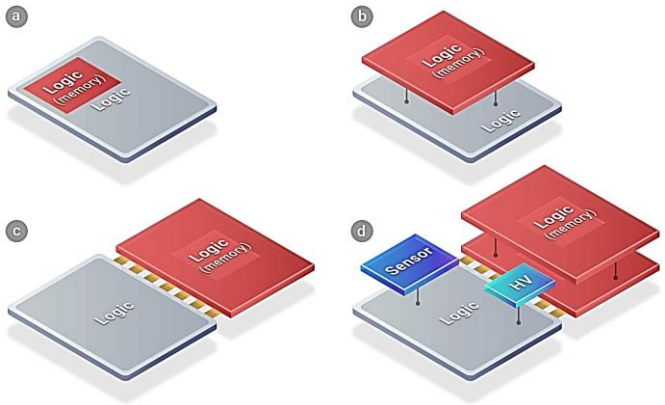
Images Source: Xperi

DBI® Ultra process flow

3D SOC/SOIC PACKAGING (USING HYBRID BONDIND APPROACH)

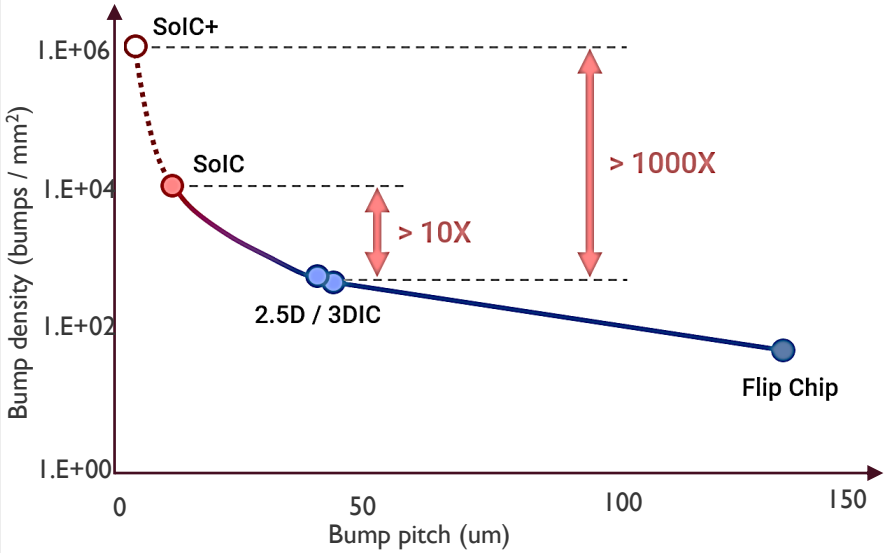
Key features of 3D SoIC technology: Heterogeneous integration, scalability & 3D system integration

Heterogeneous integration of KGDs with different chip sizes, functionalities and wafer node technologies



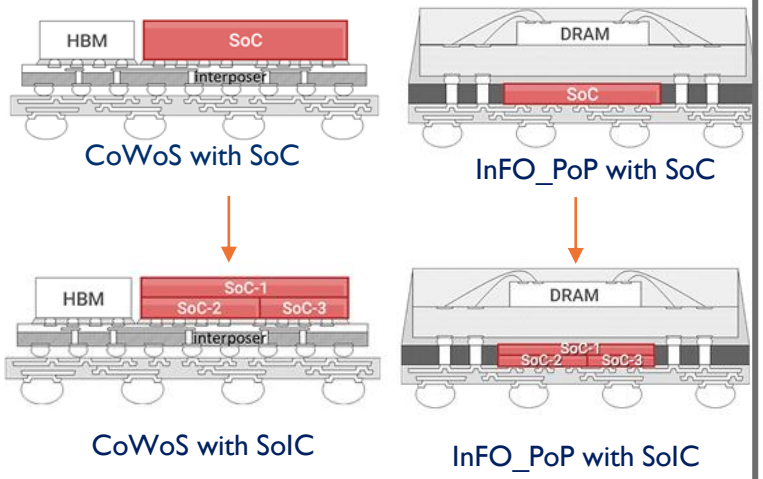
(a) SoC before chip partition; (b), (c), (d) Variant partitioned chiplets and re-integrated schemes enabled by SoIC

Exceptional scalability



With the innovative bonding scheme, SoIC enables strong bonding pitch scalability for chip I/O to realize high-density die-to-die interconnects. The bond pitch starts from sub-10 µm. Short die-to-die connection of SoIC has the merits of smaller form-factor, higher bandwidth, better power integrity (PI), signal integrity (SI), and lower power consumption compared to the current industry state-of-the-art packaging solutions.

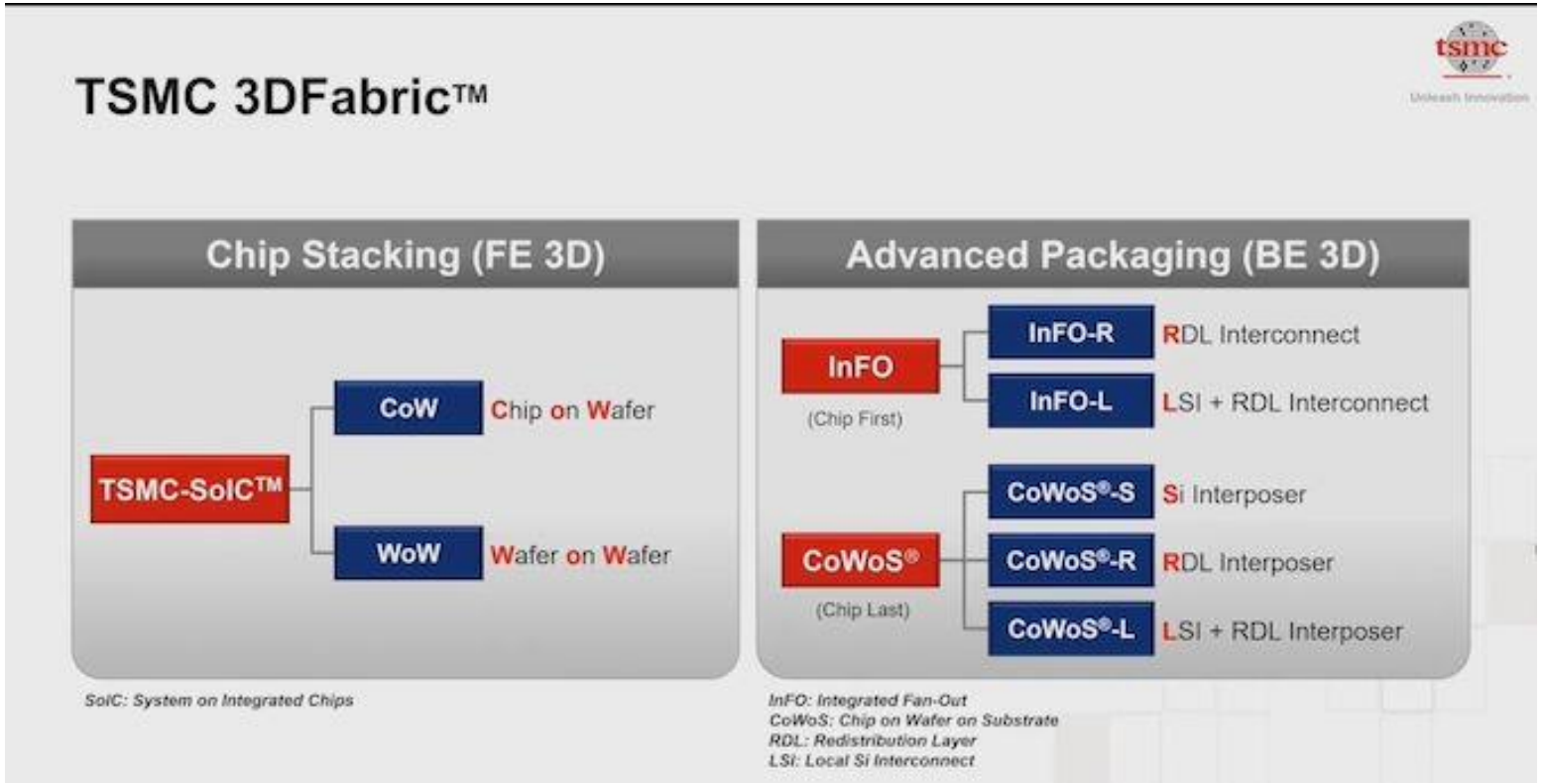
Holistic 3D system integration



SoIC integrates both homogeneous and heterogeneous chiplets into a single SoC-like chip with a smaller footprint and thinner profile, which can be holistically integrated into advanced WLSI (aka CoWoS and InFO). From external appearance, the SoIC is just like a general SoC chip yet embedded with desired and heterogeneously integrated functionalities.

TSMC'S NEW ADVANCED PACKAGING BRANDING

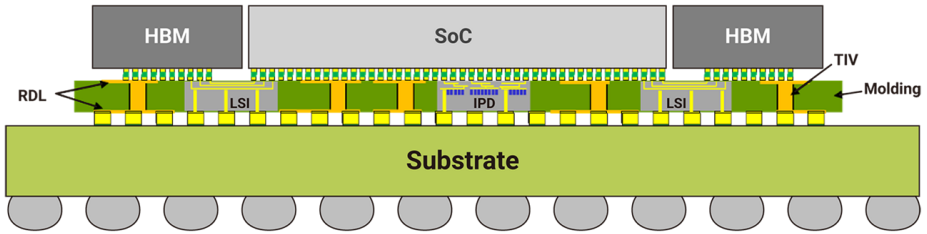
TSMC has introduced 3D Fabric Technology Segmentation in 2020



F2F Technology	3D-IC	SoIC	SoIC_UHD
Structure	µbump	SoIC Bond	SoIC Bond
Bump pitch	36 µm	9 µm	0.9 µm
Bump Density	1.0X	16.0X	1600.0X
Speed*	1.0X	11.9X	11.9X
Bandwidth Density**	1.0X	191.0X	19100.0x
Power Consumption (Energy/bit)	1.0X	0.05X	0.05x

TSMC's InFO integration with an LSI is called InFO-L or InFO-LSI, and follows a similar structure with the new addition of it integrating this new local silicon interconnect intermediary chip for communication between two chips.

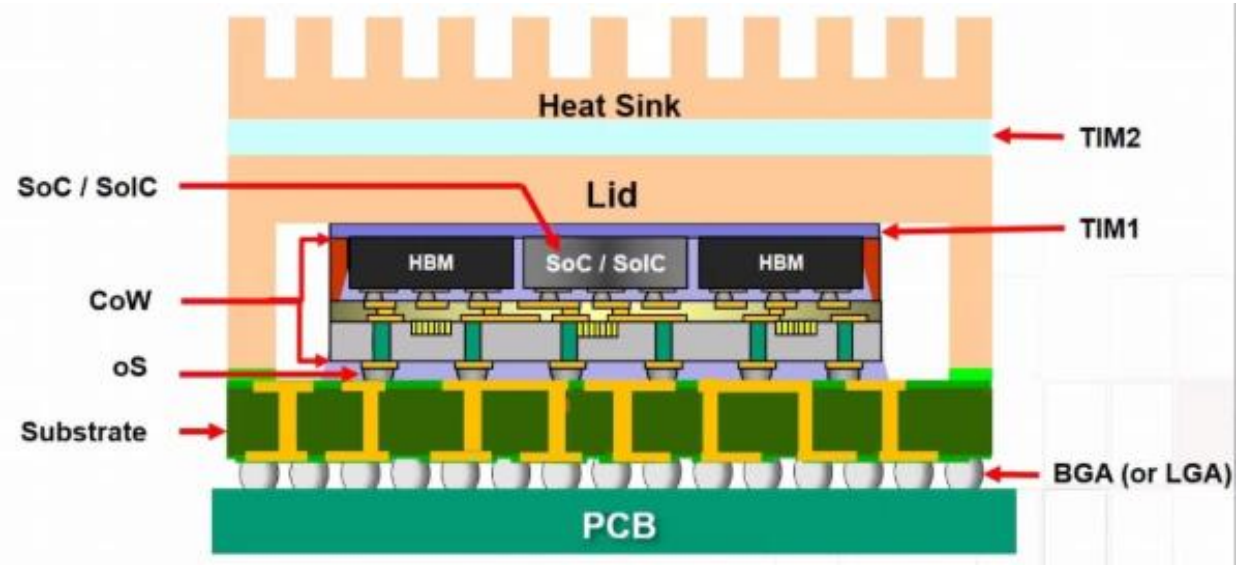
CoWoS-L is the new variant of TSMC's chip-last packaging technology. It adds in the Local Si Interconnect in combination with a RDL to achieve higher bandwidth than just an RDL packaging implementation (CoWoS-R) and will be more cost-effective than a full silicon interposer implementation (CoWoS-S).

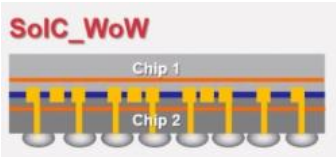


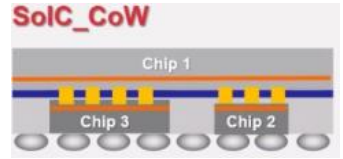
Source: TSMC

3D SOC/SOIC PACKAGING (USING HYBRID BONDIND APPROACH)

3DFabric building blocks







- SoC/TSV
- SoIC hybrid bond
- Si, RDL, embedded Si/RDL interposers
- Integrated IPDs/DTC
- Mass reflow/LAB/TCB
- Substrate
- TIM & Thermal
- PCB (BGA/LGA)

Path to SoIC: technical requirement

- From Bump to SoIC
  - Bonding alignment accuracy: 5-20um (bump) to <0.5um (bumpless)
  - Bonding interface defect: 10um to <1um
  - Topography: um to nm
  - Die warpage: 60-100um to 10-20um
- Stringent equipment capability & process control critical for high yield

HYBRID BONDING STATUS

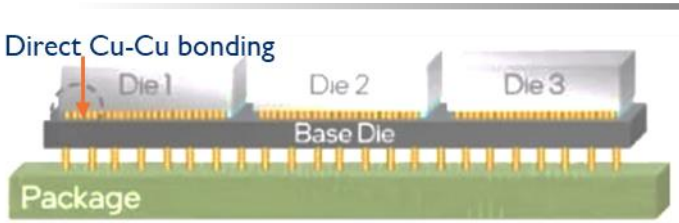
Types	Application	Production Status	Key players
W2W	CIS, 3D NAND	HVM	Sony, YMTC, Samsung, TSMC, Global Foundries
D2W/D2D	Heterogeneous integration (logic to logic, logic to memory, logic to active Si interposer)	Qualified, HVM in 2022	TSMC, AMD, Intel, Samsung, UMC, Global Foundries
	3D memory (HBM, 3DS), logic to logic	Development, HVM in 2023/ 2024	Samsung, SKHynix, Micron, TSMC

Hybrid bonding for D2W and D2D, nevertheless, comes with severe technological challenges:

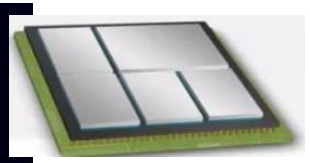
- Unprecedented placement accuracy below 200 nm at each point of the chip
- ISO 3 cleanroom class at the processing area to ensure void-free bond interfaces
- High productivity of > 3000 units per hour (UPH)
- CMP: Recess between Cu and dielectric
- Dicing method to ensure minimum particle generation

HETEROGENOUS INTEGRATION: INTEL CORPORATION

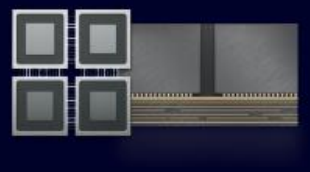
During Intel Architecture Day 2021, Intel announces Foveros Direct using hybrid bonding. Planned to entry the market in 2023, enlarging Intel'a advanced packaging toolbox. As such, EMIB and Foveros will be be Mix and Match -ed for High Performance Computing Applications..



Continued leadership in advanced packaging



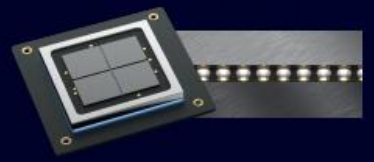
Embedded Multi-die Interconnect (EMIB)



bump pitch **50-40 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

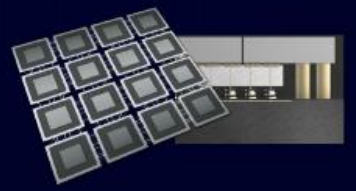
Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

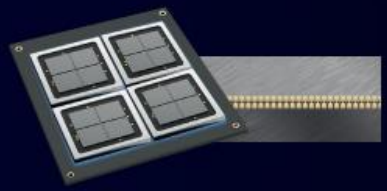
Foveros Omni



bump pitch **~25 microns**

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

Foveros Direct



bump pitch **< 10 microns**

- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

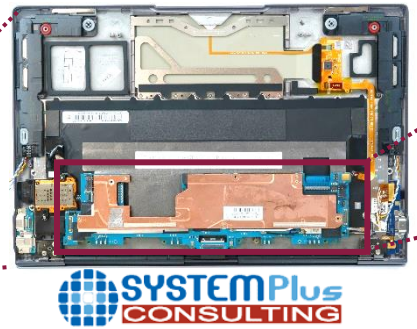
Source: Intel Accelerated 2021 Event

INTEL PROCESSOR WITH 2.5D STACKING TECHNOLOGY

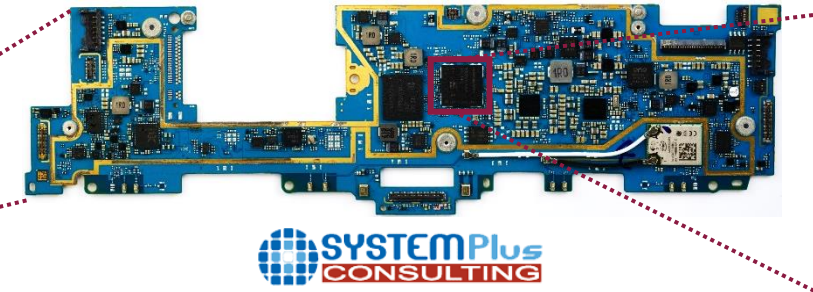
Intel's Foveros in the Samsung Galaxy Book S (1/2)

Samsung Galaxy Book S

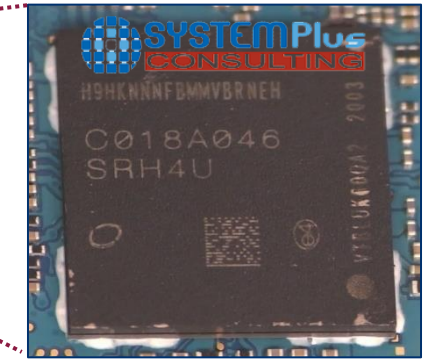
Samsung Galaxy Book S Teardown



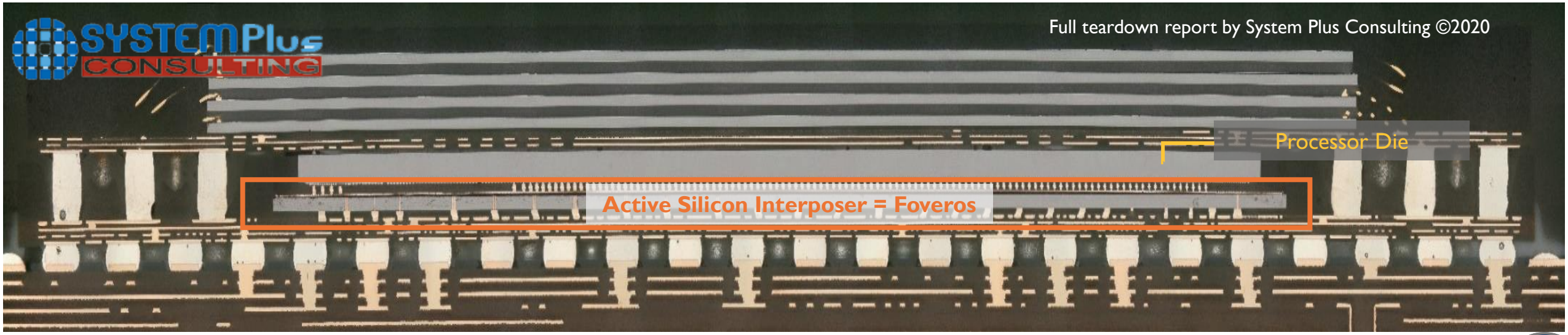
PCB Board



Intel Core i5-L16G7 3D Package



Cross-Section (Optical View) of Intel Core i5-L16G7 3D Package



Source: System Plus Consulting ©2020

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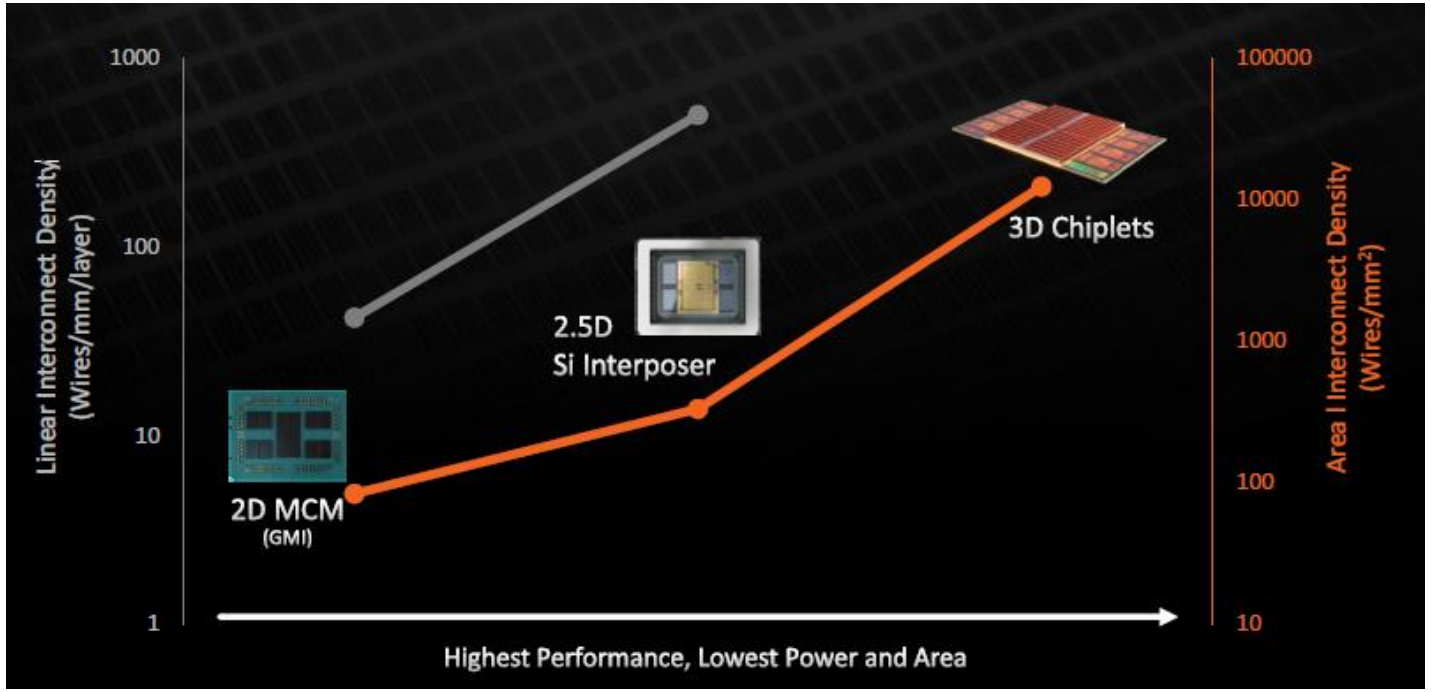
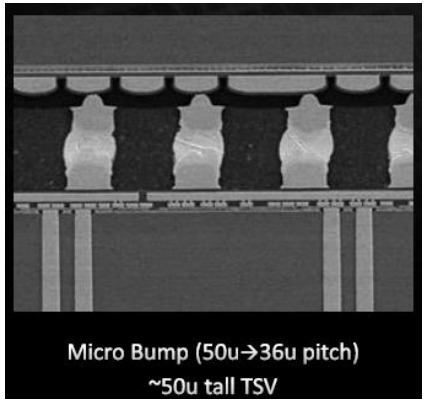
AMD ADOPTION OF SOIC HYBRID BONDING FOR HPC APPLICATION

AMD package roadmap



Migration from micro bump to hybrid bond: >15X interconnect density compared to microbump
>200X Connection Density Compared to On-Package 2D Chiplet
> 3X Interconnect Energy Efficiency Compared to micro bump 3D

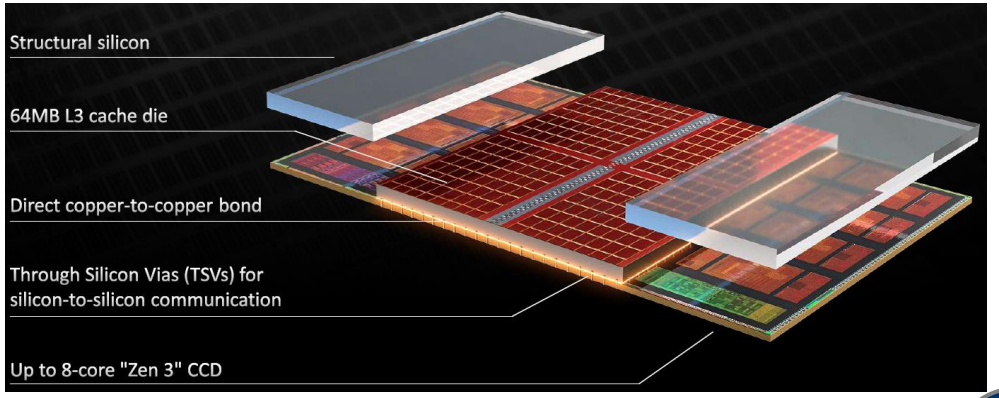


Source: AMD

Last year, AMD demonstrated the 3D chiplet stacking called 3D V-Cache. The Ryzen 5000-series microprocessors incorporate one or two Core Complex Dies (CCDs) along with an I/O Die (IOD). The V-Cache is a 64 MiB SRAM die that is said to be fabricated on TSMC's 7-nanometer process. The V-Cache die is thinned and is then stacked directly on top of each CCD directly above the existing L3 cache area using hybrid bonding.

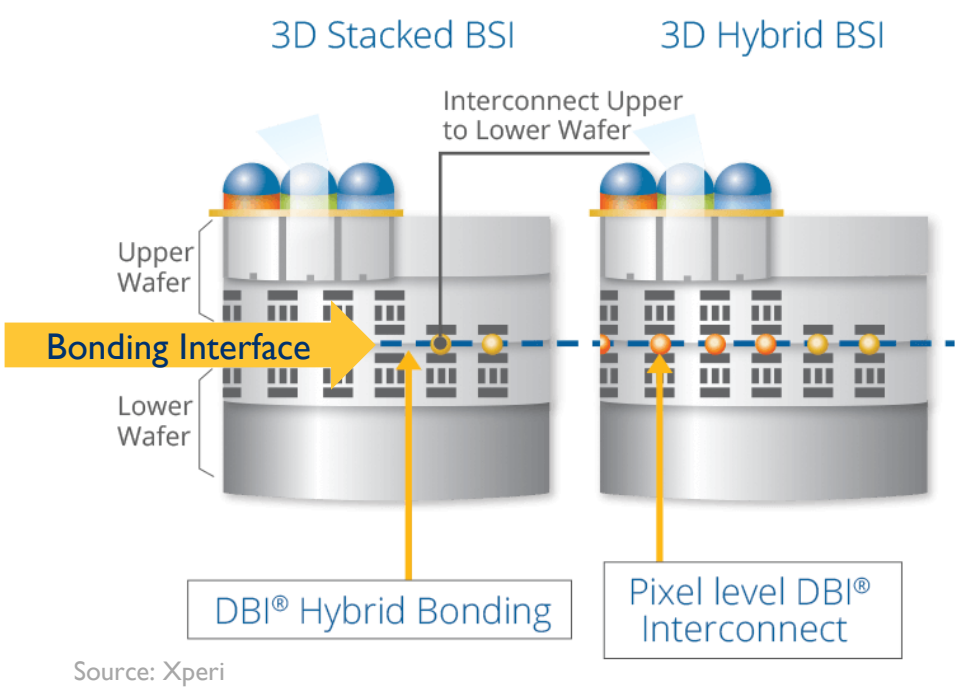
Two AMD products are planned to be launched in 2022 using hybrid bonding:

- AMD Ryzen processor with incorporated 3D V-CacheTM technology dedicated to gaming applications.
- Milan–X CPU with 3D V-CacheTM technology allowing SRAM Cu-Cu interconnection with CPU based on Zen 3 architecture (TSMC 7nm+) dedicated to server applictaions.

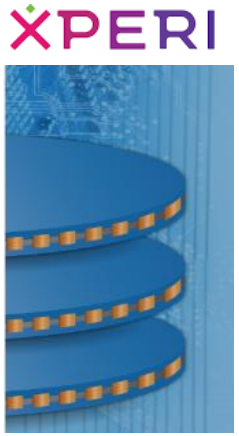


FOCUS ON CIS: XPERI AND SONY

Applications of DBI®: W2W Hybrid Bonding

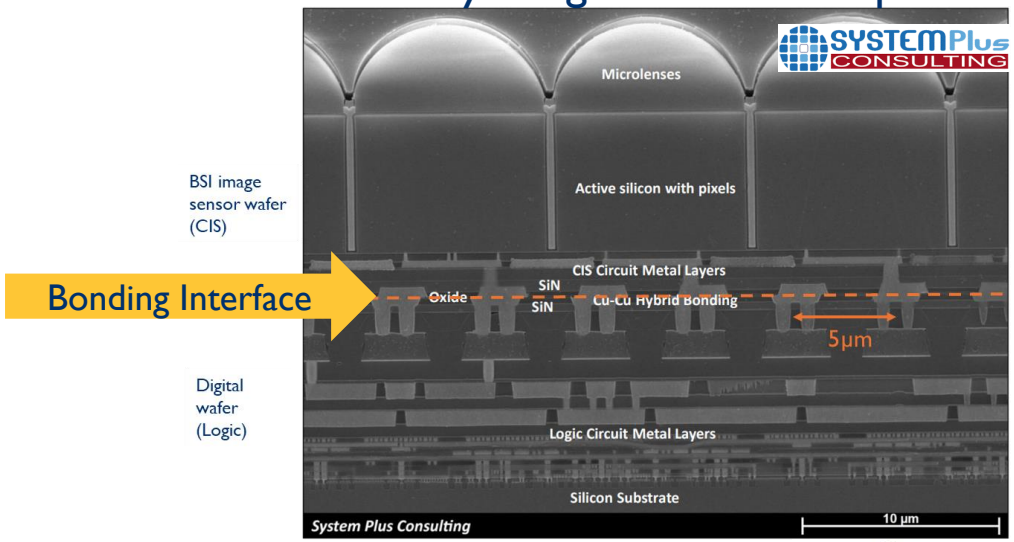


Source: Xperi

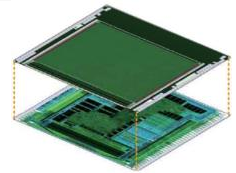


Source: Xperi

Sony Image Sensor Example



SONY



DBI wafer fabrication has been in volume production since 2015 (Sony CIS implemented in Samsung Galaxy S7) on **W2W** level, for **CMOS image sensor (CIS)** solutions in high-end smartphones. Next big applications are expected for Industrial (barcode reader, surveillance camera, and machine vision) and Automotive (ADAS)

STACKED MEMORY WITH HYBRID BONDING

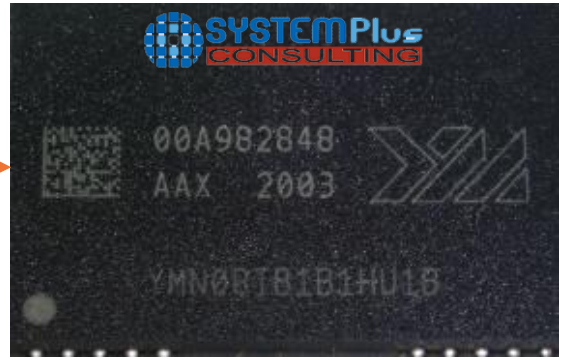
YMTC'S 3D NAND X-STACKING in GLOWAY SSD

Gloway 512GB SSD

Opening of Gloway 512GB SSD

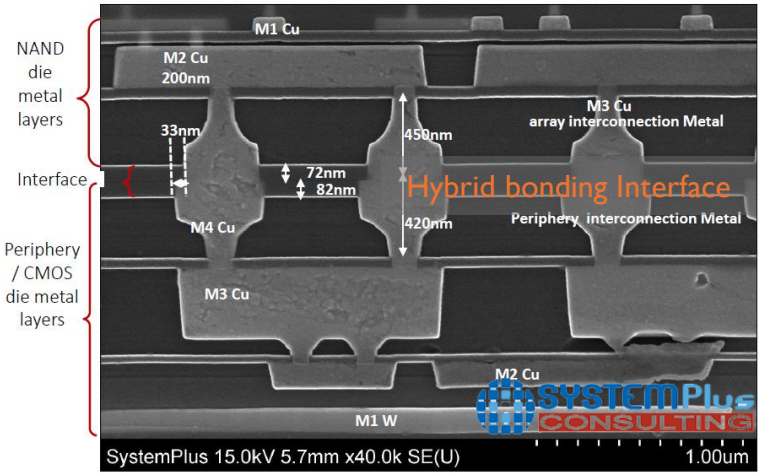
YMTC 128GB 3D NAND X-Stacking

Total 4x 125GB found in top/bottom PCB



Cross Section of 3D NAND X-Stacking

3D Hybrid Bonding

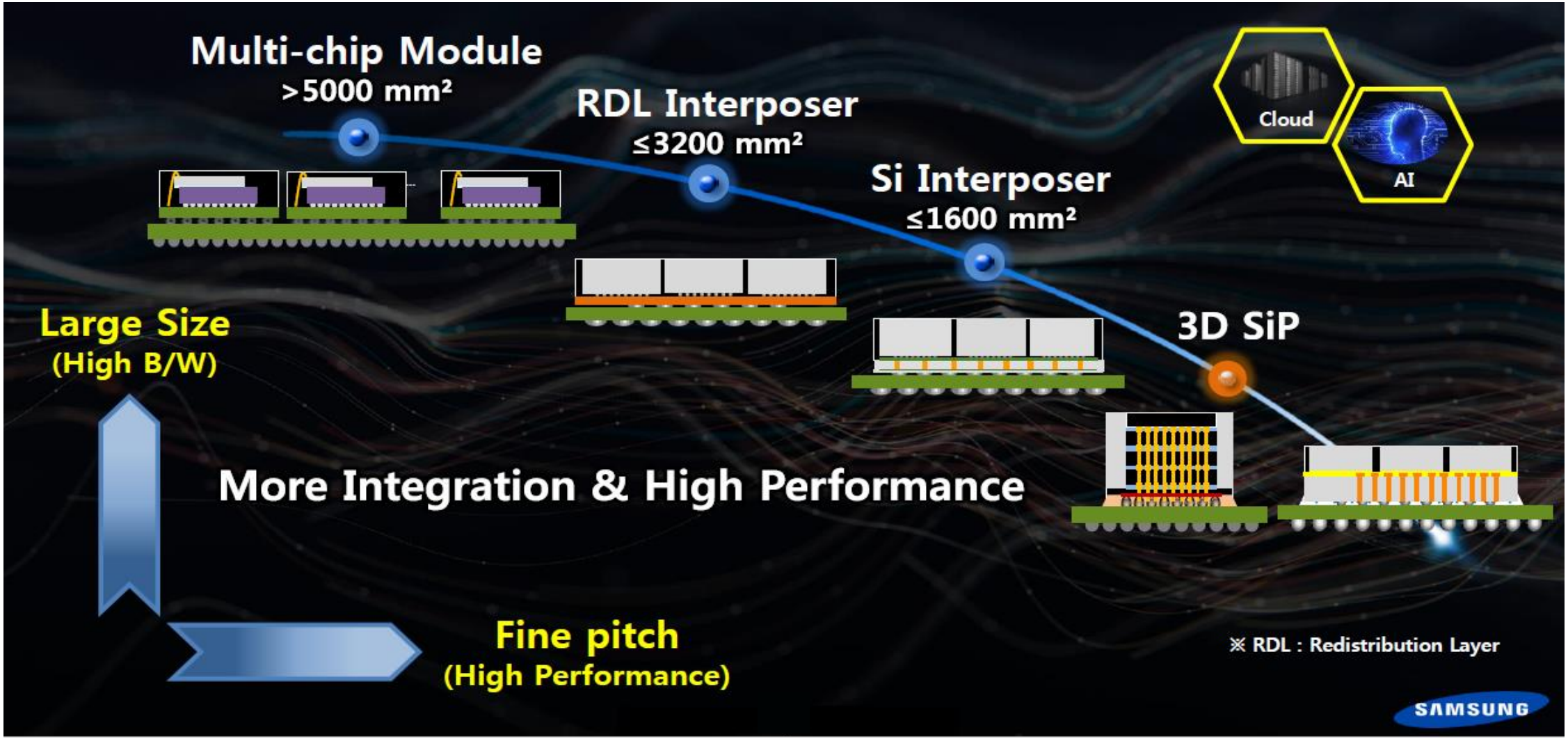


Gloway 512 GB SSD is targeted to enable faster boot-up, shutdown, application load and response, due to YMTC's new 3D Hybrid Bonding X-Stacking technology from YMTC. There is a shorter communication path between CMOS and NAND cells as compared to 3D NAND, hence, Gloway is expected to read/write 20 times faster (Sequential Read Speed: 540 MB/s and Sequential Write Speed: 450MB/s) as compared to a normal hard drive. More reliable, stable and durable than a hard drive by using 3D NAND technology.

The bonding interface is done by chemical bonding between the two wafers, NAND Array and Periphery CMOS. The physical interaction between the dielectric material and the metal material in the two wafers forms the bond – Hybrid Bonding.

SAMSUNG'S ADVANCED PACKAGING TECHNOLOGY ROADMAP

AI/HPC/Server Platform revolves around High-end Packaging



Source: Samsung Foundry

SAMSUNG LATEST DEVELOPMENT

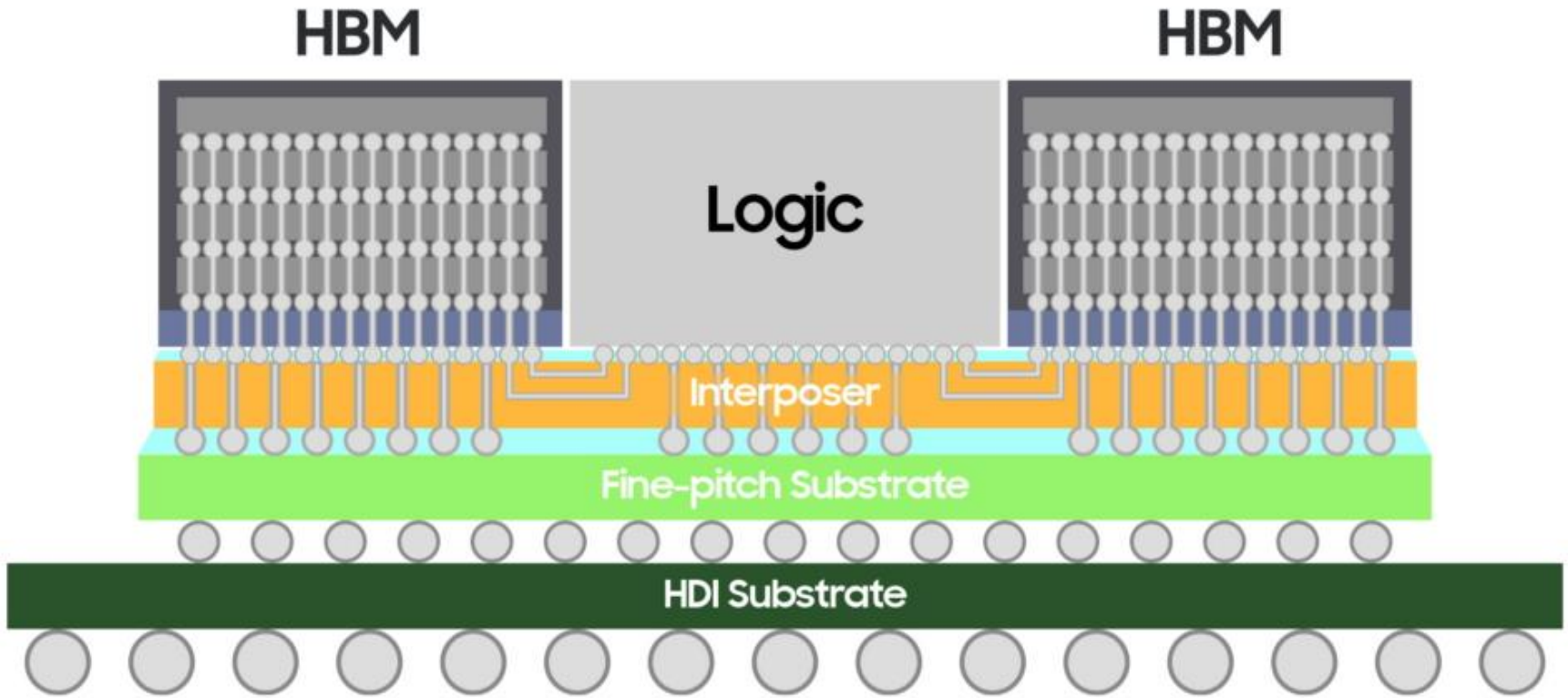
Samsung's H-Cube

H-Cube Structure & Features

2,5D Package

- Logic Chip
- 6 HBMs
- Si Interposer
- Fine-pitch Substrate
- HDI Substrate

Hybrid substrate



H-Cube™ Package Structure Concept - Source: Samsung

- ✓ Improved reliability
- ✓ Minimized signal loss or distortion
- ✓ Lower cost

Thanks!

ACKNOWLEDGEMENT