18TH INTERNATIONAL CONFERENCE & EXHIBITION ON
DEVICE PACKAGING
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Design and Analysis Challenges of 3D Multi-Chiplet Heterogenous Architectures

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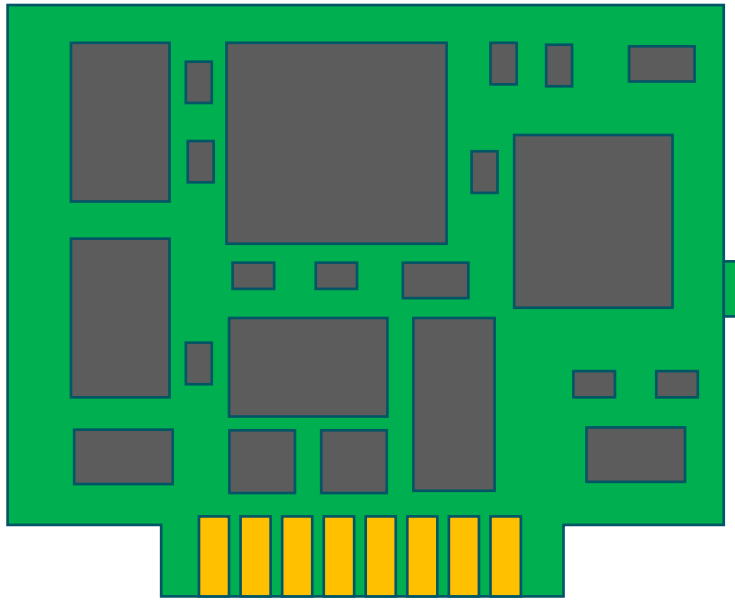
SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures

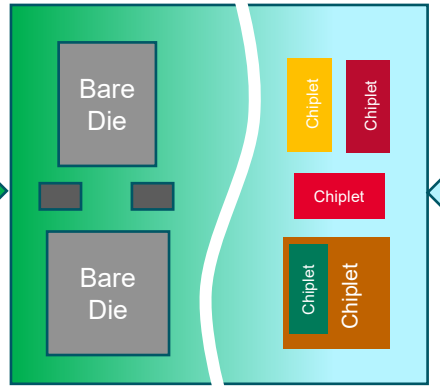
The transition from system on a chip (SoC) to system in a package (SiP)

PCB → Board size/complexity reduction (SWaP) → **Multi-Chip(let) Packaging (Including vertical stacking)** ← Disaggregated SoC ← **SoC/ASIC**



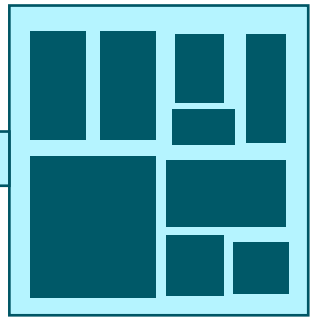
MCM/SiP

Unpackaged die



Heterogeneous Integration

Chiplets

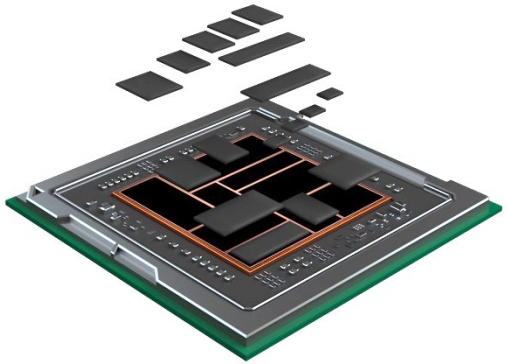


PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

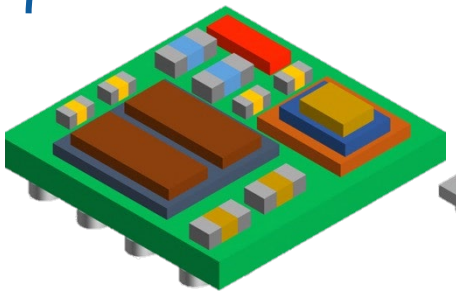
SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

Heterogenous Integration Leverages Multiple Packaging Technologies

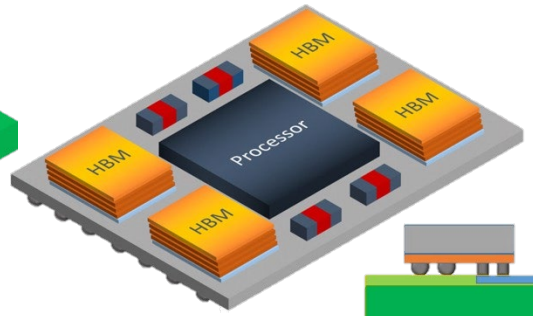
Including 3D packaging and 3D integration technologies



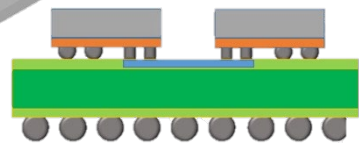
Heterogeneous Integration



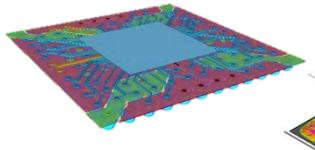
System in Package (SiP/MCM)



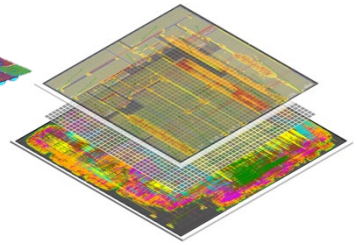
2.5D-IC (Silicon/RDL Interposer)



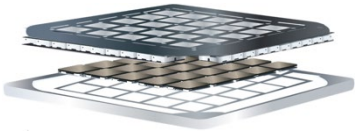
Embedded Bridges



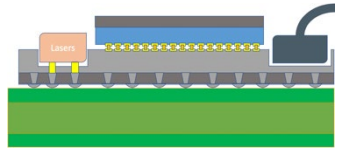
FOWLP (Ultra-High-Density RDL)



Bumpless 3D Integration



3D System-on-a-Wafer



Co-Packaged Optics

1990 2010 2012 2015 2018 2020 2022

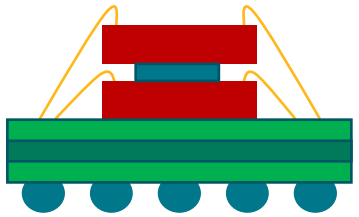
3D Packaging (Back-End 3D) vs. 3D Integration (Front-End 3D)

System-Level Design and Analysis Tools

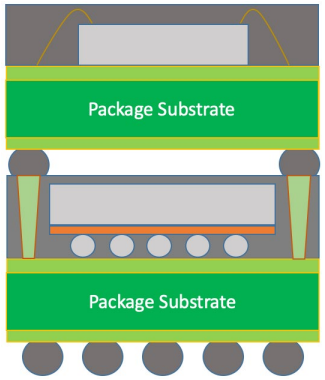
Hybrid (Package-Style Layout with IC-Style Verification)

IC Design and Verification Tools

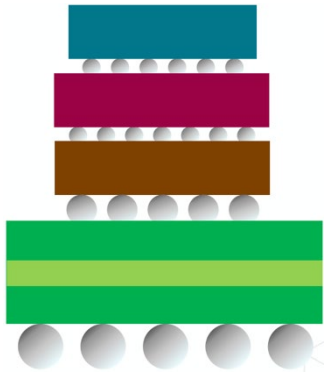
3D Packaging



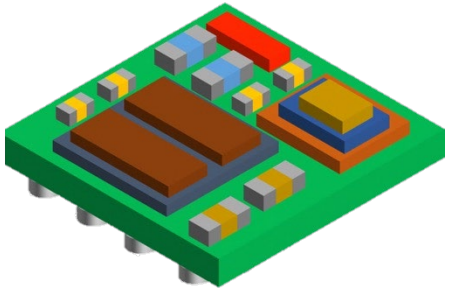
Wire-bonded BGA



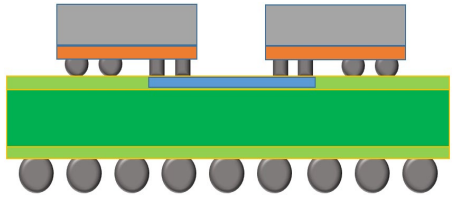
Package on package (PoP)



Micro-bump stacking

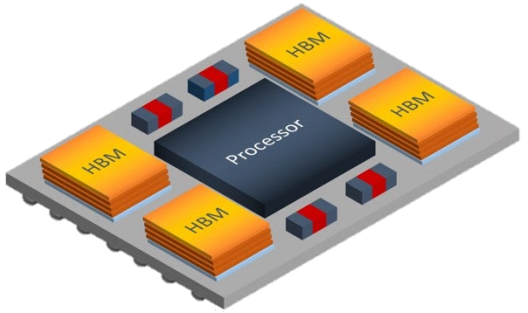


SiP/MCM

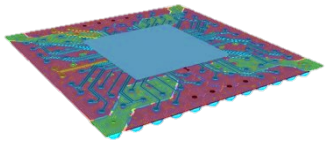


Embedded bridges

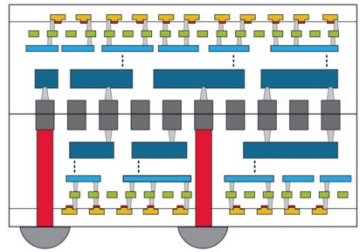
3D Integration



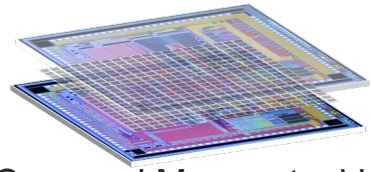
Silicon (TSV) interposer



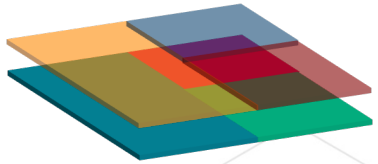
FOWLP (Ultra-high-density RDL)



Bumpless stacking
Cu-to-Cu bonding
Direct bonding
Hybrid bonding



Core and Macro stacking



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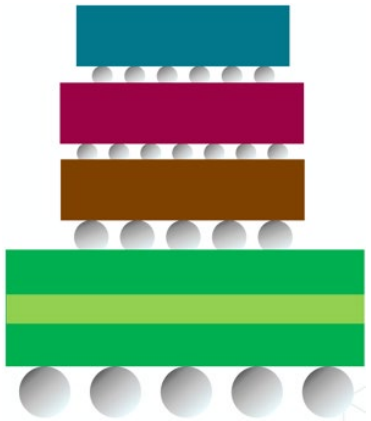
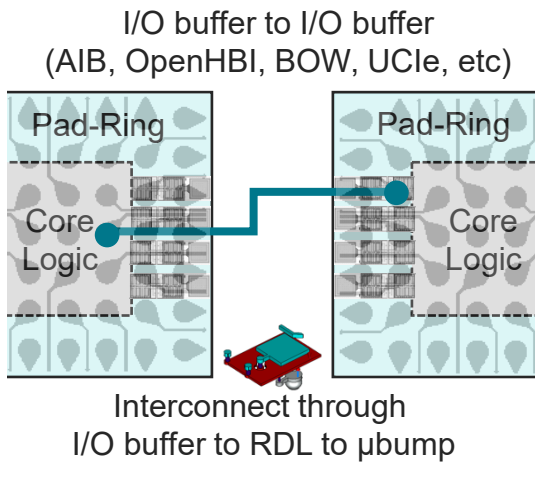
3D Packaging Versus 3D Integration

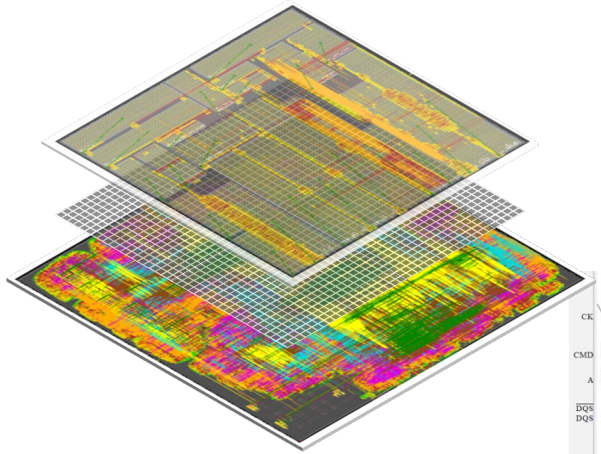
3D Packaging

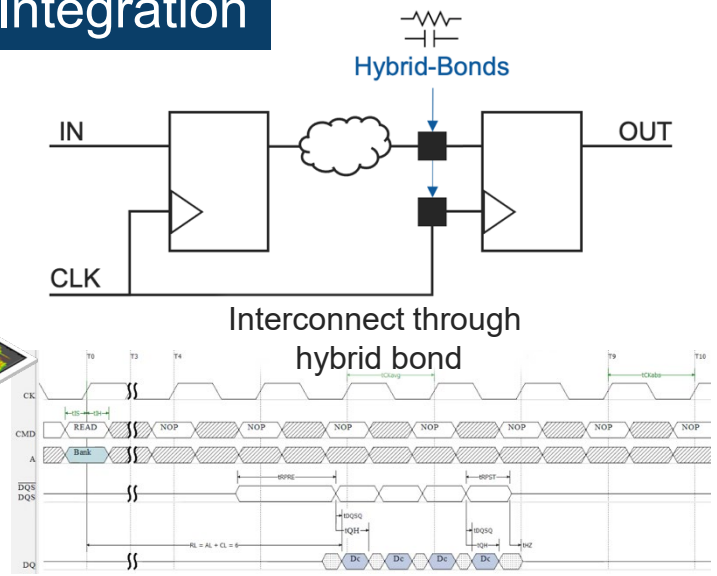




- (Micro)Bumped
  - Timing closed/signoff each die separately
  - Typically, no concurrent design of the dies
  - Common approach for Memory and CIS for over 5 years

3D Integration



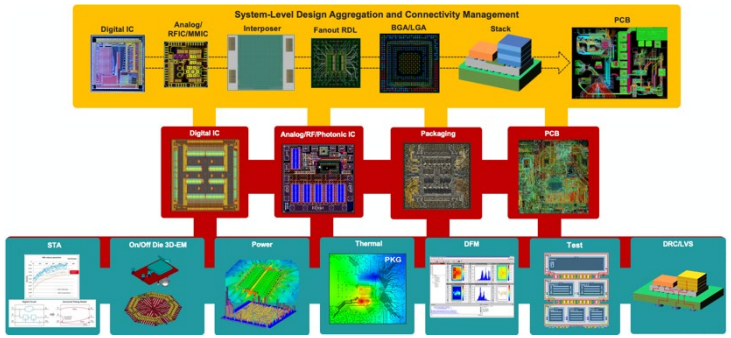


- Bump-less (Hybrid-bond/Cu-to-Cu bond, Direct bond)
  - No I/O buffers between die/macros
    - Concurrent design/analysis mandatory
    - Timing-driven routing and STA required for digital designs
    - Cross-die/chiplet route resource sharing
    - Z-dimension placement

Multi-Chiplet 3D Ecosystem Challenges

Chiplet
Physically realized and tested (hardened) IP with standard communication interface Primary component to heterogeneous integration

Interface Considerations Serial, Parallel or Proprietary
Package type
Reach (on/off package)
Power (pJ/bit)
Latency
Speed
Bandwidth
Routing complexity
Test, ESD, ???



Assembly Design Kits

- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
  - OSATs have large design centers to off-set this limited formal sharing of design requirements
- Foundries are helping to drive the concept of a PDK into the packaging world

Commercialization and Standards for Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
- Exchange formats
- *Common* communication interface
  - UCIe, BoW, OpenHBI, …
  - Might be too many packaging options to standardize on a single interface

Developing a Design Methodology

- Explosion in the number of design tools required
- Die designer vs package designer, who's best suited
- Collaboration/co-design across multiple tools, design teams and across multiple companies
- Design partition strategies including D2D chiplets, thermal and off-package IO
- Rapid prototyping with risk mitigation strategies

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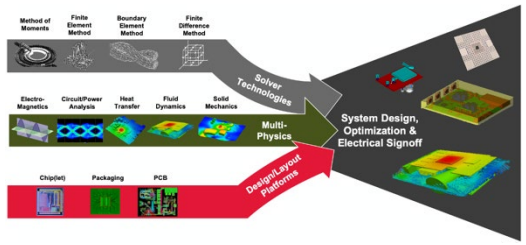
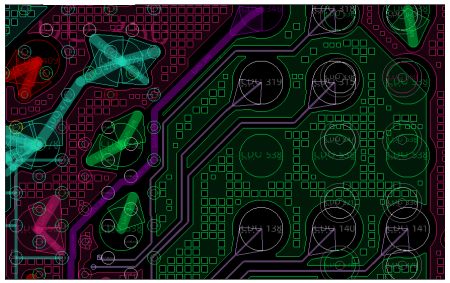
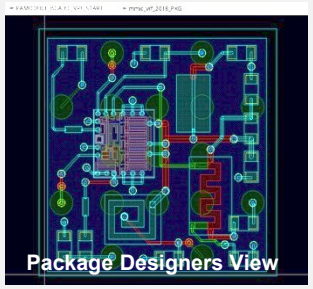
Packaging Challenges

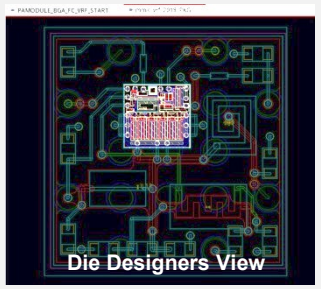




Cross-Domain Co-Design

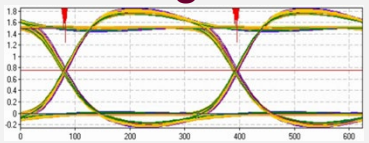
- Single view of IC, package and PCB layouts
  - Abstract-level for early planning
  - Detailed-level for physical co-design
- Tight-loop ECO process
- System-level LVS

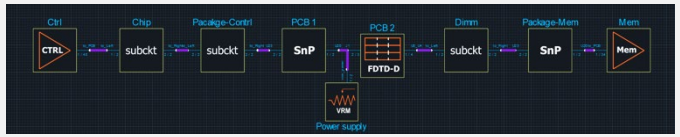




System-Level Analysis

- PCB-like analysis capabilities
  - Chiplet-to-chiplet signal integrity and compliance
  - System-level power analysis
- Multi-physics analysis
- On-die EM/IR coupled with off-die electromagnetics

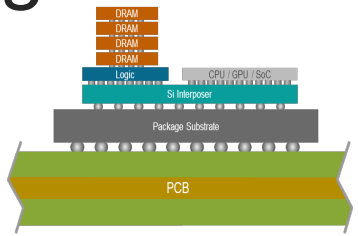


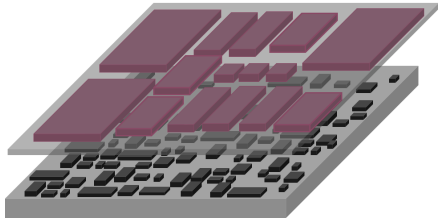


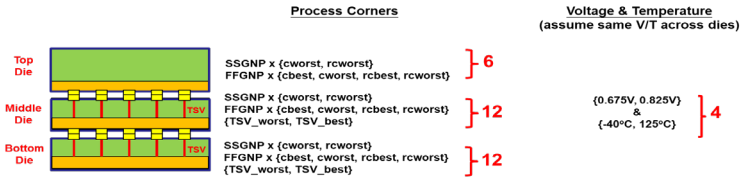
Silicon-Based Packaging Technologies

- Transitioning from laminate design to silicon design
  - Formal sign-off of DRC and LVS
- Differencing power/ground routing styles
  - Stripes/rails
  - Copper pour
- Advanced metal balancing
- Design capacity
  - Tens of thousands to hundreds of thousands (or more)

3D Integration Design and Sign-Off Challenges







System-Level Design Aggregation

- System-level assembly planning, optimization and risk management
- Common database for entire 3D-IC system
  - Chips, chiplets, tiles, packaging and PCB
- Early-stage thermal/power analysis
- Hierarchical netlisting
  - Source of golden/sign-off netlist
  - Partitioning by integration level

True Multi-Chiplet 3D Implementation

- Design size capacity
- Concurrent editing of multiple devices at full transistor-level detail
  - No abstraction
  - Homogenous and heterogenous
- On-the-fly die splitting and re-partitioning in Z direction
- Timing driven cross-chip(let) routing
- Support for 3D-IC test standards

3D-Enabled Analysis and Sign-Off

- STA with automated corner reduction
- Rule-deck-free system-level LVS
  - Alignment and connectivity checking
- Multi-die EMIR
  - Accounting for dynamic loading across multiple die
- Comprehensive thermal stress and CMP planarity checks

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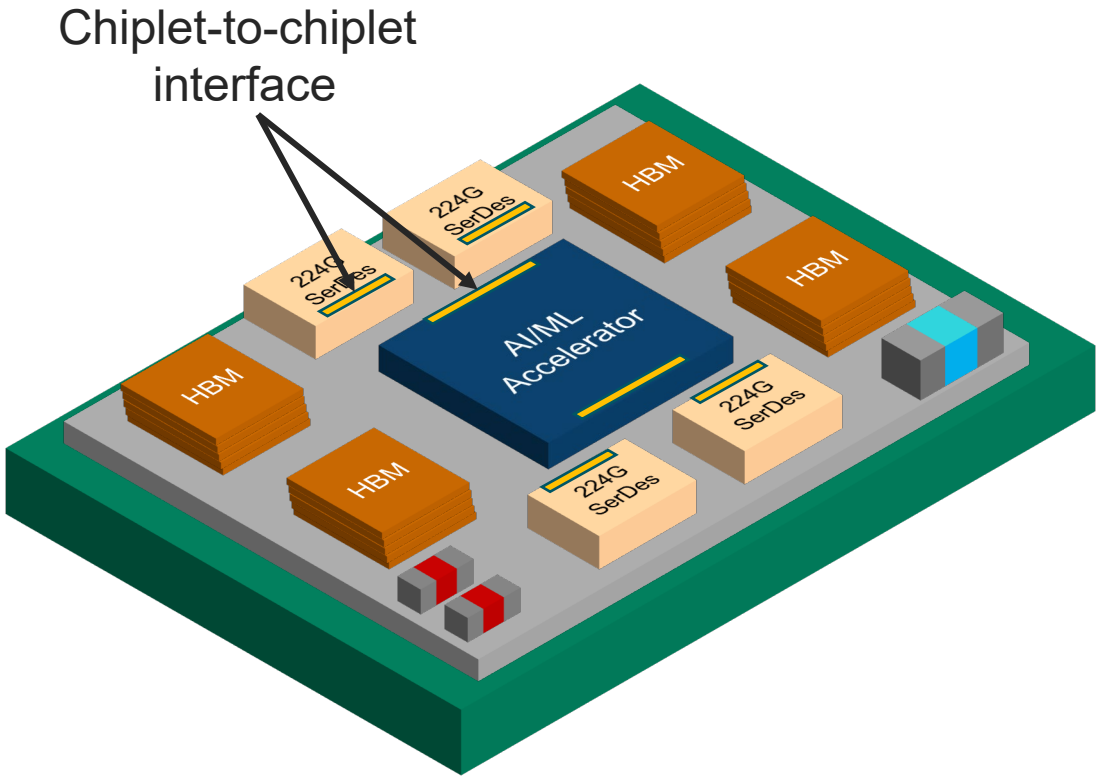
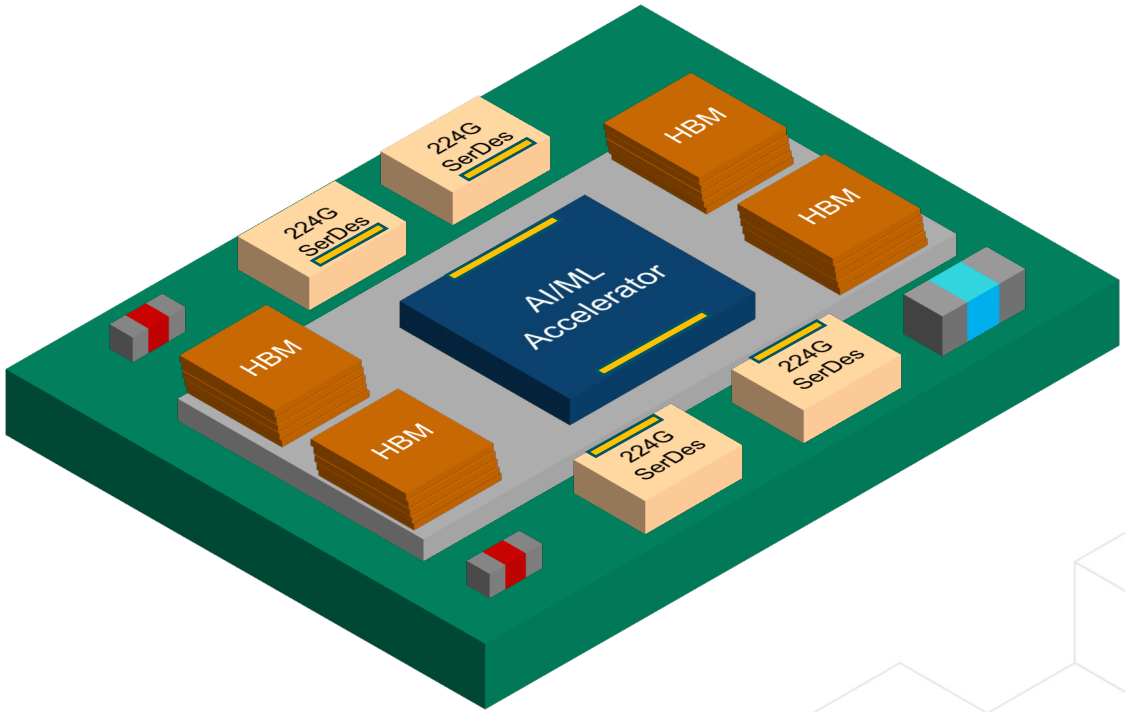
Example Challenge; Pre-Layout Planning
Model-based engineering

- Performance/Compliance impact of moving chip(let)s to different packaging tiers

Vs.





Chiplet-To-Chiplet Eye Mask Requirements

- Interconnect Specifications are provided for common communication interfaces
  - Before the design can be manufactured, electrical compliance of interfaces must be validated

Symbol	Parameter	Gen1 Mode and Gen2 Mode low-speed signals[2]			Gen2 Mode data and forwarded clock[3]		
		Near end	Trace	Far end	Near end	Trace	Far end
V_{EH}	Minimum difference between LO and HI (eye diagram height)			+/-90 mV			+/-50 mV
V_{HI}	Minimum output voltage for HI state	0.7 V			0.4 V		
V_{LO}	Maximum output voltage for LO state	0 V			0 V		
V_{OS}	Typical output swing	0.9 V			0.4 V		
V_{CM}	Common mode voltage	V_{OS} / 2			0.2 V +/- 10mV[1]		
t_{EW}	Minimum duration of valid output (eye diagram width) for data and forwarded clock	0.56 UI	0.1 UI	0.4 UI	0.65 UI	0.2 UI	0.4 UI
t_{BEW}	Minimum duration of valid output (eye diagram width) for receive-domain clock	0.66 UI	0.1 UI	0.56 UI	n/a	n/a	n/a

1. V_{CM} tolerance includes all board level effects, with power supply variation (e.g. regulator) within 5%.
2. "Gen2 Mode low-speed signals" includes all signals of Table 4 except *TX, RX, ns_fwd_clk, ns_fwd_clkb, fs_fwd_clk, fs_fwd_clkb.*
3. "Gen2 Mode data and forward clock" are the signals *TX, RX, ns_fwd_clk, ns_fwd_clkb, fs_fwd_clk, fs_fwd_clkb.*

Table 21. Electrical signal specifications

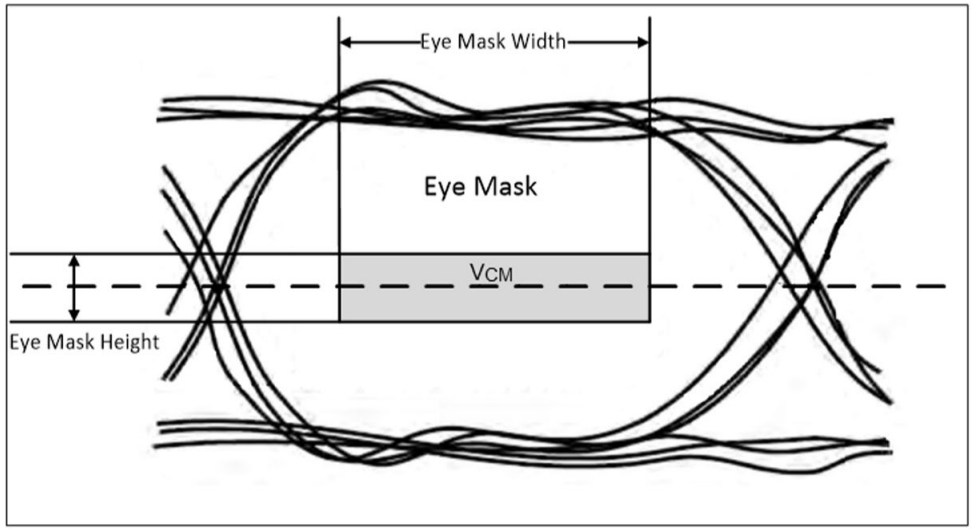
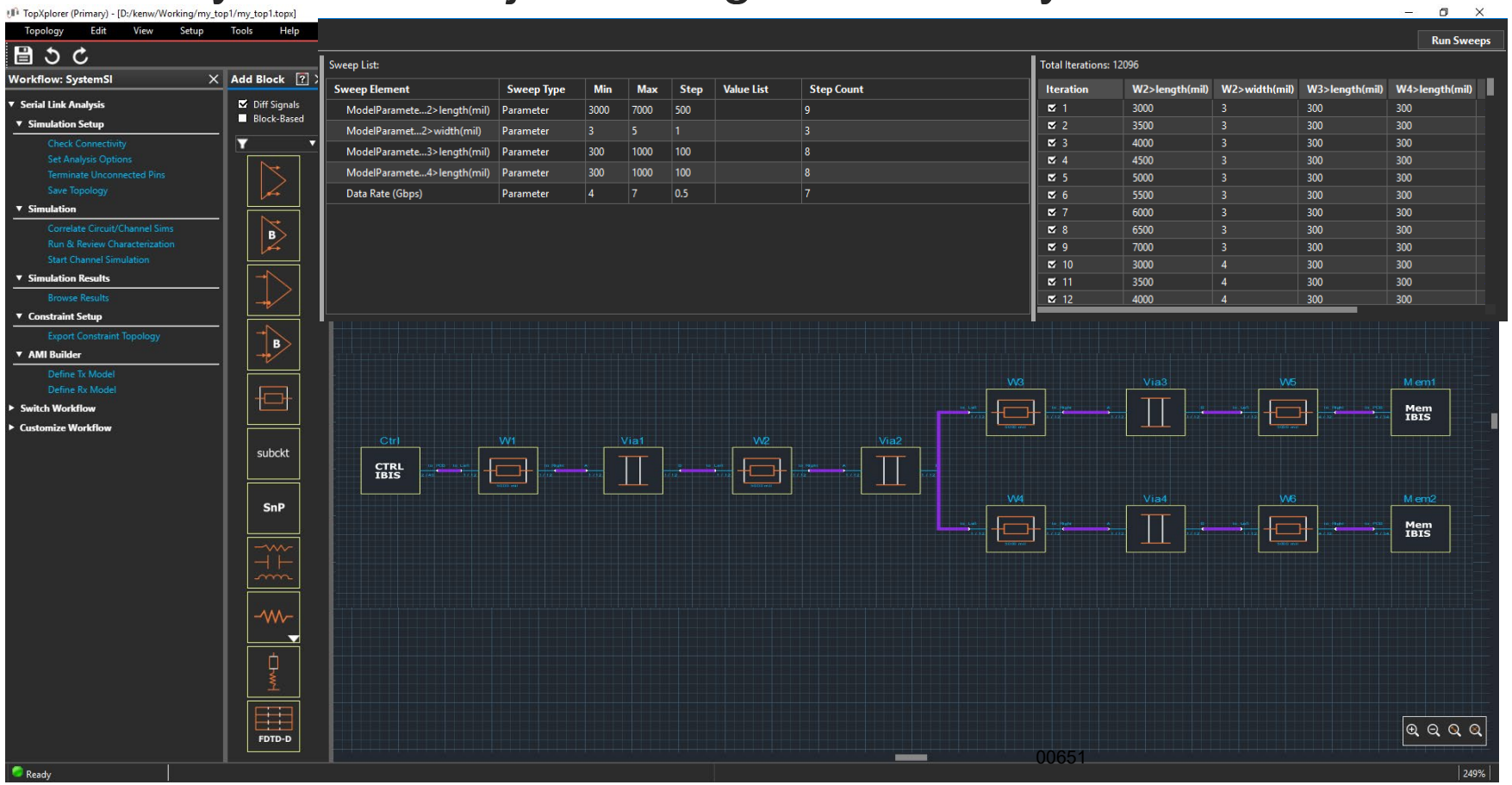
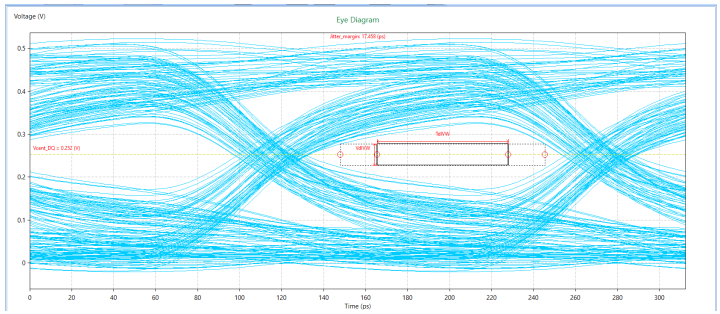


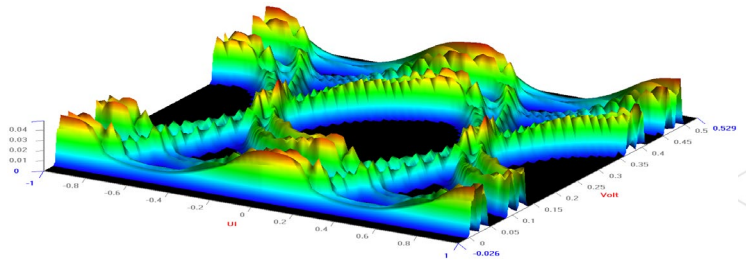
Figure 49. Compliance Eye Mask

Creating Interconnect Topology, Parametric Sweeping of Interconnect Characteristics and Displaying/Analyzing the Results

- Sweep parameterize lengths, subcircuit parameters, models, and more, to determine the solution-space and define layout constraints
- Verify noise and jitter margins vs. Rx eye mask for each signal







Channel simulation might be required to collect eye density, and extrapolate

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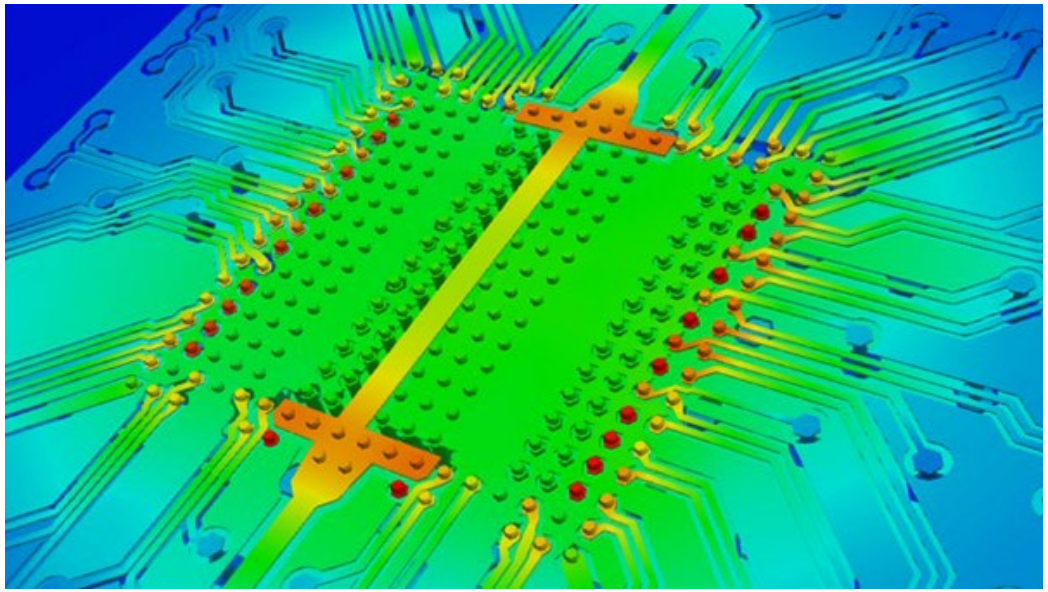
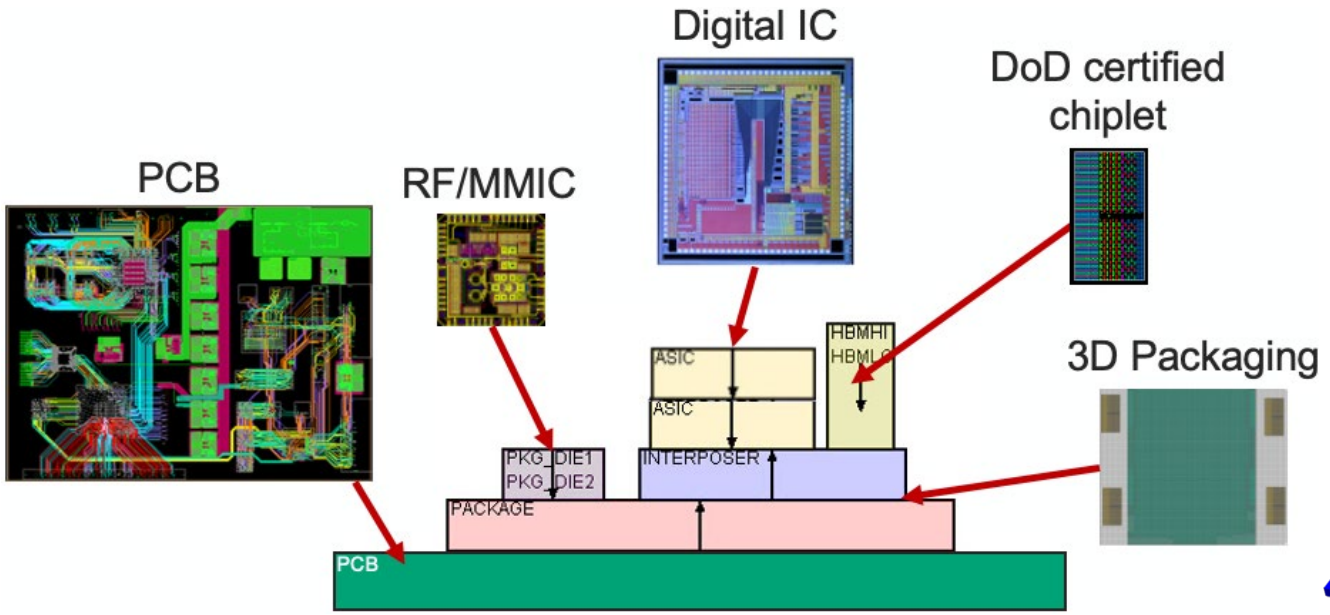
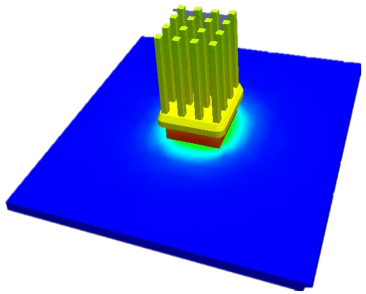
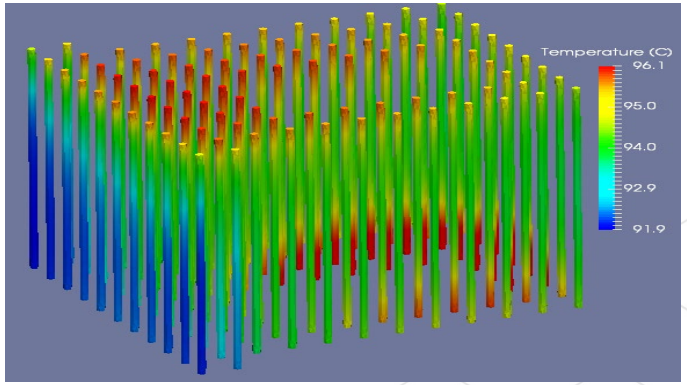
3D Integration Challenge: Early-Stage Thermal Analysis

- Aggregation and optimization platform
- Parametric user-entered data for bump height, material, underfill, molding compound, heatsink configuration, board size, etc









Summary

- 3D Integration Requires a Design Methodology Similar to IC Design
- Packaging Tools and System-Level Analysis Still Required to Complete the Design
- There are Several Challenges Facing Designers Moving to 3D Integration
- Is it Time to Reevaluate Your Design Methodology?