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DEVICE PACKAGING
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Heterogeneous integration of chiplets Lego-like IP for more than Moore

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Gordon E. Moore Observations

the number of transistors on a microchip doubles every two years, though the cost of computers is halved. This so called "Moore's Law" states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them. Another tenet of "Moore's Law" asserts that this growth is exponential

Expert opinions see these observations ending in the 2020's driven by:

1. Reticle limits
2. NRE costs
3. Availability of required IP
4. Yield
5. Die cost
6. Device scaling
7. Function aggregation
8. I/O scaling

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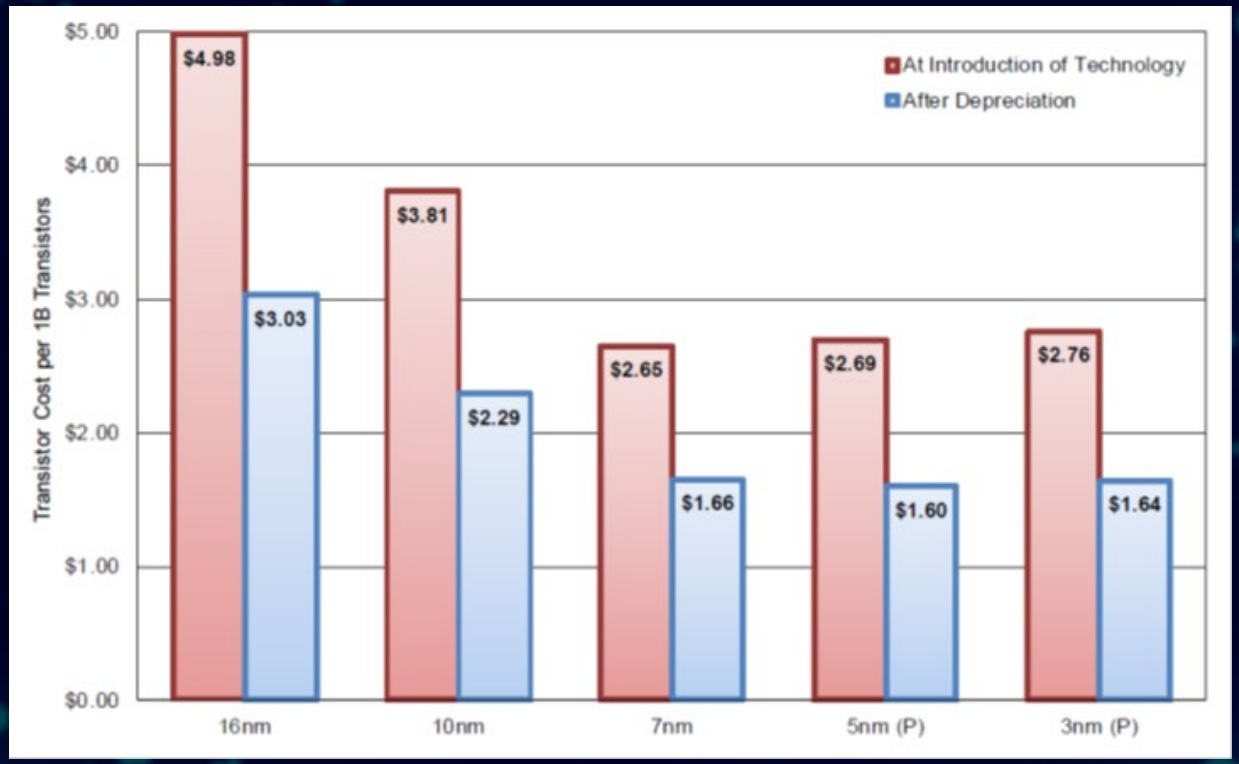
Transistor Costs

Trends



7nm the pivot point?

Monolithic forces all functions to be at same node

Memory and I/O not ideal

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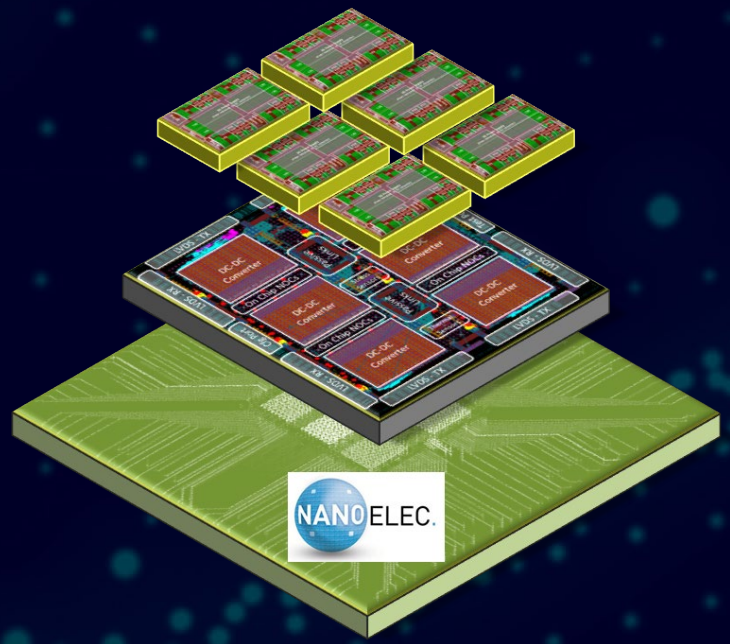
Technology inflection point

Trends



Cost and yield driving alternatives to monolithic solutions

- SOC disaggregation into hard IP or “chiplets”
- Multi-die implementation to avoid reticle limitations (vs. single die)

Data movement - low latency, high-bandwidth

- Use of High Bandwidth Memory (HBM)
- 3D memory directly stacked on logic
- High-speed IO for chip-to-chip interfaces

Heterogeneous integration provides path forward

- Supports multiple micro-architecture scenarios
- Leveraging 2.5 and 3D assembly platforms
- Utilizes System Technology Co-optimization (STCO)

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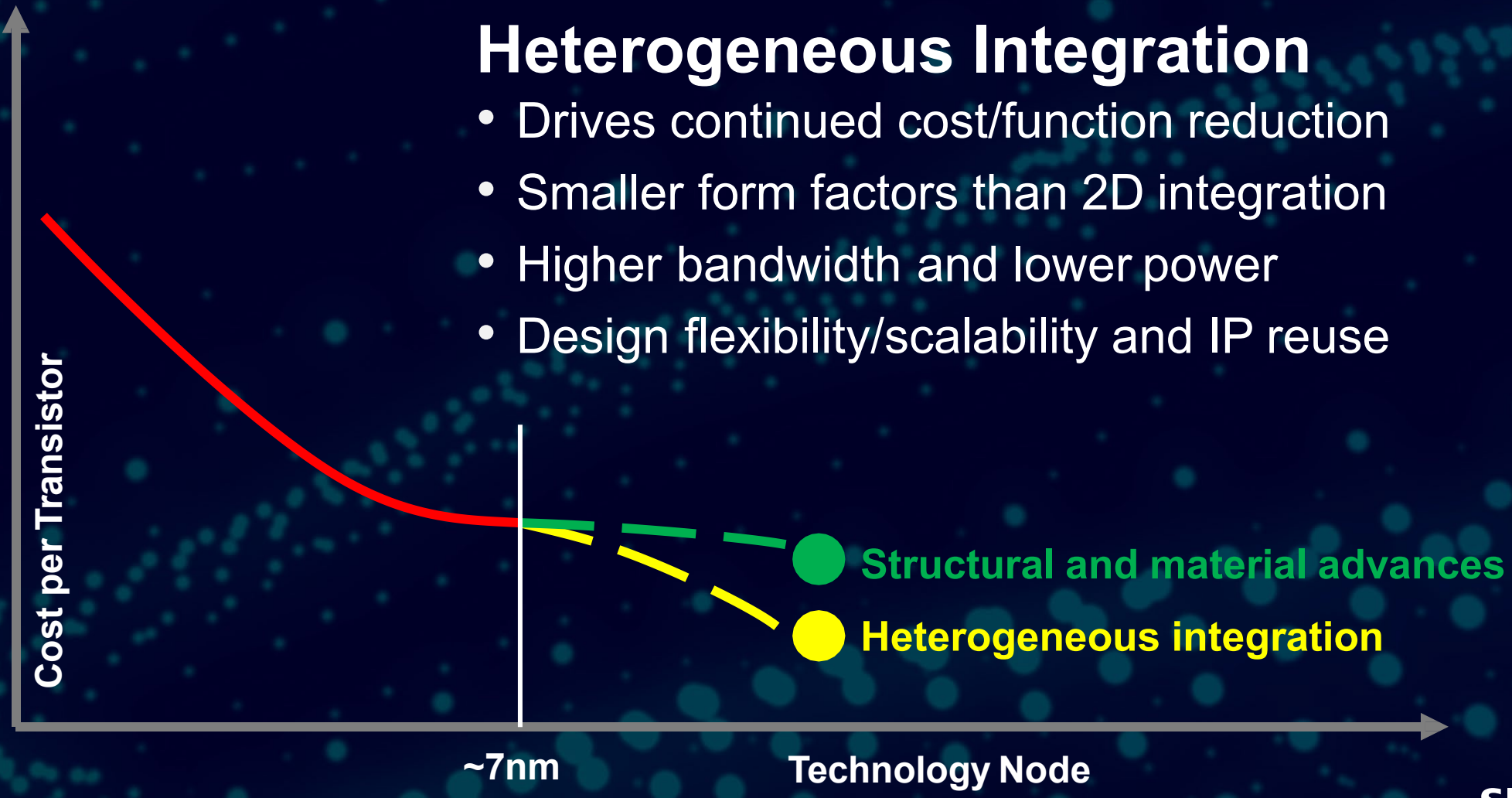
Extending "Moore's Law"

Trends

Heterogeneous Integration

- Drives continued cost/function reduction
- Smaller form factors than 2D integration
- Higher bandwidth and lower power
- Design flexibility/scalability and IP reuse



Heterogenous Integration path forward

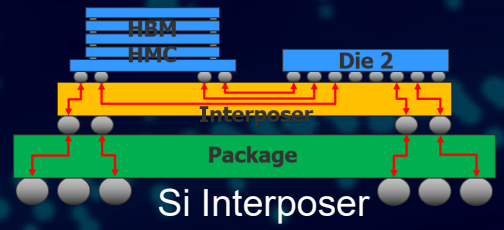
Trends

Enabling alternative Micro-architectures

High Bandwidth Memory (HBM)
ASIC Die Disaggregation
ASIC IP Disaggregation
2.5D Silicon Interposers, Fanout/RDL, Silicon Bridge
3D IC Stacked Die

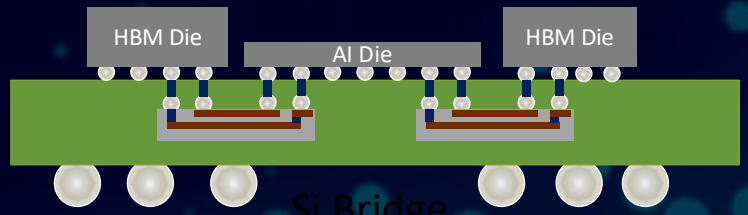
Key Benefits

Increased Performance
Reduced Power
Lower unit cost/NRE
Product Configurability

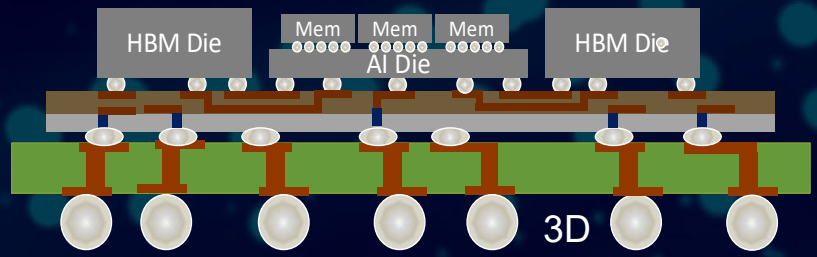


Si Interposer

Fanout/RDL



Embedded Bridge



3D

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Case study results

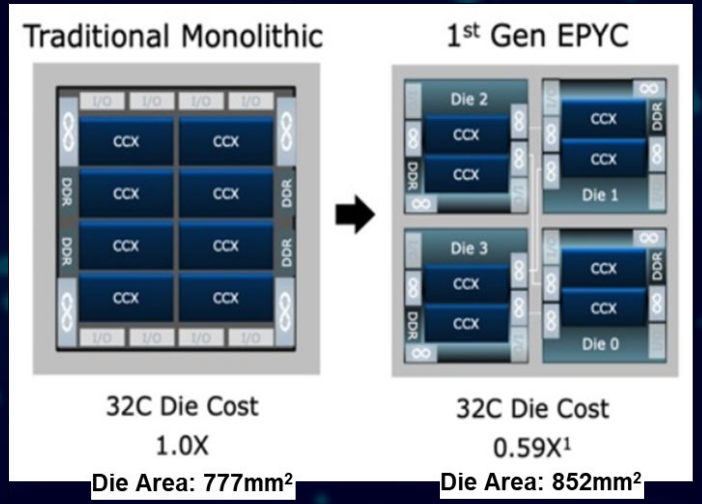
Trends

AMD Cost comparison of chiplets vs. monolithic

- 41% reduction in die cost and higher yield
- Maximize platform value – product configurability from single tape-out

Developing eco-system

- Standards for chiplet marketplace and exchange
- Turn-key design/build resources
- Materials suppliers



Presented at 2021 International Solid State Circuits Conference

	Monolithic	Diff	Chiplet
Wafer Cost (7nm)	$9,350	1x	$9,350
Total Die Size	600mm2	1.1x	660mm2
Single Die Size	600mm2		165mm2
Gross Die per Wafer	96		387
Defect Rate (per cm²)	0.2	1x	0.2
Effective Area	80%	1x	80%
Estimated Yield (Dingwall)	43%		78%
Net Die per Wafer	42		300
Single Die Cost	$224		$31
Total Die Cost	$224		$124
Total Test Cost	$10	1.2x	$12
Package and Packaging	$160	1.25x	$200
Packaging Loss	1%	4x	4%
Total Manufacturing Cost	$398		$347

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Chiplets

Trends

Enabling modular function design

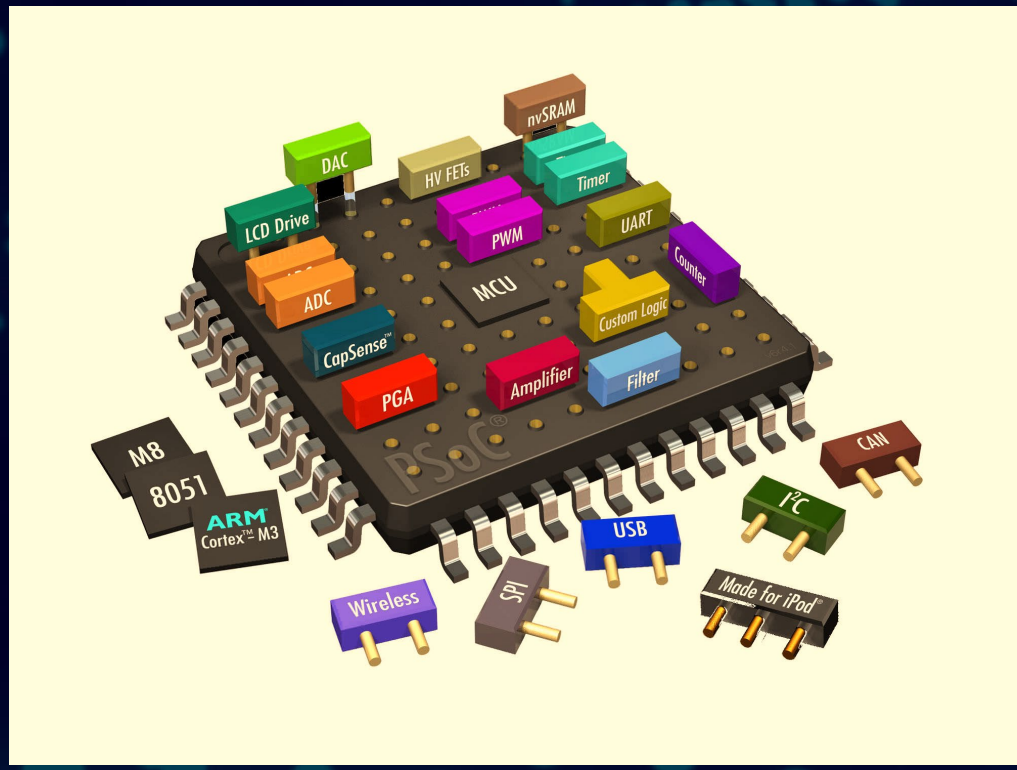
- No need to own/design full stack
- Aggregated with custom ASIC(s)

Fabricated using ideal nodes

Integrated through standardized interfaces and CDK's

Commercially available

Low NRE and fast TTM



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Success with Chiplets

Needs

Chiplet design kits

Heterogeneous planning and co-optimization

Physical verification at every level of 3D assembly

Multi-domain testing

Ecosystem interoperability

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Standardized chiplet design kit

Needs

Open Domain
Specific Architecture

Machine readable models

JEDEC
Global Standards for the Microelectronics Industry

IEEE
Advancing Technology for Humanity

Standards

Documentation

Security and Traceability Assurance

Chiplet Design Kit (CDK)

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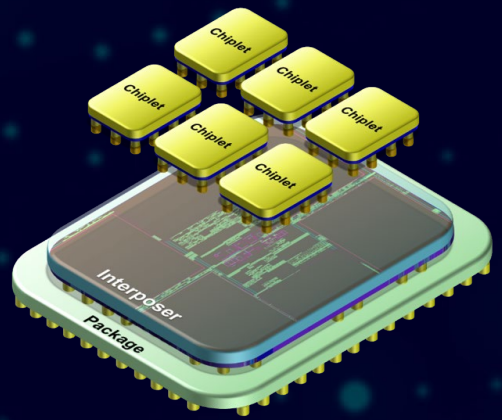
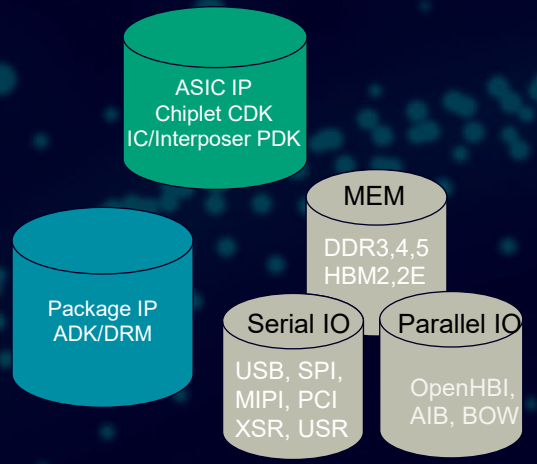
Chiplet ecosystem enablers

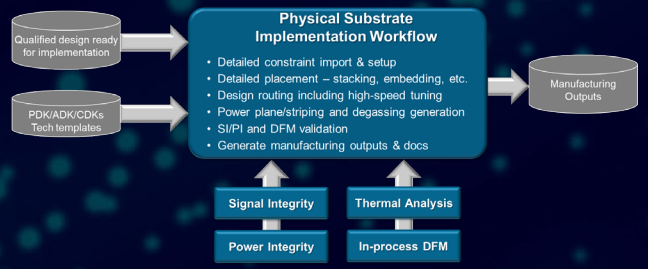
Needs



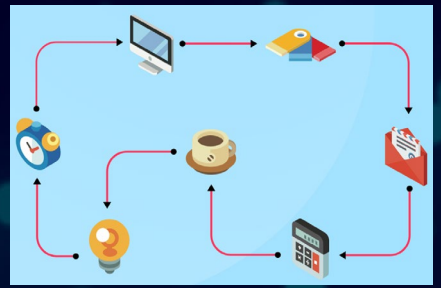
Technology



Intellectual property



Workflows/ design kits



Business models

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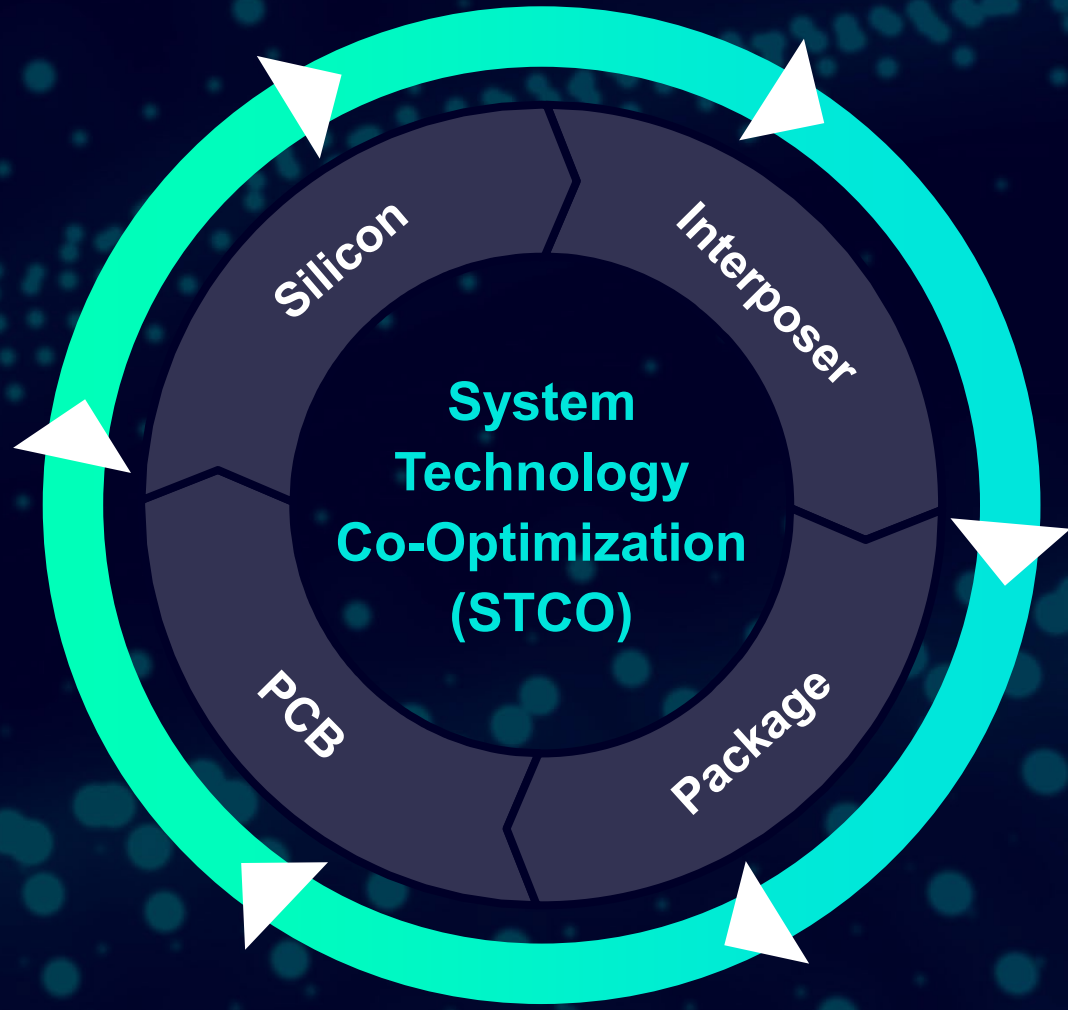
Heterogeneous Planning & Prototyping

Needs

- Single digital twin and system logi netlist
- System Technology Co-Optimization
- Predictive modeling to prototype and qualify design scenarios
- Replacement of spreadsheet-based flows as communication mechanism of design intent



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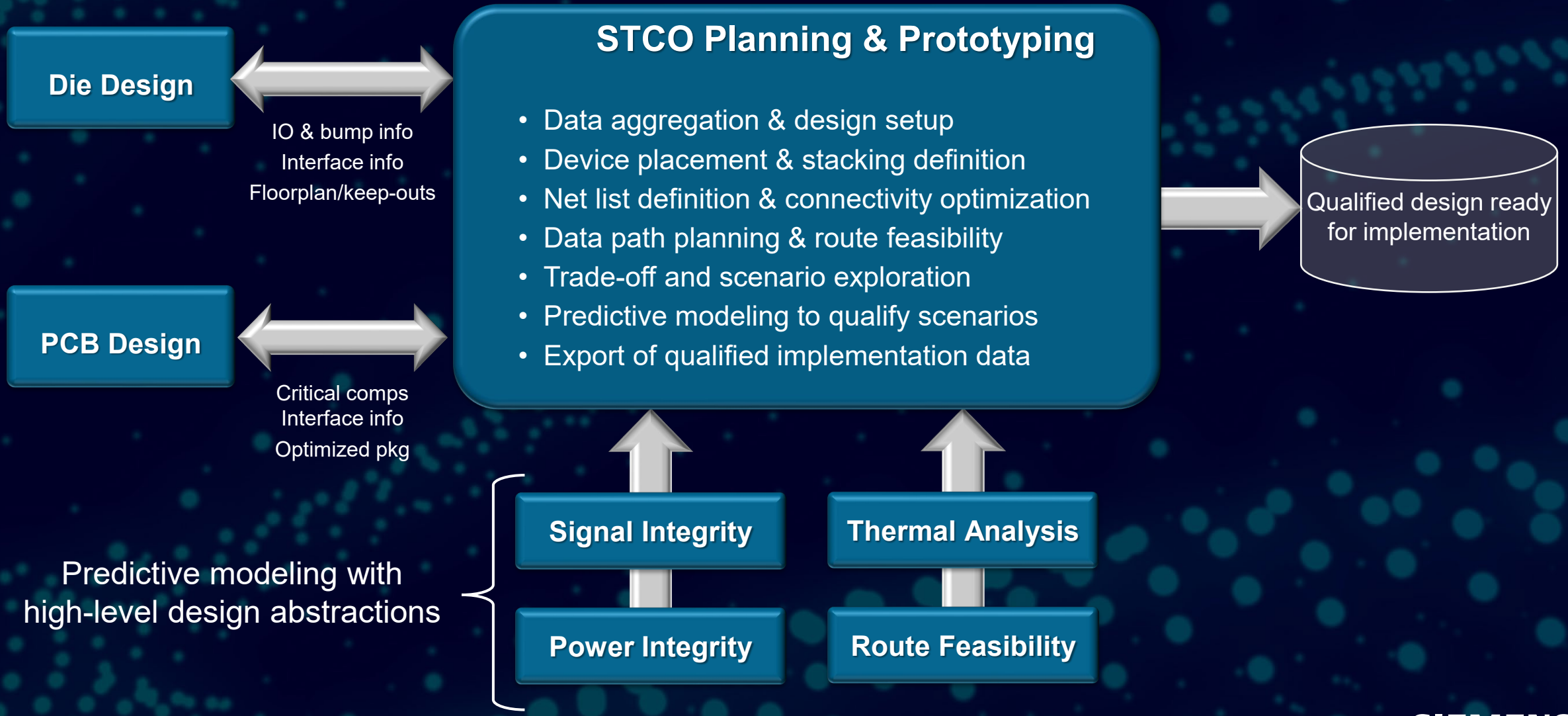
Planning and prototyping workflow



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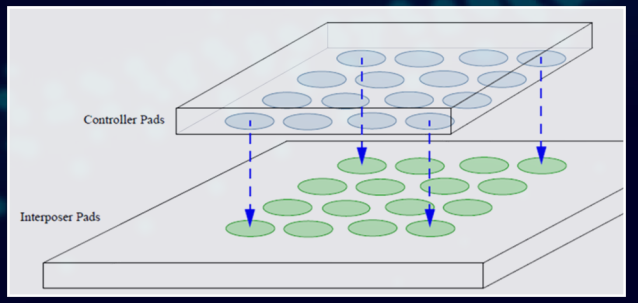
Verification at every level

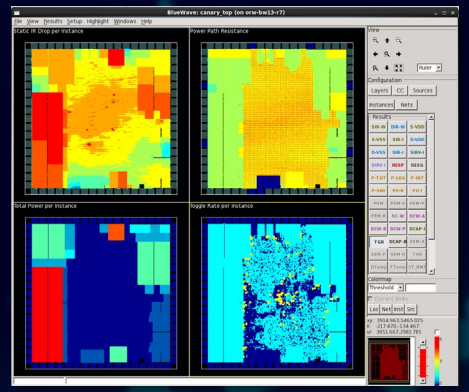
Needs

Substrate level fabrication DRC

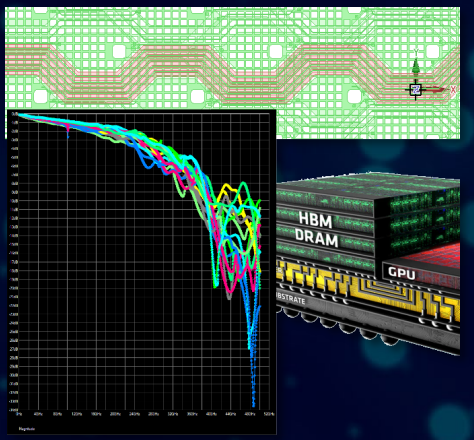
3D assembly level LVS



Predictive thermal, stress and reliability



Timing, signal and power integrity



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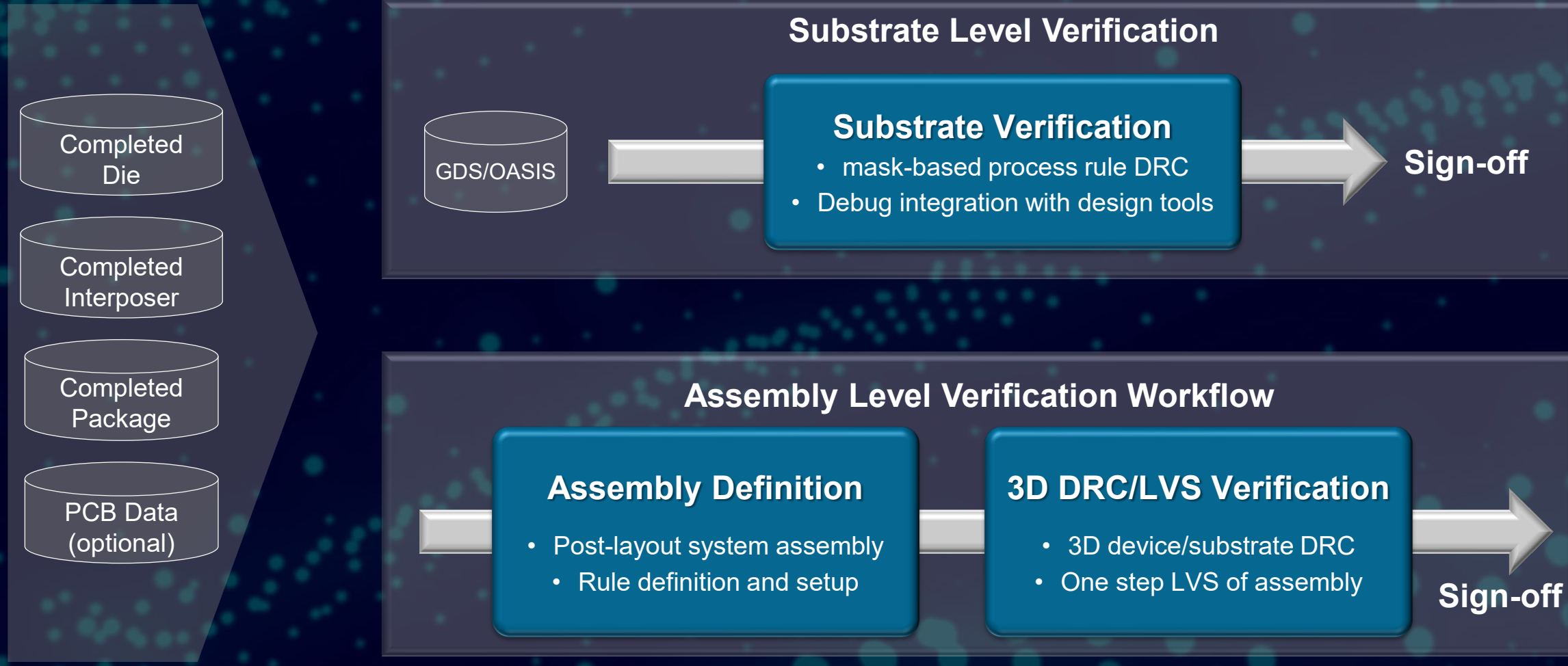
DRC/LVS verification workflows



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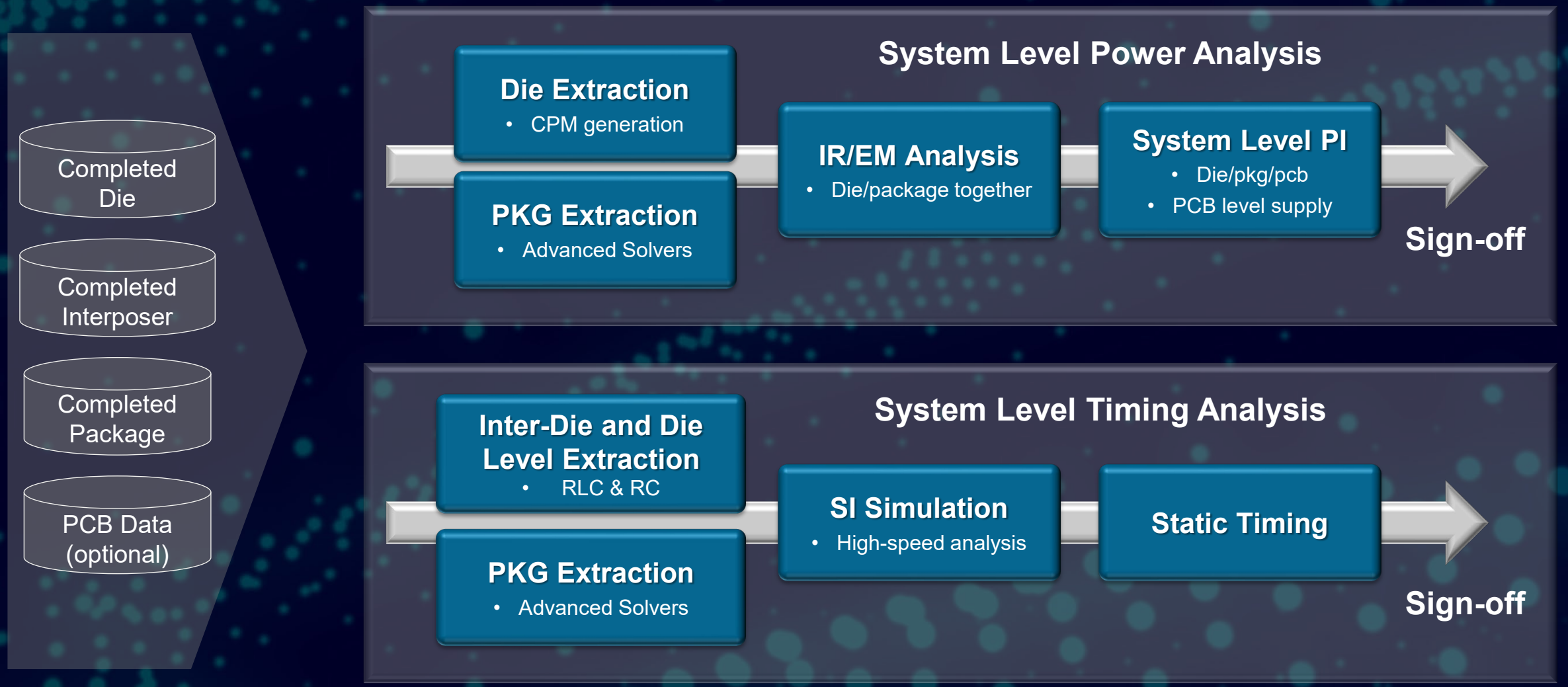
SI/PI Modeling workflows



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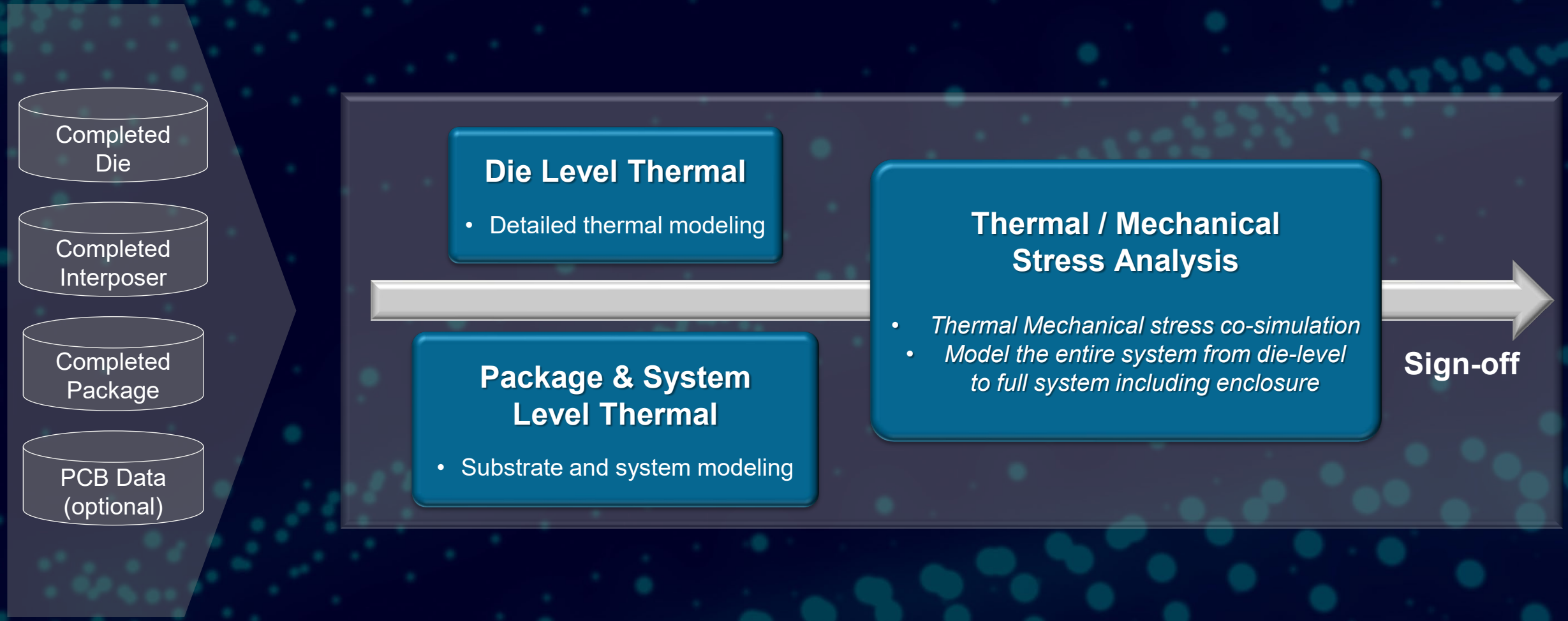
Thermal / stress workflow



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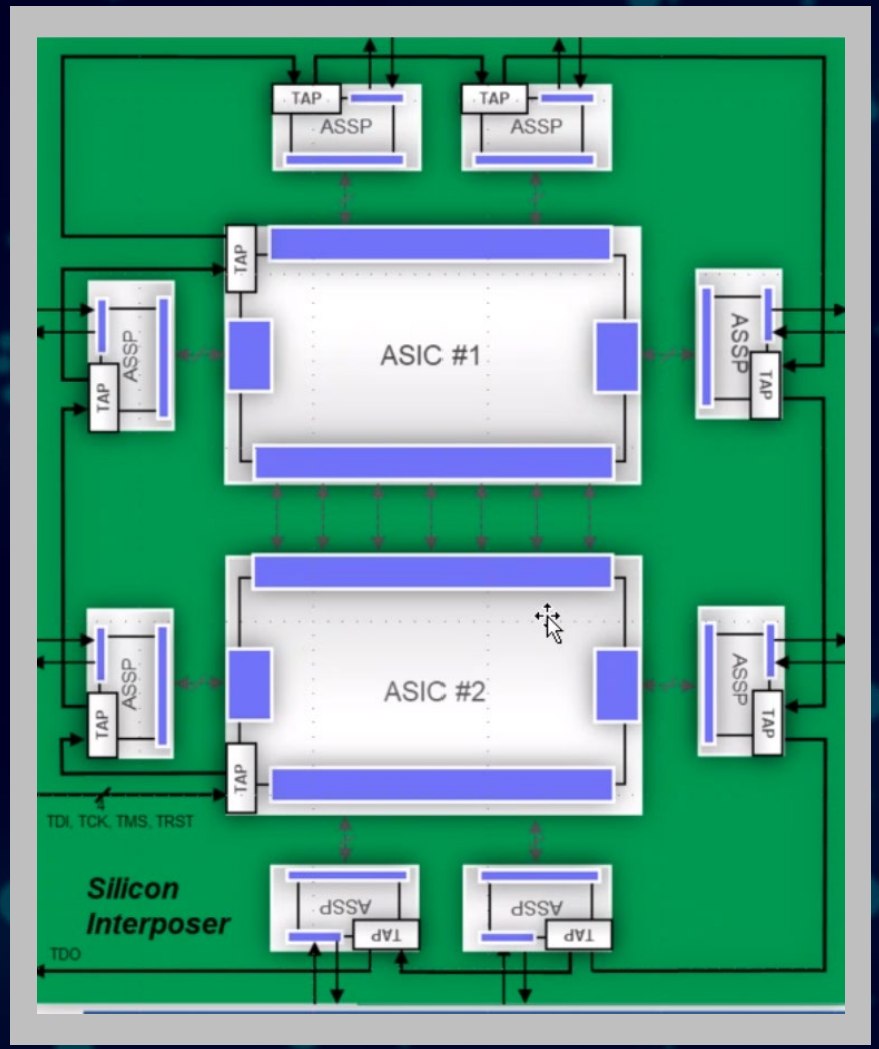
DFT/Test

Needs

- ASIC DFT Planning
- Interposer DFT Planning
- 2.5/3D Level Testing
- 2.5/3D DFT Verification



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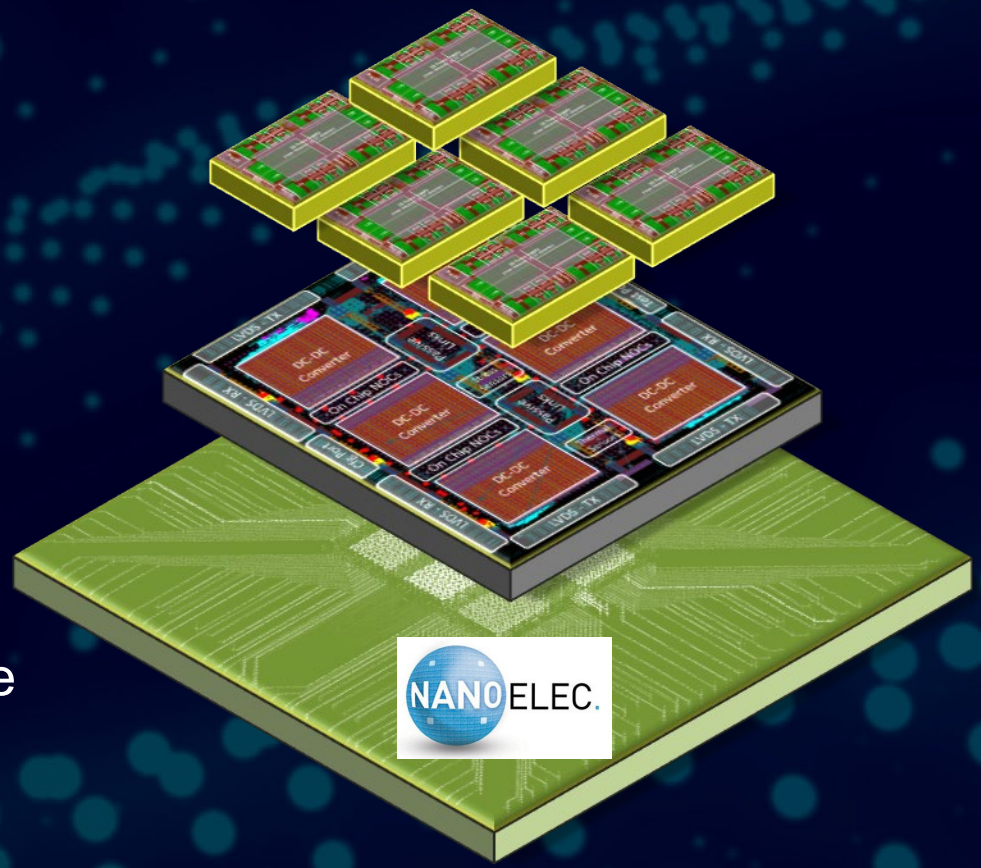
Summary

HI of chiplets using STCO enables compelling product benefits

- Increased Performance
- Reduced Power
- Lower unit cost/NRE
- Product configurabilty & hyper-scalability

General Comments & Observations

- Emerging chiplet Ecoysytem
- Assess HI scenarios early in the product design cycle
- Advanced HI package/ASIC STCO Flow
  - Multi Domain Design Planning, Analysis & Signoff
  - Predictive multi-domain analysis



Design images courtesy of CEA-Leti

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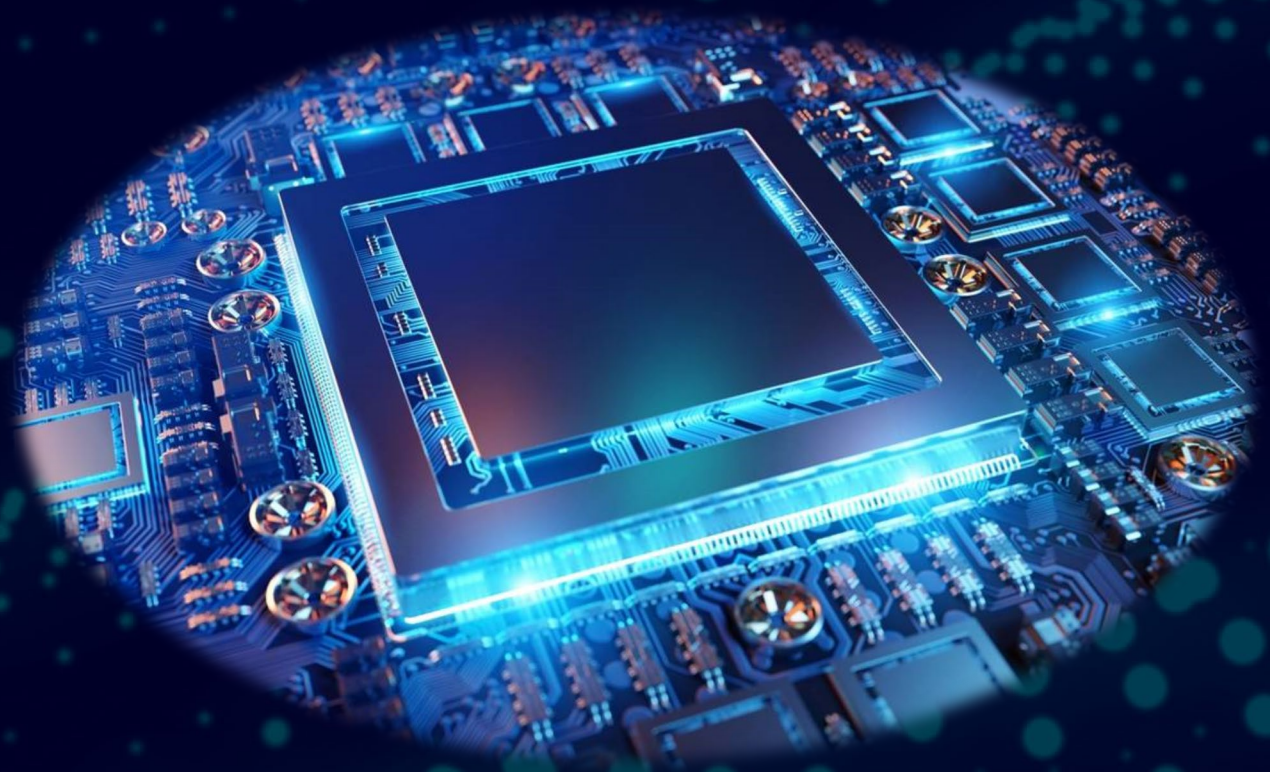
Thank You



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