Heterogeneous integration of chiplets

Lego-like IP for more than Moore

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the number of transistors on a microchip doubles every two years, though the cost of computers is halved. This so-called “Moore's Law” states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them. Another tenet of “Moore's Law” asserts that this growth is exponential.

Expert opinions see these observations ending in the 2020’s driven by:

1. Reticle limits
2. NRE costs
3. Availability of required IP
4. Yield
5. Die cost
6. Device scaling
7. Function aggregation
8. I/O scaling
Trends

Transistor Costs

7nm the pivot point?

Monolithic forces all functions to be at same node

Memory and I/O not ideal
Technology inflection point

Cost and yield driving alternatives to monolithic solutions
- SOC disaggregation into hard IP or “chiplets”
- Multi-die implementation to avoid reticle limitations (vs. single die)

Data movement - low latency, high-bandwidth
- Use of High Bandwidth Memory (HBM)
- 3D memory directly stacked on logic
- High-speed IO for chip-to-chip interfaces

Heterogeneous integration provides path forward
- Supports multiple micro-architecture scenarios
- Leveraging 2.5 and 3D assembly platforms
- Utilizes System Technology Co-optimization (STCO)
Extending “Moore’s Law”

Heterogeneous Integration
- Drives continued cost/function reduction
- Smaller form factors than 2D integration
- Higher bandwidth and lower power
- Design flexibility/scalability and IP reuse

- Structural and material advances
- Heterogeneous integration

Trends

Cost per Transistor

~7nm

Technology Node
Heterogenous Integration path forward

Enabling alternative Micro-architectures
High Bandwidth Memory (HBM)
ASIC Die Disaggregation
ASIC IP Disaggregation
2.5D Silicon Interposers, Fanout/RDL, Silicon Bridge
3D IC Stacked Die

Key Benefits
Increased Performance
Reduced Power
Lower unit cost/NRE
Product Configurability
Case study results

Trends

AMD Cost comparison of chiplets vs. monolithic
• 41% reduction in die cost and higher yield
• Maximize platform value – product configurability from single tape-out

Developing eco-system
• Standards for chiplet marketplace and exchange
• Turn-key design/build resources
• Materials suppliers

<table>
<thead>
<tr>
<th>Monolithic</th>
<th>Diff</th>
<th>Chiplet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Cost (7nm)</td>
<td>$9,350</td>
<td>1x</td>
</tr>
<tr>
<td>Total Die Size</td>
<td>600mm²</td>
<td>1.1x</td>
</tr>
<tr>
<td>Single Die Size</td>
<td>600mm²</td>
<td>1.1x</td>
</tr>
<tr>
<td>Gross Die per Wafer</td>
<td>96</td>
<td>1x</td>
</tr>
<tr>
<td>Defect Rate (per cm²)</td>
<td>0.2</td>
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<tr>
<td>Effective Area</td>
<td>80%</td>
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<tr>
<td>Estimated Yield (Dingwall)</td>
<td>43%</td>
<td>1x</td>
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<tr>
<td>Net Die per Wafer</td>
<td>42</td>
<td>1x</td>
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<tr>
<td>Single Die Cost</td>
<td>$224</td>
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<tr>
<td>Total Die Cost</td>
<td>$224</td>
<td>1x</td>
</tr>
<tr>
<td>Total Test Cost</td>
<td>$10</td>
<td>1.2x</td>
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<tr>
<td>Packaging and Packaging</td>
<td>$160</td>
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<tr>
<td>Packaging Loss</td>
<td>1%</td>
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<tr>
<td>Total Manufacturing Cost</td>
<td>$398</td>
<td>4x</td>
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</tbody>
</table>

Presented at 2021 International Solid State Circuits Conference
Chiplets

Enabling modular function design
• No need to own/design full stack
• Aggregated with custom ASIC(s)

Fabricated using ideal nodes

Integrated through standardized interfaces and CDK’s

Commercially available

Low NRE and fast TTM
Success with Chiplets

- Chiplet design kits
- Heterogeneous planning and co-optimization
- Physical verification at every level of 3D assembly
- Multi-domain testing
- Ecosystem interoperability
Standardized chiplet design kit

Needs

Open Domain
Specific Architecture

Machine readable models

Standards

Documentation

Security and Traceability Assurance

Chiplet Design Kit (CDK)

JEDEC
Global Standards for the Microelectronics Industry

IEEE
Advancing Technology for Humanity
Chiplet ecosystem enablers

Technology

Needs

Intellectual property

Workflows/design kits

Business models
Heterogeneous Planning & Prototyping

**Needs**

- Single digital twin and system logi netlist
- **System Technology Co-Optimization**
  - Predictive modeling to prototype and qualify design scenarios
  - Replacement of spreadsheet-based flows as communication mechanism of design intent

**System Technology Co-Optimization (STCO)**

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Planning and prototyping workflow

STCO Planning & Prototyping

- Data aggregation & design setup
- Device placement & stacking definition
- Net list definition & connectivity optimization
- Data path planning & route feasibility
- Trade-off and scenario exploration
- Predictive modeling to qualify scenarios
- Export of qualified implementation data

Qualified design ready for implementation

Die Design
- IO & bump info
- Interface info
- Floorplan/keep-outs

PCB Design
- Critical comps
- Interface info
- Optimized pkg

Predictive modeling with high-level design abstractions

Signal Integrity

Power Integrity

Thermal Analysis

Route Feasibility

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Verification at every level

- Substrate level fabrication DRC
- 3D assembly level LVS
- Predictive thermal, stress and reliability
- Timing, signal and power integrity
DRC/LVS verification workflows

**Substrate Level Verification**

- **Substrate Verification**
  - Mask-based process rule DRC
  - Debug integration with design tools
- **GDS/OASIS**
- **Sign-off**

**Assembly Level Verification Workflow**

- **Assembly Definition**
  - Post-layout system assembly
  - Rule definition and setup
- **3D DRC/LVS Verification**
  - 3D device/substrate DRC
  - One step LVS of assembly
- **Completed Die**
- **Completed Interposer**
- **Completed Package**
- **PCB Data (optional)**
- **Sign-off**
SI/PI Modeling workflows

Die Extraction
- CPM generation

PKG Extraction
- Advanced Solvers

System Level Power Analysis
- IR/EM Analysis
  - Die/package together

System Level PI
- Die/pkg/pcb
- PCB level supply

Sign-off

Inter-Die and Die Level Extraction
- RLC & RC

PKG Extraction
- Advanced Solvers

System Level Timing Analysis
- SI Simulation
  - High-speed analysis

Static Timing

Sign-off
Thermal / stress workflow

- **Die Level Thermal**
  - Detailed thermal modeling

- **Package & System Level Thermal**
  - Substrate and system modeling

- **Thermal / Mechanical Stress Analysis**
  - Thermal Mechanical stress co-simulation
  - Model the entire system from die-level to full system including enclosure

**Completed**
- Die
- Interposer
- Package
- PCB Data (optional)

**Sign-off**
DFT/Test

- ASIC DFT Planning
- Interposer DFT Planning
- 2.5/3D Level Testing
- 2.5/3D DFT Verification
Summary

HI of chiplets using STCO enables compelling product benefits

- Increased Performance
- Reduced Power
- Lower unit cost/NRE
- Product configurability & hyper-scalability

General Comments & Observations

- Emerging chiplet Ecoysystem
- Assess HI scenarios early in the product design cycle
- Advanced HI package/ASIC STCO Flow
  - Multi Domain Design Planning, Analysis & Signoff
  - Predictive multi-domain analysis

Design images courtesy of CEA-List
Thank You