Keys to Successful and Stable On-Shore Packaging and Advanced Packaging Defense Industrial Base

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Outline

• Introduction – MicroElectrics as Foundational Economic Driver
• USG Defense and National Security Considerations
• The New Paradigm
• Toolbox and Ecosystem Concept
• SkyWater Technology Role in Ecosystem
• Considerations and Keys for Successful On Shoring
Introduction

• Commercial Semiconductor Foundry background
• Career impacted by offshoring and global competition
• Almost but didn’t take alternative career path in different industry
• Opportunity to contribute as DOE NNSA Contractor supporting semiconductor products and components
• Mission impact and risk as result of off-shoring in supply chain, particularly packaging and advanced packaging
• Interest and focus grew as result of National Security Mission needs
• iMAPS events and association key to expanding knowledge
• Motivated to address on-shore Industrial Base Ecosystem
Introduction

• Microelectronics enabled a revolution in commercial products and services since they were introduced in the 1950s
• Initially created through USG investment and matured into a critical and dominant Global Commercial market
• Present-day industrial capabilities are key to the domestic economy as well as US military capabilities
• The U.S. is completely dependent on Microelectronics
• The critical role of Microelectronics has raised, to the highest level, the importance of U.S. access to a secure and reliable Microelectronics supply chain, including a strong industrial base for on-shore manufacturing
Introduction

The U.S. is completely dependent on Microelectronics

Automotive
Banking
Consumer

Industrial

But accounts for <12% of overall Semiconductor output
Introduction

Global Supply Chain
USG Defense and National Security Needs

Future Warfighting Needs

Dependency on Advanced Microelectronics Technology

- **Cyber & Quantum**
  - >1000x performance enhancement and efficiency for real-time ID/processing/response/security

- **Mesh Networked C3**
  - Open and distributed architecture to enable local processing of raw data on the battlefield
  - Adaptive processing for multi-antennas and frequencies for robust comm. and radar systems

- **Artificial Intelligence and Autonomy**
  - Need vision, semantic, and navigation processing for high-performance imagers and navigation

- **Directed Energy**
  - Advanced Imagers, optoelectronic technology, signal processing and control systems, spectral awareness

- **Space & Hypersonics**
  - Significant increases in rad-hard on-board sensor processing, communications, targeting, controls

Source: DoD Trusted and Assured Microelectronics Summary, Dr. Jeremy Muldavin, NDIA Electronics Division Annual Meeting, February 2019
USG Defense and National Security

Sustainment
New Paradigm

COVID - 19

Trade

‘China warns Taiwan independence 'means war' as US pledges support’ – BBC News 1/29/21

‘Russia could hit U.S. chip industry, White House warns’ – Rueters 2/11/22
Toolbox

Design
Interconnect
TSV
RDL
Micro Bump
CSP

Wafer Thin & Dice
Modification
Re-ball
Solder Dip
Lead Trim Form

Material Systems
Application
Environment
Digital RF Mixed
Fusion Sensors, Transceiver, Photonics
MCM SiP

AP HGI
Wafer Bond
Die-Die & Die-Wafer
3D

Assembly
SMT
2.5D Flip Chip
Underfill
Wire Bond

Packaging
Lead Frame, SiP
Over mold
BGA
QFP SERDIP ...

Test
Wafer probe
COTs Upscreen
Environmental
Reliability
SiP Test

AP
WLFO Integration

ITAR or Trusted Controls
Ecosystem

Industry and OGA Outreach

Security Solutions
- DARPA
- FVCS Research
- ARL Research
- mercury
- DRAPER

DIB- SHIP Partners
- BAE SYSTEMS
- LOCKHEED MARTIN
- Raytheon
- LITTELFUSE
- Northrop Grumman
- Boeing

Packaging Technologies
- mercury
- bridg
- micros
- skywater
- silicon wafer
- DECA

➢ Collaborate on security solutions and technologies:
  - Security requirements and gaps
  - Advanced packaging roadmap and future system needs
  - Feedback on platforms under development to support multiple programs
  - Access/Availability

Source: NDIA SOTA SHIP Awareness Day, Peter O’Donnel, NDIA Electronics Division, December 2021
Actively Extending Our Capabilities and Reach
SkyWater Florida Opened February 2021

Entry into Advanced Packaging Solutions

Location: Kissimmee, FL
Size: 109,000 sq ft total

- The first U.S. based advanced packaging pure-play service provider
- Site offers unique facility and process tooling to support 2.5D/3D system in package (SiP)
- Sensitive item workspaces and Fab, CAT1A Trusted Accreditation in progress
- Endeavor strategically leverages public private partnerships with BRIDG (non-profit), Osceola County, FL and the USG, as well as linking with higher education for workforce development and research
Actively Building Innovative Partnerships
Partnership with BRIDG to Develop Si-Interposers
Heterogeneous Integration & Advanced Packaging

Establishes a domestic silicon interposer capability for the industrial base

*BRIDG Industrial Base Analysis and Sustainment (IBAS) Program
SkyWater Si-Interposer

Phase I: Metallization buildup layers.

Phase 2: Via formation
Si-Interposer Assembly – BRIDG & SWFL

- Build Si-Interposer at SWFL.
- BRIDG and SWFL work with domestic supplier on first phase of assembly development.
- Generate reliability test data with NSWC Crane.
On Shore Hybrid Bonding W₂W, D₂W

Source: SUSS
Vision – On Shore Next Generation DECA WLFO for USG and DIB

Cu Pillar Flip Chip
(Flip chip on substrate)

TSMC InFO
(Chips first fan-out)

M-Series Gen 1
(Chips first fan-out)

EMIB
(Hybrid chips in substrate)

M-Series Gen 2
(Chips first fan-out)

Higher density bond pad pitch

Flip Chip Cu Pillar
Die pad pitch: 100 µm
IO per mm²: 105

TSMC InFO
Die pad pitch: 55 µm
IO per mm²: 314

Deca M-Series Gen 1
Die pad pitch: 45 µm (36 µm*)
IO per mm²: 492

Intel EMIB
Die pad pitch: 45 µm (36 µm*)
IO per mm²: 492 (806)

Deca M-Series Gen 2.1
Die pad pitch: 20 µm
IO per mm²: 2,518

M-Series Gen 2 delivers order-of-magnitude density increase

*https://www.anandtech.com/show/15980?cPage=s2&ali= Phần 36 và phần 806
Vision – **On Shore** Next Generation DECA WLFO for USG and DIB

**Gen 1**
- 2018 ➔
  - Codec
  - RF
  - IoT Device
  - PMIC
  - Dual PMIC

**Gen 1.5**
- 2021 ➔
  - 3D PoP - Mobile Applications Processor
  - Fan-out SoC – Advanced node silicon
  - Embedded Bridge Die Interposer – HBM intg

**Gen 2 (SkyWater Fl.)**
- 2022 ➔
  - 20 µm bond pad pitch
  - 2 µm lines & spaces
  - Up to 5 layers of RDL
  - Full frontside & backside routing
    - 3D PoP
    - Fan-out SoC
    - Embedded Bridge Die Interposer
    - Passive & Active Interposers

**Ultra-High Density (UHD) Integration**
- New lithography & AOI equipment
- Further material optimization for 5 µm vias
- New design rules supporting 2 µm RDL
- Adaptive metal fill for up to 5 layers of RDL

**Single-die**
- Protected fan-in
- Fan-out

**Multi-die**
- RF & IoT modules
- Integrated PMICs

**Passive & Active Interposers – CPU, GPU, AI**
- *Existing lithography & AOI equipment*
- Optimized direct & indirect materials
- Enhanced process flows for 3D integration
- New design rules supporting 3D
Capabilities for On Shore Advanced Integrations

Silicon Interposers w/TSV

Hybrid Bonding

Wafer Level and Fan-Out
Deca’s M-Series Gen 2

Solder Bumping & Assembly

2021 | | 2024
Considerations and Keys to Successful On Shoring

- Align USG Business and Funding practice with Commercial Industry
- Consolidate and forecast USG full lifecycle demand and technology needs to align with commercial industry planning cycles
- Be sensitive to the risks associated with political change, funding uncertainty, and shifting priorities
- Restrict USG contract awards to trusted and assured on-shore supply chains, inclusive of sub-tiers, when available
Considerations and Keys to Successful On Shoring

• Develop Data-driven models to show current and forecasted supply capacity and domestic demand, particularly from military, government, and semiconductor dependent industries

• Develop Baseline metrics to support accurate assessments of program-wide progress towards economic and security objectives and to highlight remaining gaps that may require other support
Considerations and Keys to Successful On Shoring

• Expand existing and develop new, pre-competitive Public-Private Partnership organizations in workforce development, R&D, design, fabrication, packaging, and test infrastructure involving both academia and industry (small and large)

• Fully leverage existing onshore assets and take better advantage of current infrastructure and workforce to optimize outcome

• Incentivize real long-term capabilities by industry beneficiaries as opposed to short-term financial manipulations
Considerations and Keys to Successful On Shoring

• Identify and prioritize assembly, advanced packaging, and test needs, gaps, and investments across the lifecycle

• Address the full semiconductor supply chain. The key US weaknesses are in fabrication, packaging, advanced packaging and testing. These areas should be the focus. It makes no sense to fabricate chips domestically just to package them overseas.

• Address more than SOTA only access. Current shortages are focused on the SOTP and Legacy that automotive, critical infrastructure and national security rely upon.
Considerations and Keys to Successful On Shoring

• Invest to develop the workforce required by collaborating with universities and colleges to modernize, update, or create new curricula to grow the talent pipeline needed for this effort.
Thank You!