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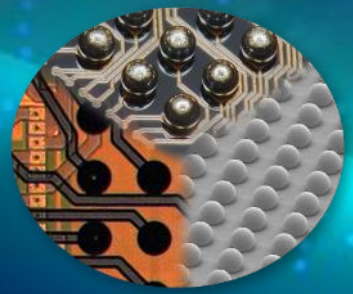

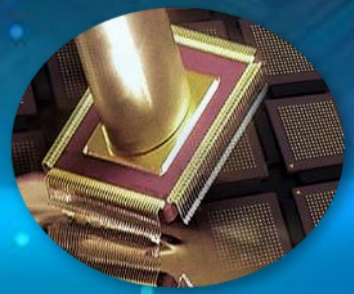
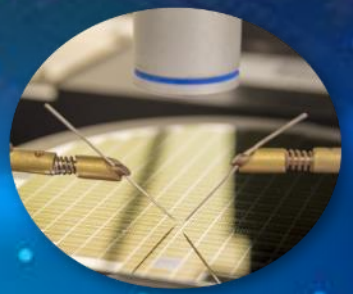
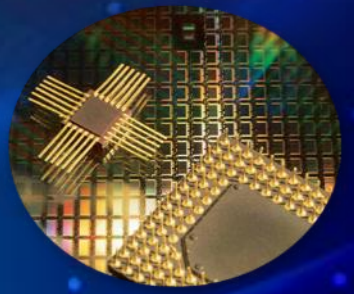

The Most Complete Provider of Advanced Microelectronic Services and Component, Die & Wafer Solutions

Domestic Advanced Packaging for Hi-Rel Microelectronics: The Future is Now

March 2022

Outline

- Introduction to Micross
- Direction of the Industry
- Realizing Advanced Packaging and Heterogeneous Integration Solutions
- Accessibility and Gaps
- It takes an ecosystem

Micross Overview

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Core Mission: To support customers' system-critical requirements through delivering Hi-Rel microelectronic solutions, assemblies, components and services on-time and to specification

- ***40+*** Years experience serving Aerospace, Defense, Subsea Oil & Gas, Space, Industrial & Medical Markets
- ***Unique 'One Source. One Solution' global turnkey solution***
- **Broadest** *Single-Source* provider of Hi-Reliability post-foundry services
- **Quality Accredited** *across all sites*
- PE owned – Yr2 with Behrman Capital

8 Global Operating Facilities; 2 International Sales Offices

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Worldwide Locations

550+ Employees

Component Modification

- **Manchester, NH**
  Robotic Hot Solder Dip
  Lead Attach/Trim & Form
- **Round Rock, TX**
  BGA Reballing
- **Crewe, UK**
- **Clearwater, FL**
  Counterfeit Detection / Test

Die Sales & Wafer Services

- **Orlando, FL**
  Die Sales, Wafer Probe & LATs
- **Norwich, UK**
  Die Sales, Wafer Probe & LATs

Assembly, Test & Products

- **Orlando, FL**
  QML Level Packaging & Products
- **Milpitas, CA**
  Test & Qualification
- **Raleigh, NC**
  Wafer Level Packaging & Advanced Interconnect
- **Norwich, UK**
  Packaging & Test

Rep Offices

- **Shanghai, China**
- **Bangalore, India**

Micross occupies a critical position in the US Microelectronics EcoSystem

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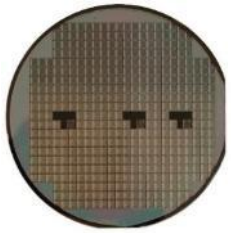


Device design and wafer from foundry

Incoming wafers from domestic (GF, Tower Jazz, On Semi, SkyWater) and international (GF, TSMC) foundries

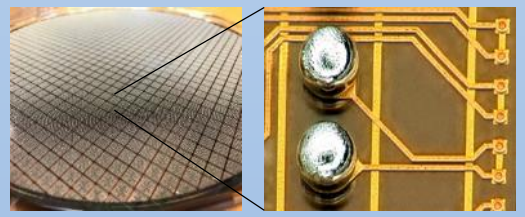
Micross STS & Hi-Rel

(Optional) Test

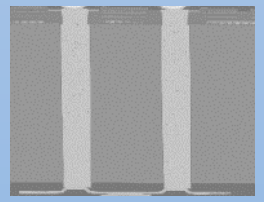
Micross AIT

Post CMOS Processing

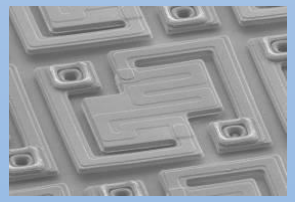
WLP



3DHI



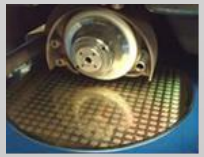
TSV insertion

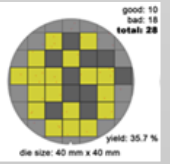


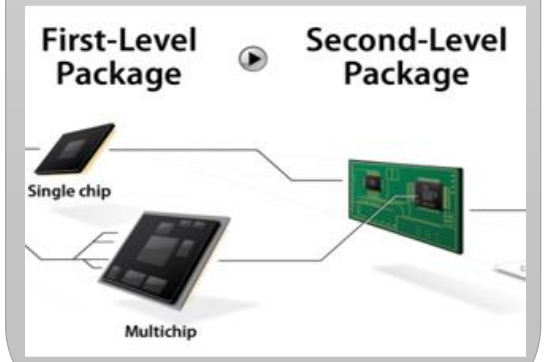
Monolithic Integration

Micross STS & Hi-Rel

Thinning/Dicing/Sort, Packaging & Test







Outgoing wafers can be shipped to the customer, or further processed at Micross STS or Hi-Rel components for dicing and subsequent die-level packaging

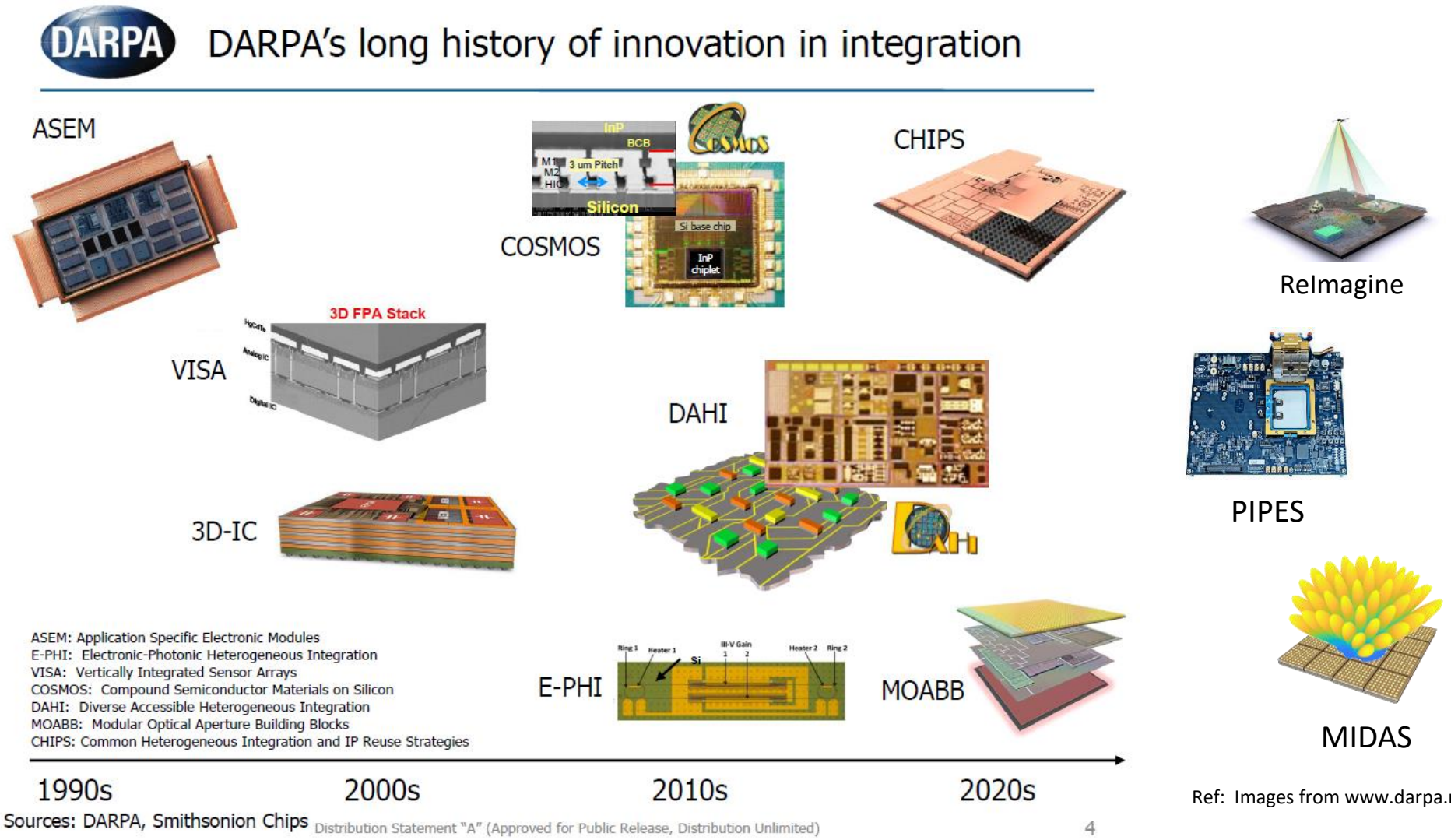
Micross AIT is the only domestic, secure, merchant supplier providing both WLP and 3DHI technologies (200mm and smaller wafer formats)

Direction of the Industry

- **Growing interest in and proliferation of heterogeneously integrated microsystems for enhanced performance of modules and microsystems**
  - Recent years have seen significant adoption of these technologies in commercial applications, driven by major fabless device companies and 1st-tier vertically integrated foundries & OSATs
    - Fabless: AMD, NVIDIA, Xilinx, Google, Marvell, etc.
    - Foundries & OSATs: TSMC, Intel, Samsung, Global Foundries, ASE, Amkor, etc.
  - 67% of semiconductor wafer production at > 40nm node (Mario Morales, IDC presentation at 2022 WLPS) → integration of legacy and leading edge device technologies to produce microsystems
    - Investment in legacy nodes lagging
    - Advanced Packaging a critical part of the future, but also lagging in investment

USG investment in HI technology

In parallel, there have been a number of U.S. government-supported programs (completed and ongoing) that focus on developing and implementing HI technologies



Ref: Images from www.darpa.mil

Ref: *Heterogeneous Integration at DARPA: Pathfinding and Progress in Assembly Approaches*, Dan Green & Jeff Demmin, ECTC 2018

Realizing HI Solutions

- **Key aspects to realizing an advanced packaging or HI solution**
  - Design
  - Availability of functional devices
  - Post CMOS processing
  - Fabrication/procurement of advanced substrates
  - Assembly
  - Test (electrical and reliability)

Realizing HI Solutions

- **Key aspects to realizing an advanced packaging or HI solution**
  - Design
    - Considerations
      - What will this microsystem do?
      - What devices will be required?
      - How will the devices be integrated? On what platform(s)? What off-chip interconnects are needed on the devices? Availability of devices with the required interconnect options?
      - What will the assembly process sequence be? Bottom up? Or other?
      - What are the performance metrics?
        - Electrical
        - Thermal
    - EDA Tools: EDA vendors developed(ing) tools for design and verification of 3D packages, but must be tied to packaging and assembly process guidelines (i.e. establishment of Assembly Design Kits) and tested through implementation -> iterative cycle to prove out EDA tools

Realizing HI Solutions

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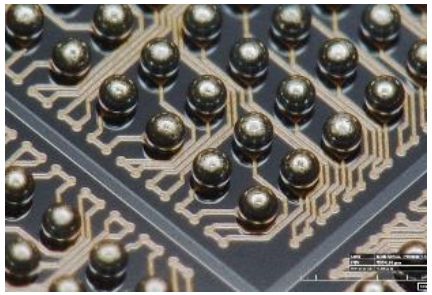
- **Key aspects to realizing an advanced packaging or HI solution**
  - Availability of functional devices
    - Acquiring devices in single die form with the desired physical interconnect (bumps) can be a challenge
      - Can you procure individual devices (chips) with reasonable cost and lead times?
      - Can you get the die with the right off-chip interconnect (bump) from the foundry? If no, you have 2 options:
        - Die processing at a post CMOS processing supplier – not necessarily trivial; depends on design requirement
        - Procure die in wafer format and use non-captive supplier for post CMOS processing
    - If HI solution includes 3D stacked die with TSVs, can devices be procured with blind vias present (requires post CMOS processing for wafer finishing) OR will TSV insertion be required (post CMOS processing)
    - Ultimately, which device functionalities are available from which vendors with the desired bump interconnect metallurgy or are available in an easily processed format for a post CMOS processing facility?

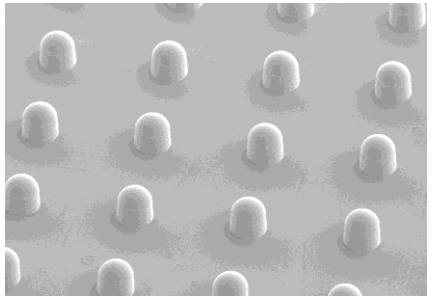
Micross offers turnkey solutions to help identify, procure, and process devices for HI applications

Realizing HI Solutions

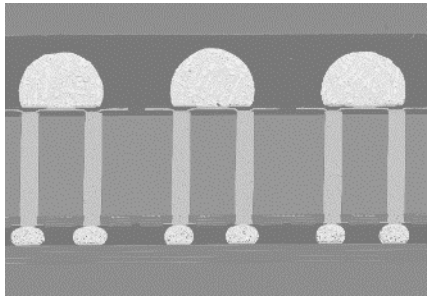
- **Key aspects to realizing an advanced packaging or HI solution**
  - Post CMOS processing is driven by unavailability of devices with the required interconnect options OR the need for wafer finishing for integration compatibility
    - Extending typical wafer bumping to processing of **individual die** is possible, but not always efficient, or feasible for all bump types. Some options are:
      - Electroless UBM deposition
      - Solder bump jetting
      - Fan-in processing of die on RCW
    - # of I/Os and real estate limitations on the integration platform (substrate/interposer) generally require solder or Cu pillar interconnects, which are generally performed on full wafers
    - If **full wafers** are available, state of the art C4, Cu pillar, microbumping (sub-20 um pitch), and DBI processes are standard offerings. Repassivation and redistribution layers can be included in the wafer bumping sequence.
      - Not all post CMOS processing suppliers offer Pb-based solder solutions due to RoHS regulations
      - Not all post CMOS processing suppliers offer flexibility in UBM and bump stacks needed for Hi-Rel applications.
    - TSV insertion and wafer finishing require full wafer processing and require thinning of the device die.



C4



Cu Pillar

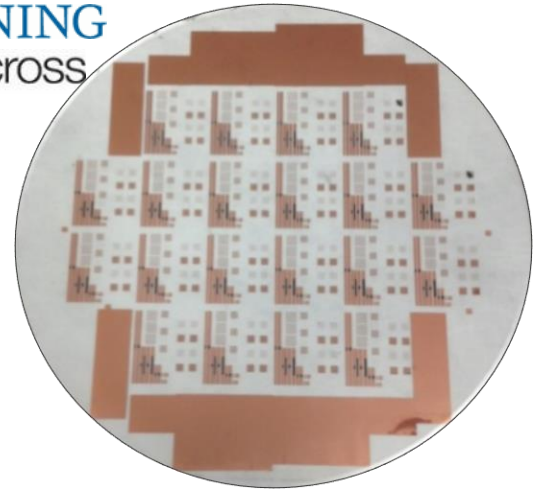


TSV Insertion

Realizing HI Solutions

- **Key aspects to realizing an advanced packaging or HI solution**
  - Fabrication/procurement of advanced substrates
    - If a Si (or glass) interposer is going to be used for the package, what options are available?
      - Procurement of Si interposers from commercial providers (i.e foundries) is possible, though typically limited to top-tier customers and higher volume engagements
      - Options for low volume or developmental applications are more limited and may require managing an ecosystem of providers to fabricate the interposer (design for manufacturing, multilayer routing, TSV insertion, interconnect structures, singulation)
        - Glass interposers currently fall into this category, but options for foundry-like MLM are more limited than Si
    - If an advanced substrate is going to be used for the package, what options are available?
      - Organic laminate – only one domestic supplier/manufacturer
      - Ceramic – currently long lead times

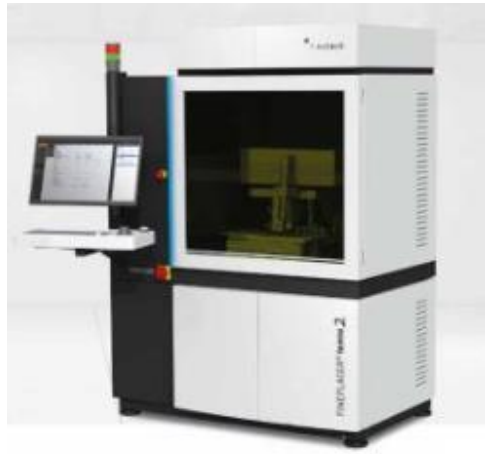
CORNING micross



Micross has established relationship with domestic, industry-leading design firm that can translate Si interposer system design requirements into wafer fabrication flows/designs for processing at domestic foundry partners to produce multilayer BEOL high density routing, with Micross executing TSV, wafer finishing, and singulation portions of the flow

Realizing HI Solutions

- **Key aspects to realizing an advanced packaging or HI solution**
  - HI Assemblies require unique capabilities when compared to typical WLP assembly operations
    - High accuracy bonder/assembly systems are needed to deal with high I/O density devices (i.e. 55um and smaller Cu pillar arrays) and components that may have varying types of bump interconnects with different assembly process requirements (C4 solder bumps, Cu pillar bumps, Au bumps for thermocompression bonding).
    - Handling thin devices is challenging and requires careful consideration of singulation, shipping containers, and die handling capabilities of the assembly tool
    - Depending on where bump interconnects are on the various components, the optimal order of assembling the components may need to be evaluated to achieve the most efficient process and best yield.
    - Pre or post-assembly application of underfills may require new materials and/or non-standard deposition methods when components are large in size, in close proximity to each other, or have high bump densities.
  - Assembly methodologies and options MUST be considered from the outset of the project and not left until later! "Bottom-up" approach is generally preferred, if possible.



Femto 2 Sub-Micron Bonder

Micross has extensive capability in standard packaging and assembly, as we all as high accuracy bonding/assembly

Realizing HI Solutions

- **Key aspects to realizing an advanced packaging or HI solution**
  - Functionality Test
    - KGD determination is a must for device; ideally this means probing bumped wafers
    - Interposer testing?
      - Through test structures on the wafers?
      - Direct testing of routing metal layers?
    - Base substrate testing – more straightforward for organic substrates
    - Final assembled module testing – need to develop test architecture, including socket or interface, test protocols and programs (custom for each module)
  - Reliability Test
    - Thermal cycling, high temp storage, HAST, THB, shock & vibe, radiation? - depends on application

Micross has both standard and advanced test solutions for both electrical and environmental testing

Accessibility

- **Volume of business may limit your accessibility to devices and form factors (die vs wafer) available from IDM's or foundries focused on HVM markets**
  - Similar reality if trying to engage large OSATs for post CMOS processing
- **Decreasing # of post CMOS processing providers offering Pb-based interconnects, required for Hi-Rel electronics**
- **Very few post CMOS processing providers with both wafer bumping and TSV capabilities – only one domestic, merchant supplier**
- **ITAR or Trusted constraints can limit your options in most aspects of realizing an HI solution as majority of the device foundries and all of the commercial OSATs migrated off-shore 20 or more years ago**

Micross can leverage IDM relationships and/or internal capability to help

Domestic Gaps

- **No credible, secure, on-shore merchant supplier of 300mm wafer bumping with Pb-based solder interconnects for Hi-Rel electronics**
- **TSV's available in limited # of nodes (mostly advanced nodes and costly) from foundries**
  - Advanced nodes mostly in 300mm format → requires 300mm wafer finishing for device integration (thinning, WLP)
  - Smaller wafer formats serviced through combination of domestic suppliers (ecosystem)
  - From security standpoint, ideal if supplier had all wafer finishing capabilities under one roof/company
- **TSV insertion in CMOS OR for Si interposer**
  - Limited # of domestic providers with TSV fabrication experience – higher MRL needed
- **Availability of Si interposers**
  - Need to develop domestic ecosystem (design, front end foundry, back-end foundry, assembly, and test) for access by domestic companies and emerging technology markets
- **Vetted EDA tools for 3DHI packages**
- **Domestic FOWLP infrastructure**

It takes an Ecosystem

- **The demand for lower SWAP through Advanced Packaging and HI solutions is only going to grow**
- **To enable current and emerging technology markets to explore/realize the benefits of an Advanced Packaging or HI solution, every key aspect must be readily available at a high MRL**
  - Requires investments in domestic Advanced Packaging and 3DHI infrastructure/tools
- **No one entity can do all of it**
  - Requires USG, key stakeholders (emerging technology companies, DIB), and the domestic advanced packaging supply chain working together
  - Key know-how and technical capability exists on-shore – fill the gaps, by leveraging strengths of existing suppliers
- **To realize the power of an integrated future, the time to engage and act is now!**

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