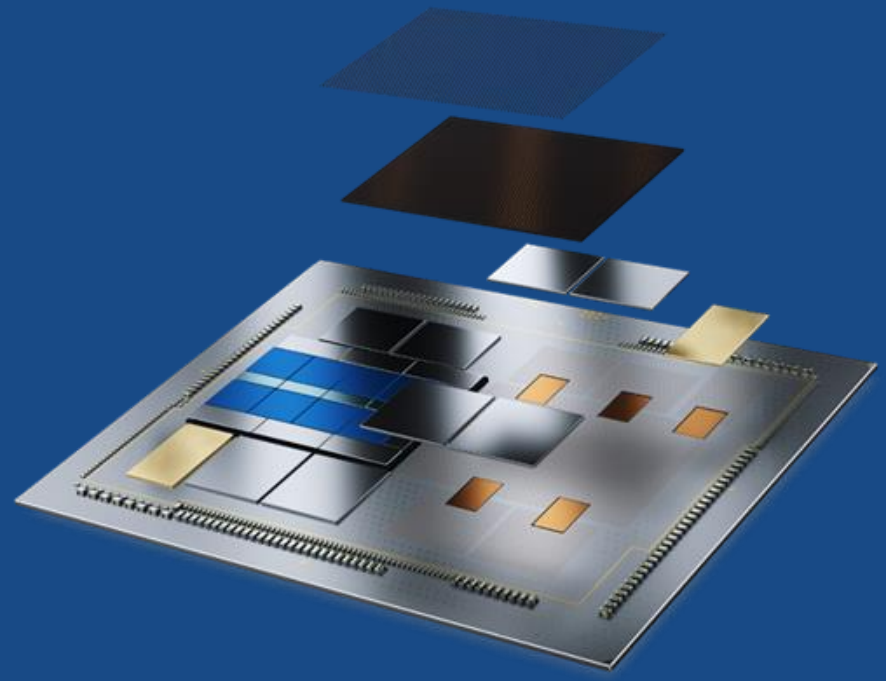
Advanced Packaging Capabilities at Intel

IMAPS Conference

March 2022



intel®

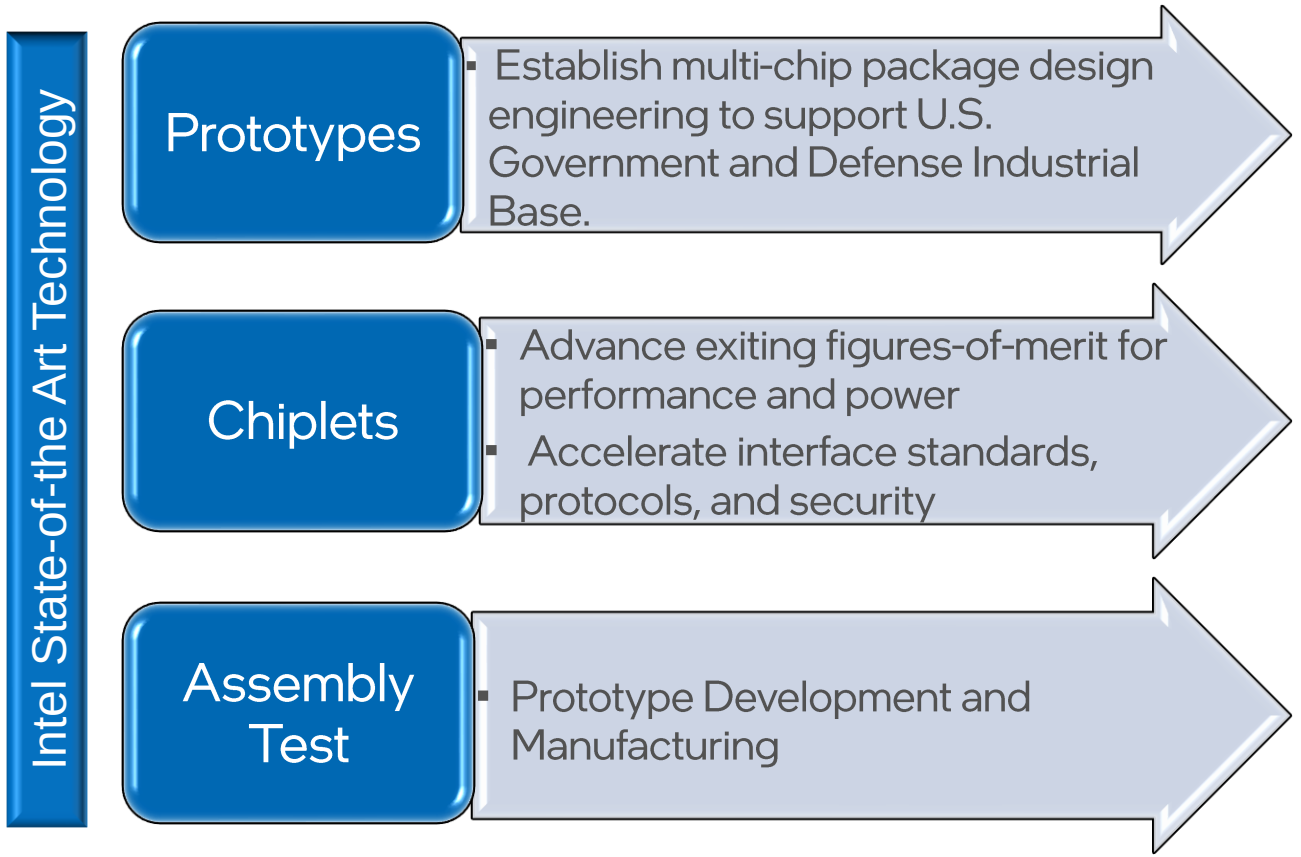
Executive summary

- Heterogeneous Integration (HI) is undeniably the vehicle to drive continued advances in Compute and Communications
- Advanced Packaging Architectures today provide unprecedented levels of Heterogeneous Integration in Client, Server and Discrete Graphics
- Intel committed to a **vision of developing heterogeneously integrated leadership products** using **advanced packaging technologies** to **match the functionality of a monolithic SOC** and more…..
- We continue to scale our Advanced Packaging Technologies Roadmap
- Federal Engagements in multiple programs (e.g. SHIP) allowing Intel to drive design and prototype diverse configurations for U.S. Government / and Defense Industrial Base; USG/DIB partnering critical for HI advancements

Supporting the U.S. Government

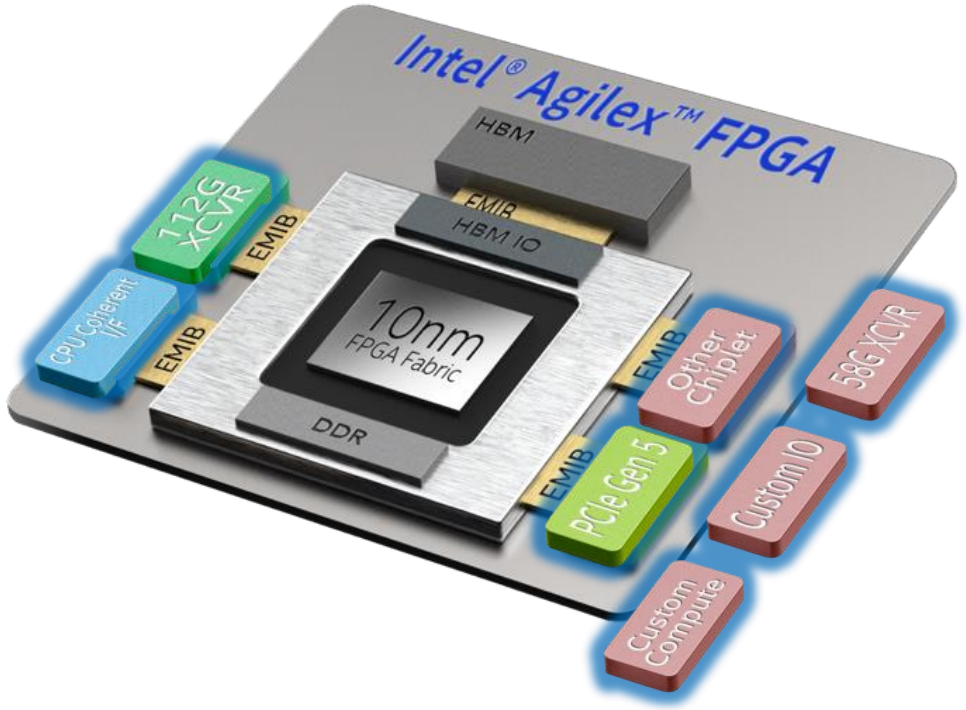
The U.S. Department of Defense has awarded Intel Federal LLC the second phase of its State-of-the-Art Heterogeneous Integration Prototype (SHIP) program. The SHIP program enables the U.S. government to access Intel's state-of-the-art semiconductor packaging capabilities…

… the program will develop prototypes of multichip packages and accelerate advancement of interface standards, protocols and security for heterogeneous systems.



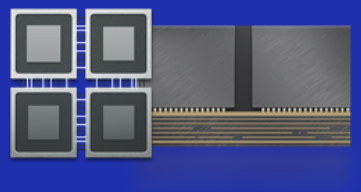
Creating Ecosystem of Tiles/Chiplets

- Implement custom & changing functionality
  - Interfaces & Evolving Standards
  - ADCS / DACs
  - Analog, RF
  - Fixed Function Digital (Processors / Accelerators)
  - Optical Interfaces
- FW/SW development support Chiplet integration for MCP's
  - Interface support (AIB 1.0/2.0/AXI)
  - Enables novel Chiplet Integ. through std. interfaces



Continued leadership in advanced packaging

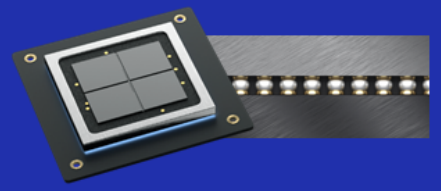
Embedded Multi-die Interconnect (EMIB)



bump pitch ≤ **55 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

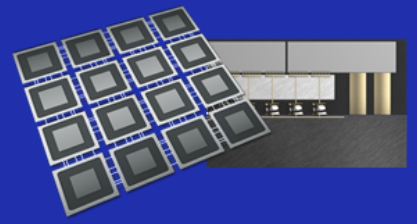
Foveros Technology



bump pitch **50-36 microns**

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

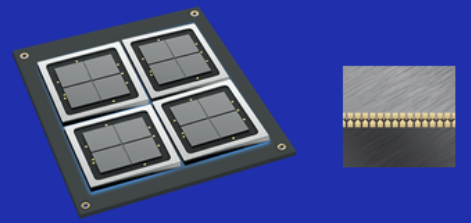
Foveros Omni



bump pitch **~25 microns**

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

Foveros Direct

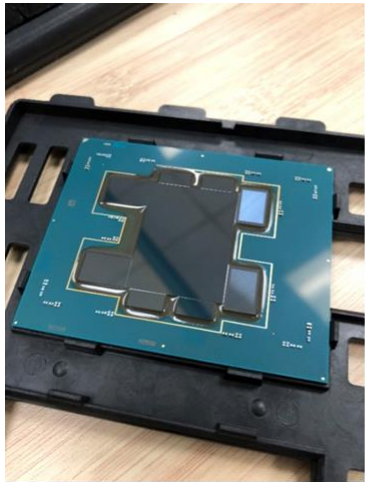


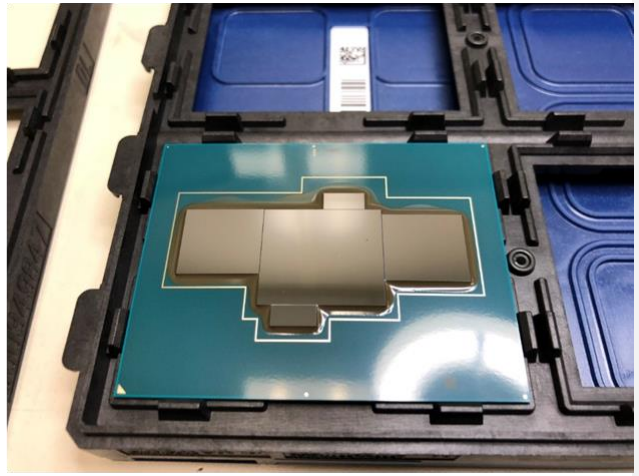
bump pitch **< 10 microns**

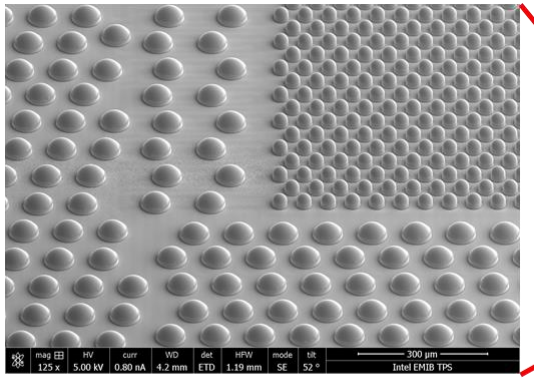
- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins

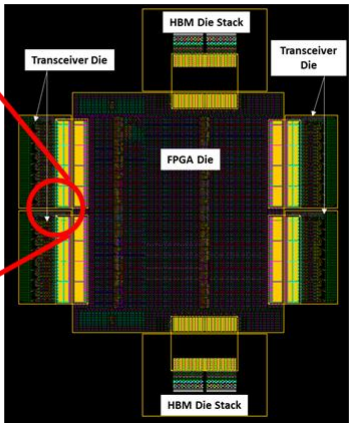
EMIB Embedded **M**ulti-Die **I**nterconnect **B**ridge

- Localized high-density wiring
- Multiple Bridges, Multiple Bridge Sizes and Bridge Technologies
- Bridge Mix and Match → Enhanced Design Flexibility
- Bridge silicon costs < Silicon interposer
  - No TSVs, Significantly less silicon area
- Die from Different Foundries
- Large Overall Die Area enabled

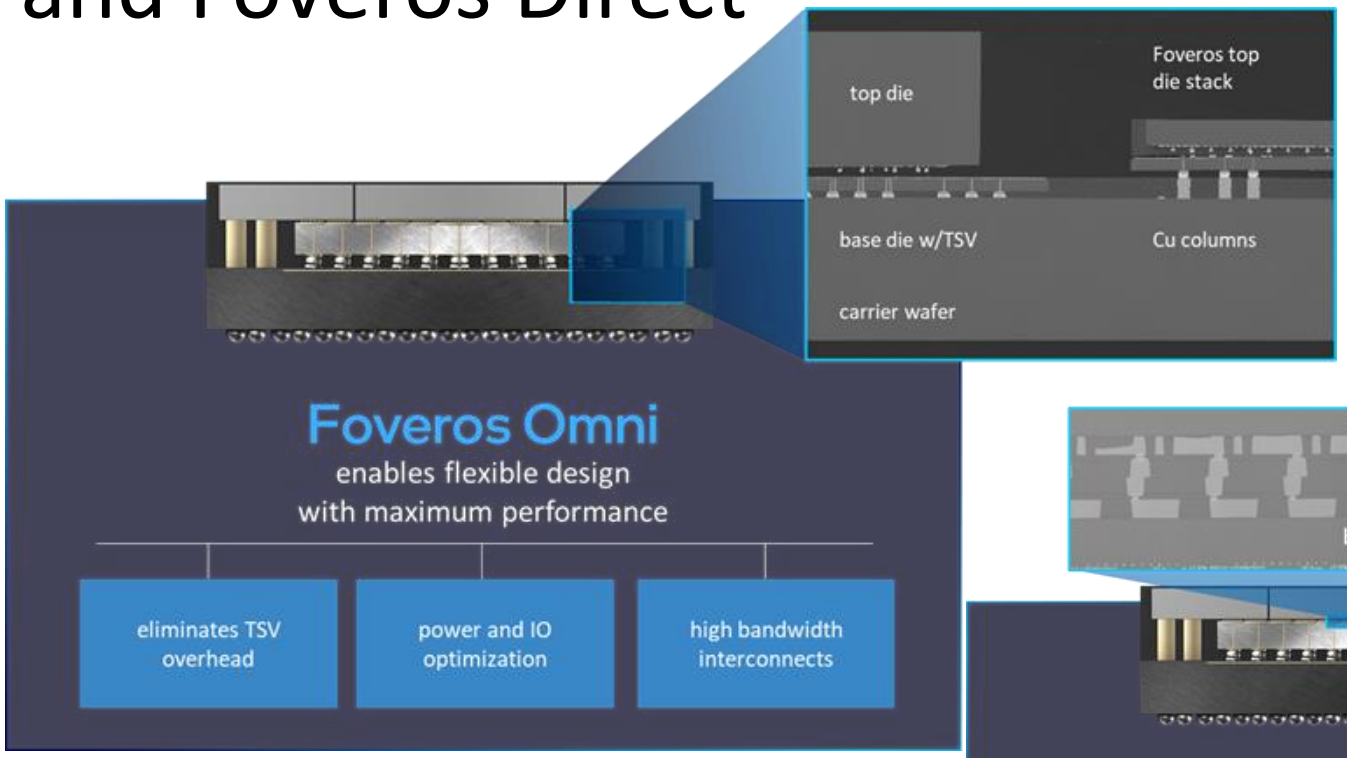




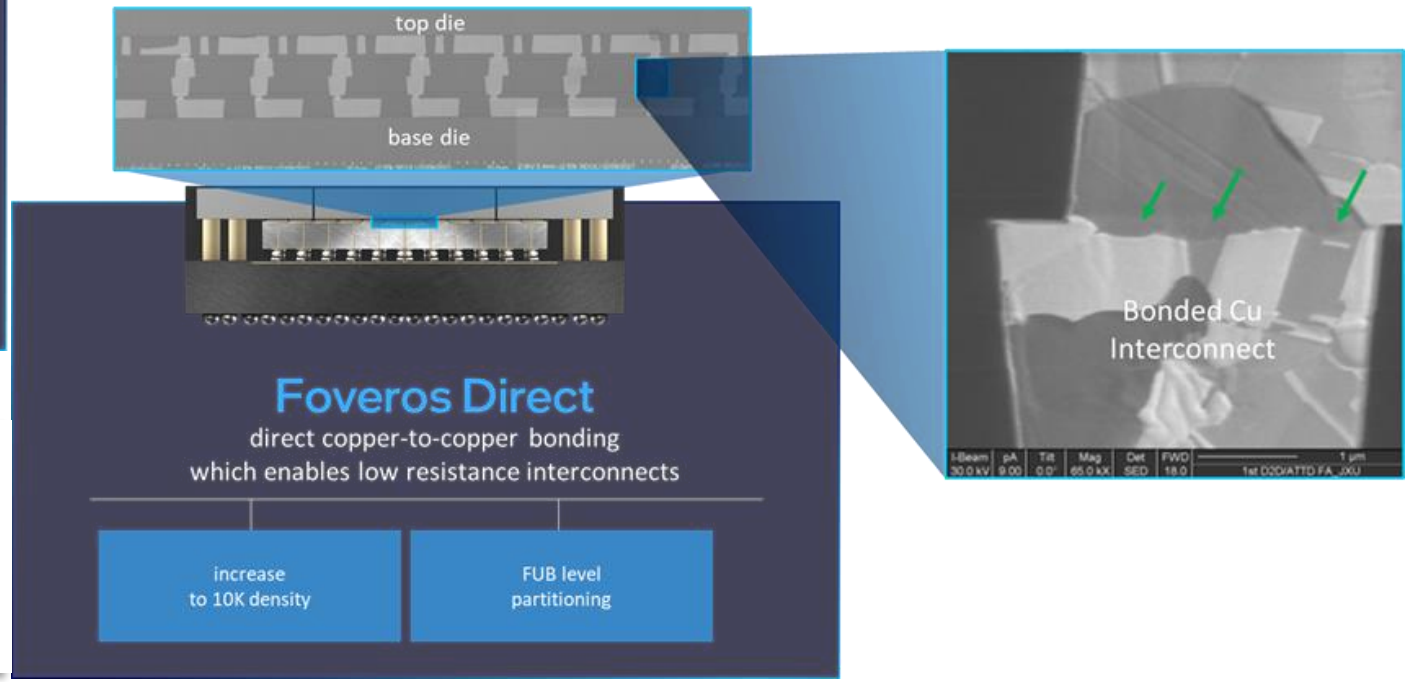




Packaging Innovations In The Near Future: Foveros Omni and Foveros Direct

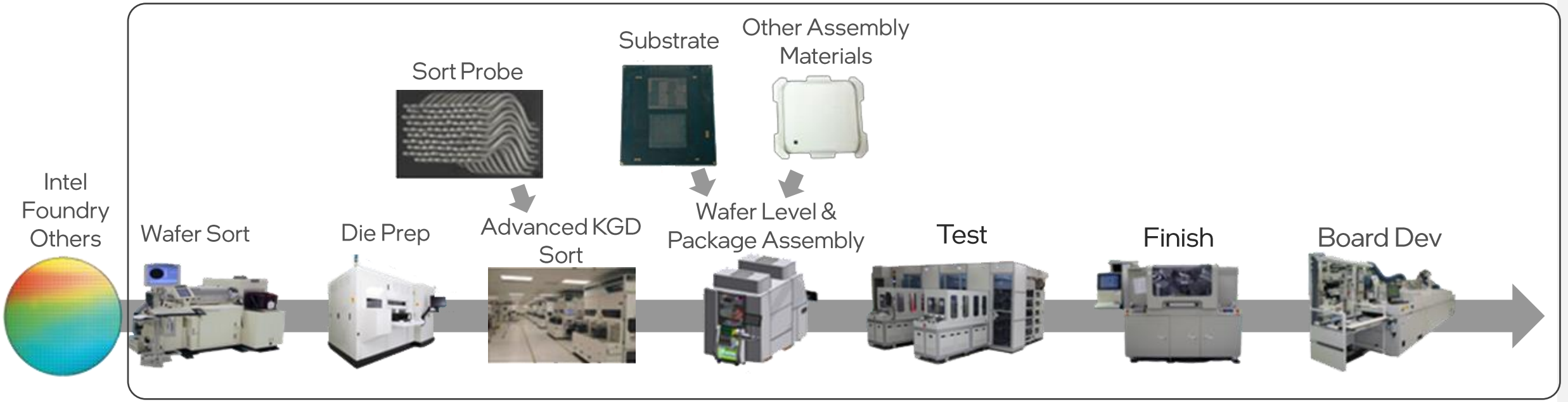


- Rich Interconnect Portfolio allows greater mix-and-match and better/independent interconnect optimization for Power and IO



- Continued Pitch Scaling increases in IO/mm^2

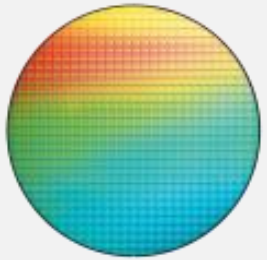
INTEL TECHNOLOGY DEVELOPMENT CAPABILITY



RnD and Development Factories

- Sort
- Substrate
- Assembly
- Test
- DP/Wafer Assembly

INTEL TECHNOLOGY DEVELOPMENT CAPABILITY



SORT

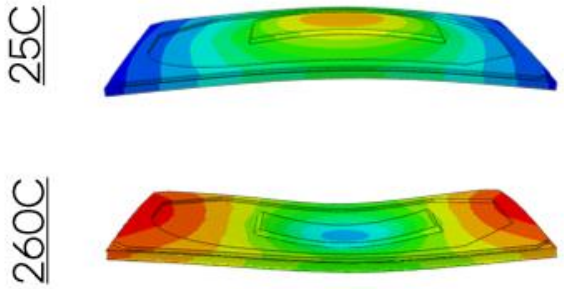
ASSEMBLY

TEST

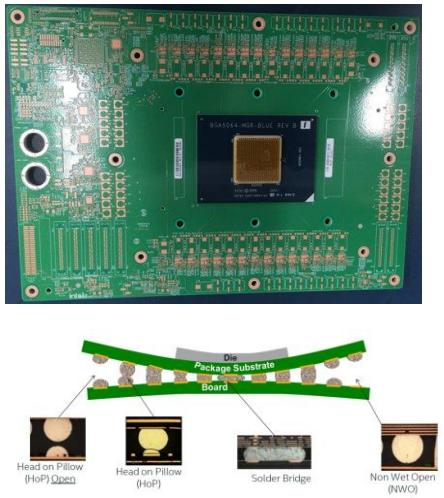
FINISH

PATHFINDING	DEVELOPMENT	HIGH VOLUME MANUFACTURING
Modeling & Simulation *(Electrical, Mech, Performance, Yield, etc.)*	Achieve Reliability & Yield Targets on POR Process	Transfer and Ramp in Factory Network
Demonstrate Proof of Concept	Validate Performance	
Cost Modeling & Manufacturability	Support Product Engineering Samples	
	Limited Volume Ramp	

Board Assembly: Manufacturing Capability & Support



Component Room & High Temp warpage modeling and manufacturing risk assessment



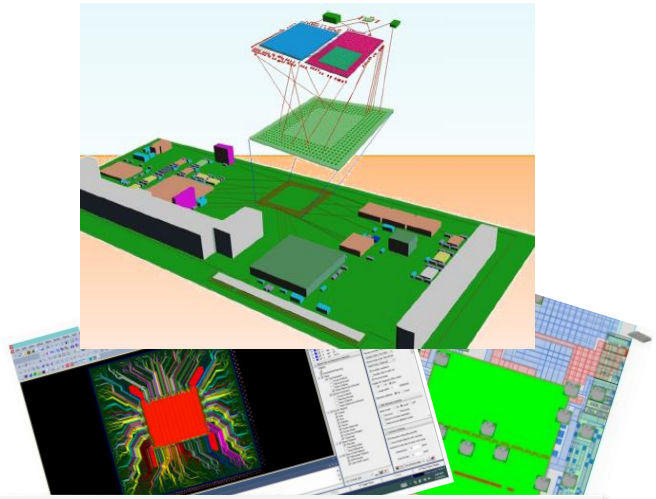
SMT Process optimization for high-risk devices at Intel

Intel provides manufacturing recipe to customer/ODM

Direct on call factory startup support

DESIGN TO MANUFACTURE

PRODUCT LIFE CYCLE MANAGEMENT



CO-DESIGN TOOLS & FLOWS

PATHFINDING

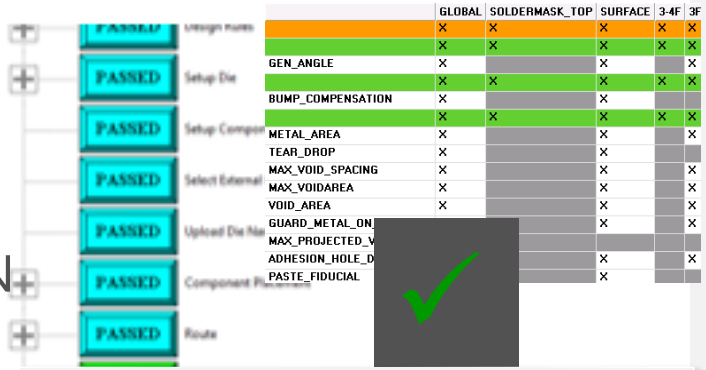
DEVELOPMENT

DESIGN EXECUTION

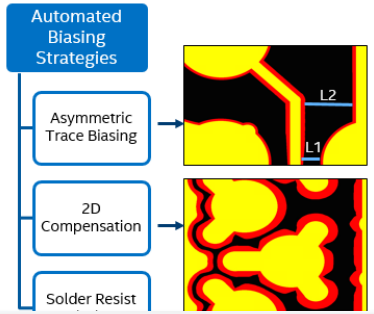
SUPPLIER TAPEOUT

HVM

Design for Performance, Quality, Affordability, & Efficiency

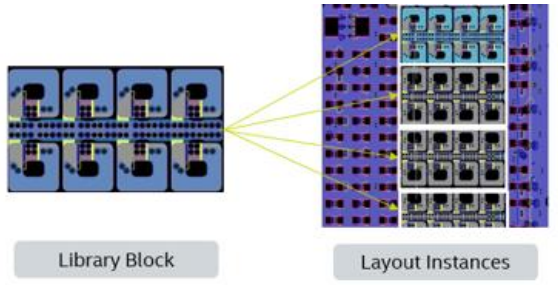


DESIGN RULE AUTOMATED CHECKING



DATA AUTOMATION

PRODUCT PREDICTABILITY AND PERFORMANCE ENHANCEMENT



LIBRARY BLOCKS FOR DESIGN EFFICIENCY

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