STATE OF THE ART (SOTA) HETEROGENEOUS INTEGRATED PACKAGING (SHIP) PROGRAM

Trusted and Assured Microelectronics

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DoD - Microelectronics Modernization

The 2018 DoD National Defense Strategy (NDS) highlights **Building a More Lethal Force** through Modernization of Key Capabilities as one of the tenets in the strategic approach. Microelectronics has been highlighted as a key focus area for DoDs Modernization.

Key Capability Areas Include:

Hypersonics, Artificial Intelligence, Microelectronics/5G, Cyber, Advanced DoD's digital modernization efforts to enhance IT architecture through cloud; AI; command, control, and communications; and cybersecurity to name a few.

All of which are steeped in microelectronics.

DoD OUSD (R&E) Modernization:

To rapidly address the development of these technologies, the Trusted and Assured Microelectronics (T&AM) Program is executing the development of key technologies in accordance with a roadmap focusing on 6 different Technical Execution Areas (TEA).

T&AM Program Overview

Description: The T&AM Program was established by the Defense Department to drive rapid modernization of defense systems through access to advanced microelectronics technologies by leveraging commercial industry capabilities

Objective:

- Support microelectronics modernization
- Keep pace with commercial microelectronics technological advances
- Mitigate persistent threats to the microelectronics lifecycle
- Reduce reliance on obsolete microelectronics
- Alleviate the Department's reliance on sole source foundries for assured SOTA microelectronics

Issues:

- DoD has very limited access to leading edge commercial CMOS ecosystem/ infrastructure
- Threats global microelectronics supply chain
- Requires increased sources of radiation hardened, radio frequency, and optoelectronic components
- Requires a more robust domestic and allied microelectronics ecosystem to rapidly and securely mature emerging advanced technology

Challenges:

1) Access to modern manufacturing processes that require commercial volumes to maintain long term viability
2) Protecting the intellectual property (IP) and verifying the integrity of the microelectronic parts

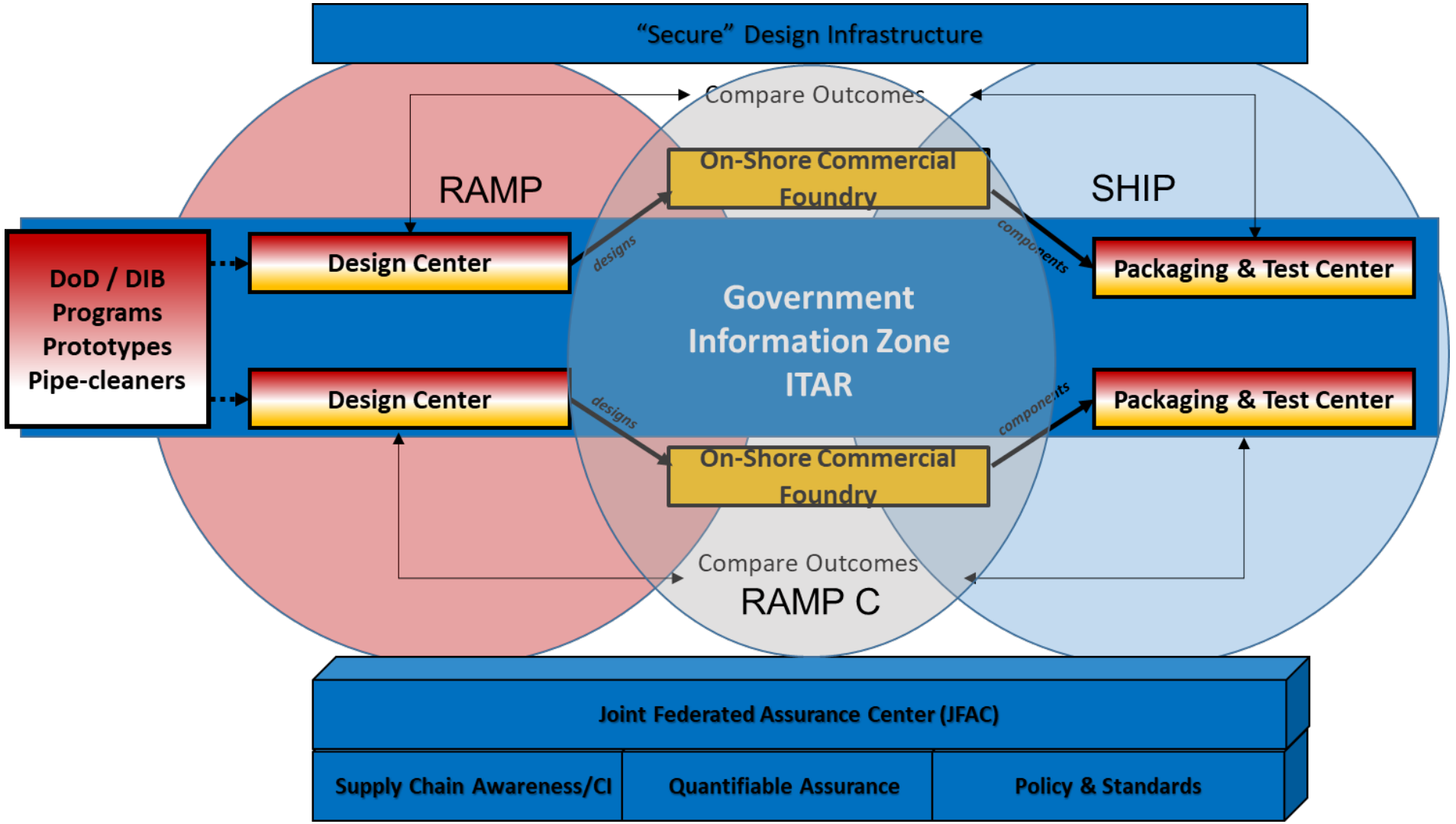
T&AM - Strategy & Objectives

- **Strategy:** Provide the U.S. warfighter with the State-of-the-Art (SOTA), assured microelectronics (ME) required to meet DoD system modernization goals.

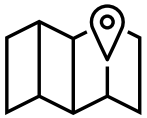
- **Objectives:**
  - **Drive for a U.S. located capability**
  - Leverage SOTA commercially-driven technology to obtain the best available technology
  - Use the Quantifiable Assurance zero-trust based method to assure the DoD supply chain
  - Quantifiable Assurance applicable across the microelectronics supply chain
  - Quantifiable Assurance applicable to Legacy and SOTA technology
  - Address the entire microelectronics supply chain from design through final package delivery

- **Technical Execution Areas:**
  - **Access to Advanced Packaging and Test**
  - Access SOTA ME
  - Access to Rad Hard ME, RF and Opto-Electronics
  - Joint Federated Assurance Center
  - Education & Workforce Development

Microelectronics Roadmap

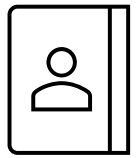


Packaging Industry Assessment



Packaging studies and roadmaps

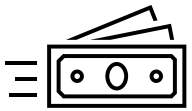
National and DoD policy and strategy



Capability list for US based domestic vendors

Gaps in capabilities, products, tech, etc.

Digital roadmap tool for microelectronics packaging using data analytics and data visualization to create a robust and dynamic decision-making tool.

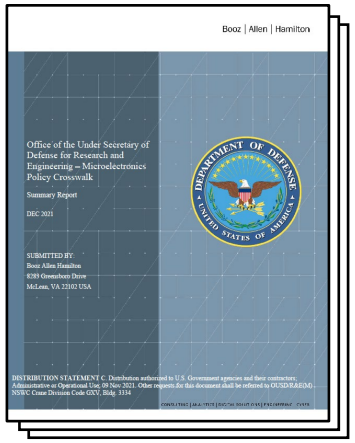


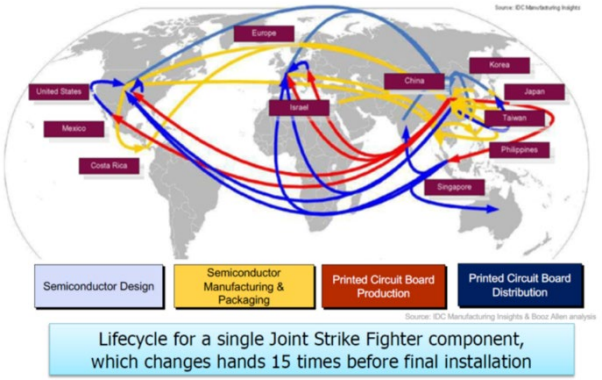
Determine the types of packaging needed to support DoD microelectronics
Forecast where commercial packaging industry is heading on its own without Government support
Decide what microelectronics packaging development the DoD should be investing in

Packaging Industry Assessment: Reports

Four main challenges in the ME ecosystem were identified.

1. Complex International Supply Chain
2. Consumer Focused Market
3. Increased International Competition
4. Rapid Technology Change and Adoption

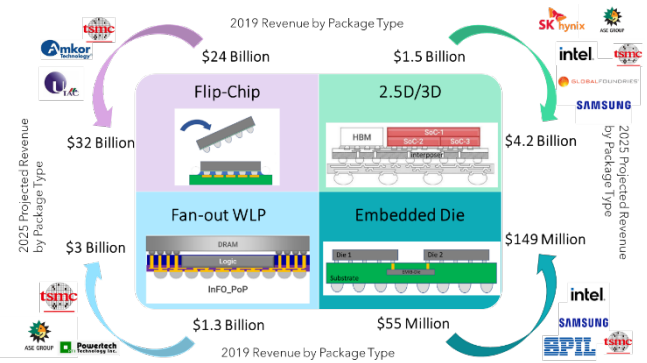




Full Report with Analysis, Policy Artifact Summaries, and Important Quotes Available

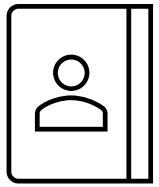
Key findings and trends from the surveyed documents are identified and presented in the following sections:

1. Semiconductor Market Forces
2. Fabrication Technologies – Leading Edge Chips
3. Advanced Packaging Technologies
4. Drivers and Disrupters



Full Report with Analysis and Summaries of Packaging Studies and Roadmaps Available

Packaging Industry Assessment: Capability Survey



On behalf of the Department of Defense, Booz Allen Hamilton is currently requesting surveys from microelectronics packaging leaders in the United States to assess the current health of the domestic advanced microelectronics packaging industry. Capabilities of interest include:

- Heterogenous integration (chiplet-based design involving interposers)
- Related fine-pitch interconnect packaging technologies (FOWLP, TSVs, RDL, etc.)

If interested in participating in this survey, please contact

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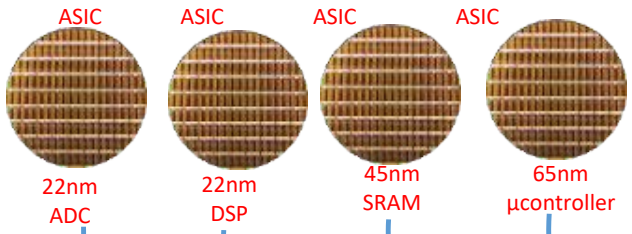
Why Industry is Moving to HI

SIP becoming the new SOC

- Modular approach vs. Monolithic approach
- Not every logic function (IP) needs to be designed in the same process node (HI)
- Leveraging IP in the form of chiplets
- Current integration of chiplets on silicon interposers, but thin-film laminate is gaining steam
- Includes latest IC packaging 2.5D, 3D, FOWLP technologies
- Board design expertise required for next-gen multi-chiplet HI designs

Optimization of wafer area (node) driven by technology, required performance and cost



Timeline – Design Factors

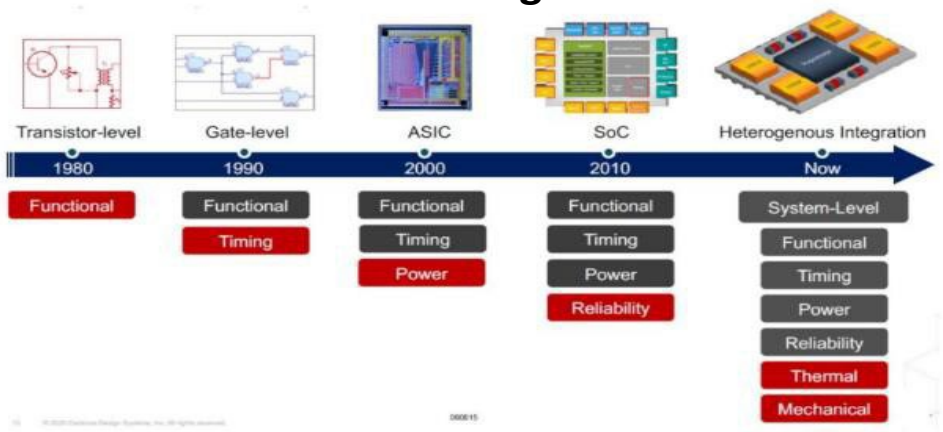


Figure 4: The timeline for chip/package co-design urgency (Source: John Park, Cadence)

Factors / Considerations

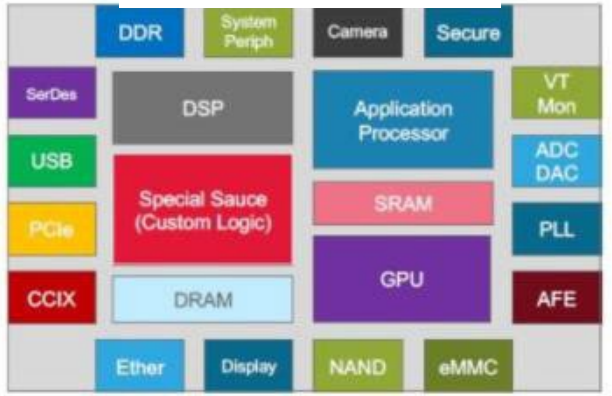
- Each chiplet node optimized
- Each chiplet manufactured at scale
- Chiplet reuse, less redesign
- MCP size ≈ SOC size
- Power ↓
- Cost ↓

Disaggregation

	Monolithic	Diff	Chiplet
Wafer Cost (7nm)	$9,350	1x	$9,350
Total Die Size	600mm2	1.1x	660mm2
Single Die Size	600mm2		165mm2
Gross Die per Wafer	96		387
Defect Rate (per cm^2)	0.2	1x	0.2
Effective Area	80%	1x	80%
Estimated Yield (Dingwall)	43%		78%
Net Die per Wafer	42		300
Single Die Cost	$224		$31
Total Die Cost	$224		$124
Total Test Cost	$10	1.2x	$12
Package and Packaging	$160	1.25x	$200
Packaging Loss	1%	4x	4%
Total Manufacturing Cost	$398		$347

Table 1. Chiplet cost comparison. This comparison assumes a large die (600mm²) with little redundancy (80% effective area) and a large (60x60mm) organic package is split into four identical chiplets. The chiplets reduce total die cost but require a more expensive package, producing a net savings of 13%. (Source: The Linley Group estimates)

Notional HI MCP



SHIP Program Overview

STATE OF THE ART (SOTA) HETEROGENEOUS INTEGRATED PACKAGING (SHIP) PROGRAM

SHIP Digital

intel

Secure Packaging

mercury

SHIP RF

qorvo

Design, Assembly, Test, & Security Knowledge Transfer

00491

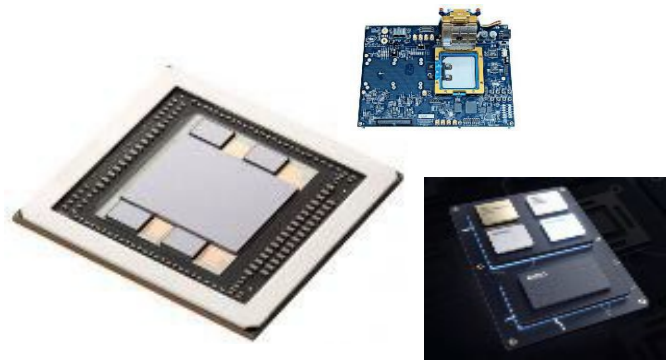
SHIP Program Motivation & Objectives

Motivation

- Provide DoD earlier access to assured SOTA Microelectronics
- Develop a US-based economically-viable SOTA heterogeneous integration and packaging capability for DoD system performance enhancement and assurance/security applications, which currently doesn't exist
- Provide sustainable, quantifiably-assured SOTA advanced packaging access to the DoD and the DIB

Objectives

- Developing a model for access to SOTA parts
  - Self-sustained business model for DoD access to customized SOTA parts using standard commercial flow
  - The prototypes are a tool to validate the model, not the end goal
- Advancing DoD capabilities
  - Improved performance, SWaP-C
  - Availability of SOTA parts
  - Domestic manufacturing
  - Increased functional density
  - Pathway to modernization



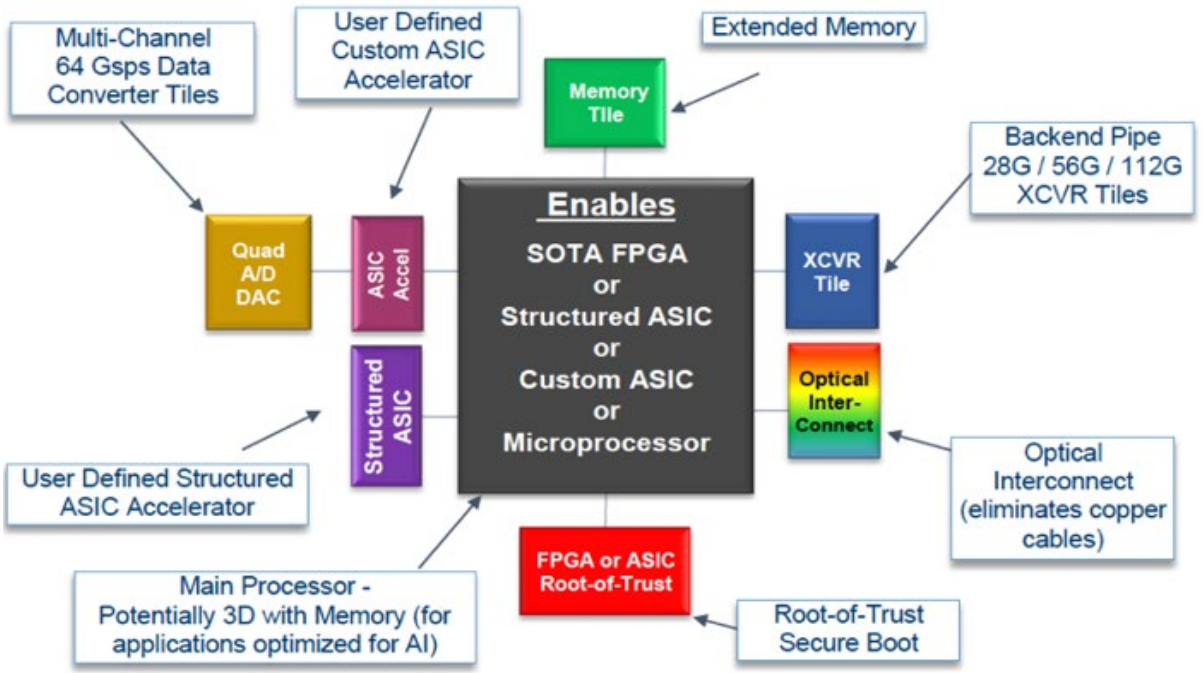
Delivering value to the USG and the DIB

SHIP leverages top commercial tech while allowing DoD customization

SHIP Digital

Key focus:

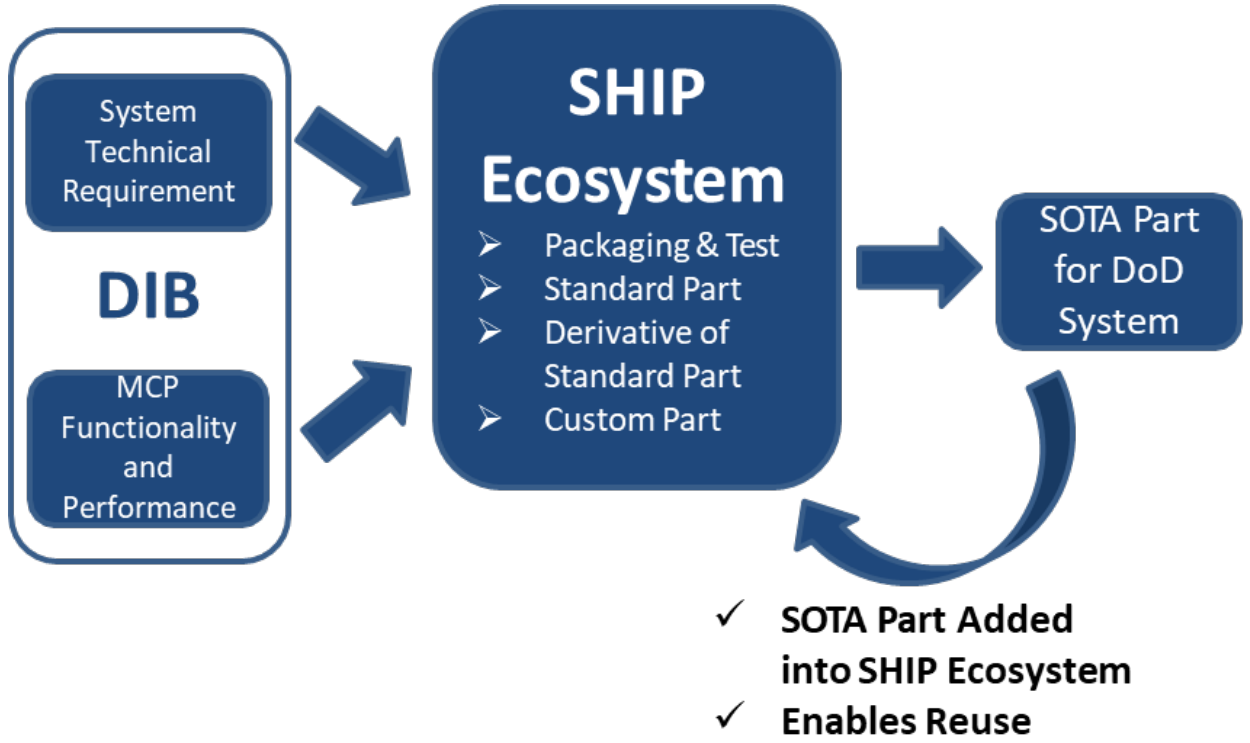
- SOTA MCP products utilizing Intel's commercial packaging, assembly, and test
- Create a catalog of designs, die, chiplets, package types, etc.
- Reuse and Standardization
- DoD customized MCP demonstrations
- Production: decrease SWAP-C and develop time
- Adoption & Use in military systems



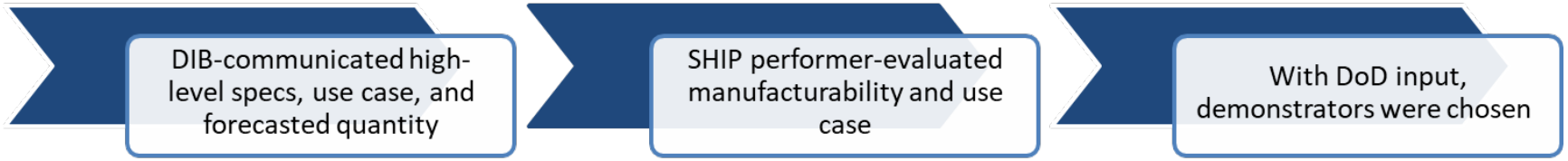
SHIP Digital will provide the DoD access to a robust catalogue of chiplets that can be assembled and packaged for a standard, derivative, or custom SOTA part.

SHIP Digital Transition

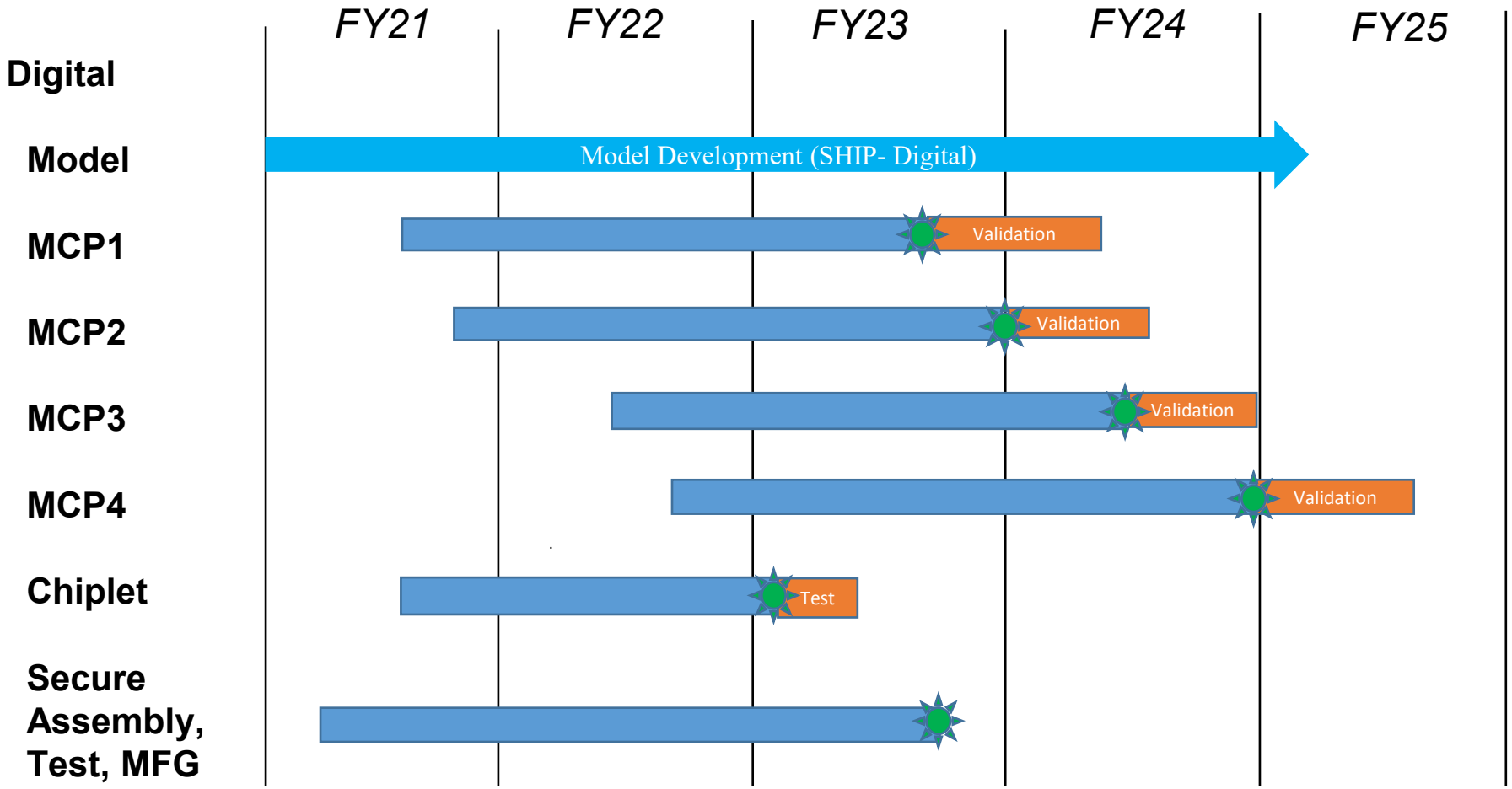
- **Collaboration with the DIB is critical for SHIP Transition**
- SHIP program creates a new innovative environment for the DIB to address the DoD push to modernize military systems
- DIB is in the position to translate DoD warfighting capabilities down to MCP functionality and performance requirements
- DIB gains access to DoD customized SOTA microelectronics

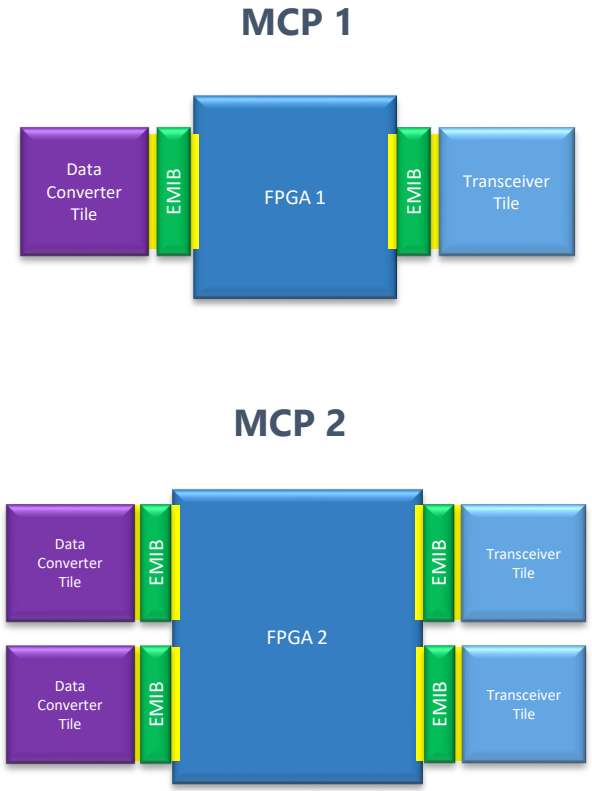


SHIP Digital Demonstrator Selection Process



SHIP Digital Roadmap

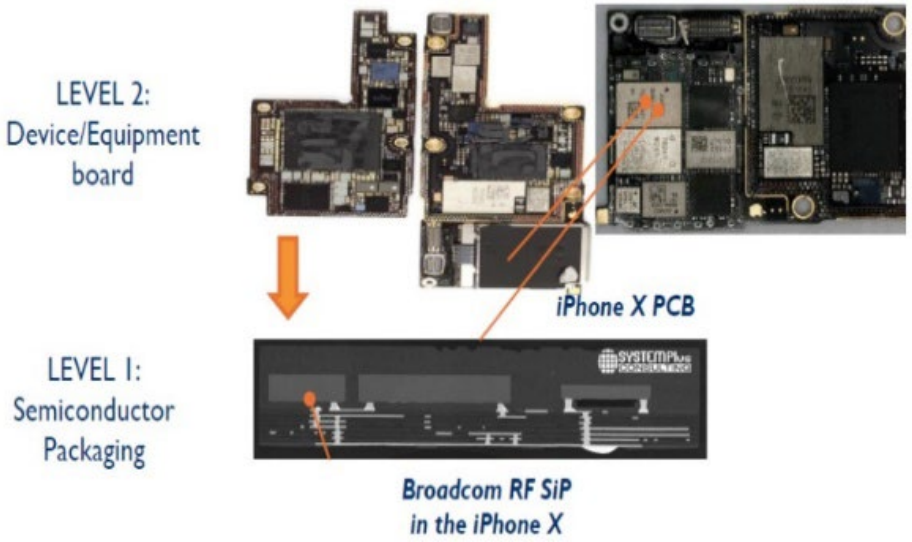




SHIP RF

Key focus:

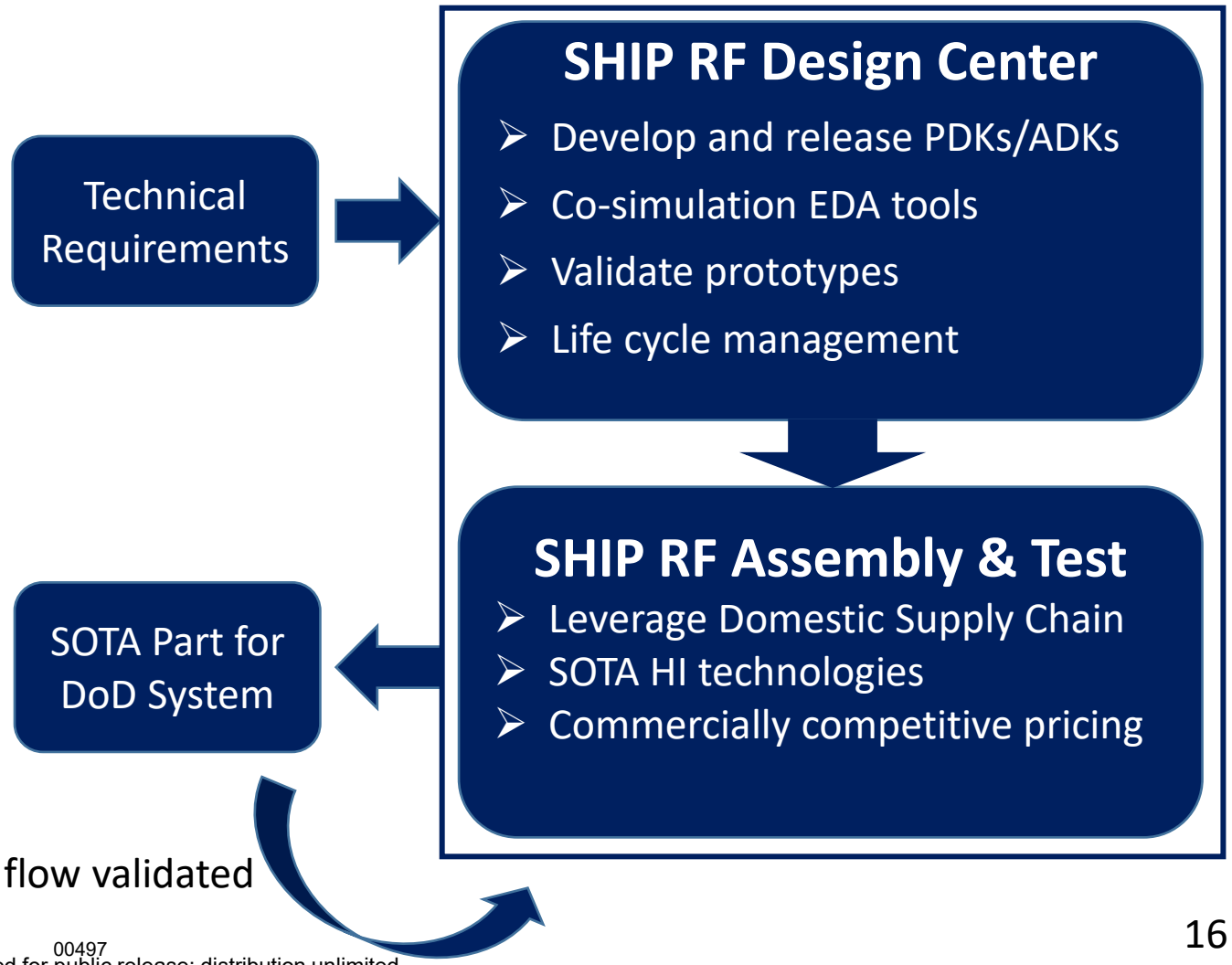
- Design, packaging, and assembly as a service
- Re-shoring mature manufacturing, assembly, and test from commercial product lines such as high-volume flip-chip capabilities
- Qorvo is enabling access to advanced RF packages by providing a full suite of design tools, advanced packaging platforms, and a wide selection of material choices
- DIB and DoD will be able to leverage this commercial design flow through SHIP RF using developed PDKs and ADKs to design custom devices



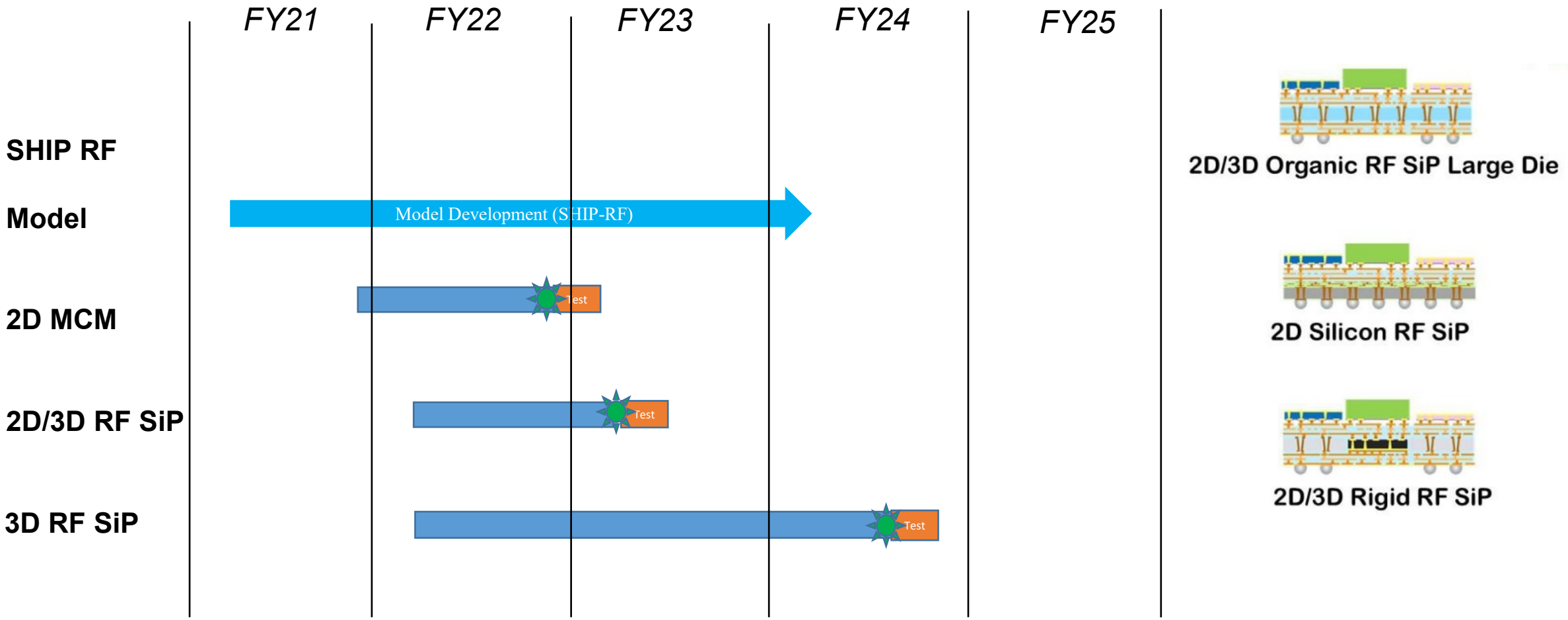
Example of RF packaging
Source*: Advanced RF System-In-Package for cell phones 2019,* Yole Development.

SHIP RF Transition

- **Collaboration with the DIB is critical for SHIP Transition**
- SHIP RF creates innovative design, assembly, and test environment for the DIB to address the DoD modernization push through custom RF packages
- DIB Partners in place with potential transition programs identified
- Prototypes serve as “pipe cleaners” for the SHIP RF design and assembly flow
- DIB gains access to DoD customized SOTA front end RF modules for current and next-gen systems



SHIP RF Roadmap

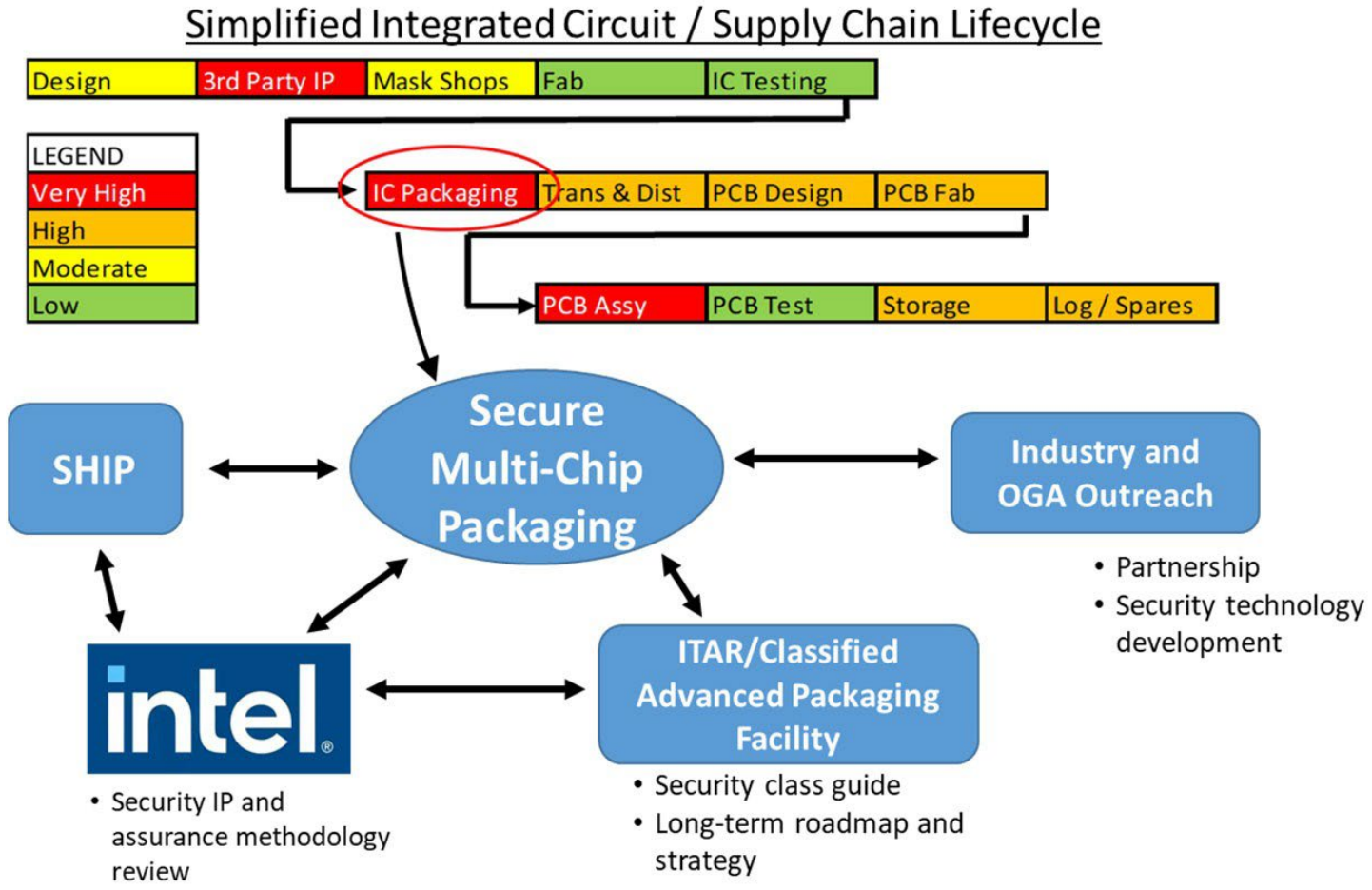


SHIP Secure Packaging

Objective:

Develop SHIP design path for ITAR/classified 2.5D and 3D HI components

- Develop portfolio of security solutions to meet DoD program requirements
- Demonstrate solutions with 2.5D/3D secure prototypes

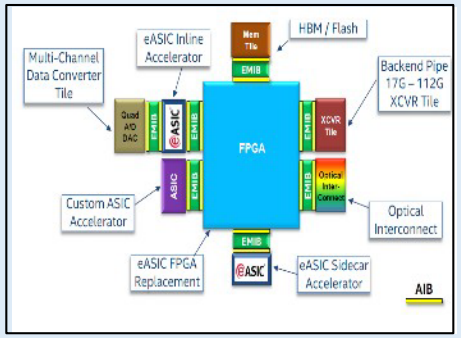


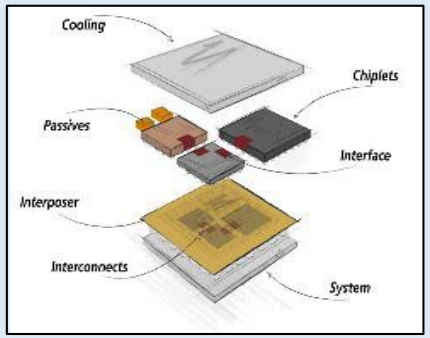
Advanced Heterogeneous Integration, Packaging & Test

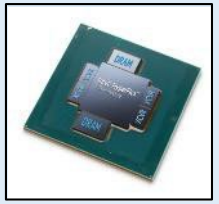
DoD ME Ecosystem

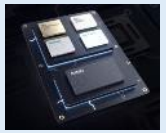
Current Chiplet Portfolio

New QA'd Chiplets









SOTA Quantitatively Assured Advanced Packaging Process Flow

- **SOTA heterogeneous packaging:**
  - Provides significant SWAP benefits
  - Allows semiconductor material decisions to optimize for cost or performance
  - Establishing domestic on-shore SOTA / SOTP production capacity

- **Reuse -** existing technology and components enablesrapid system development and deployment
- **Quantifiable assurance -** implements much greater security into the supply chain design and assembly process
- **Multiple packaging options -** enable tailoring performance for application needs

Designing and validating a sustainable model for access to customized SOTA packaging using standard commercial flows

Modernization

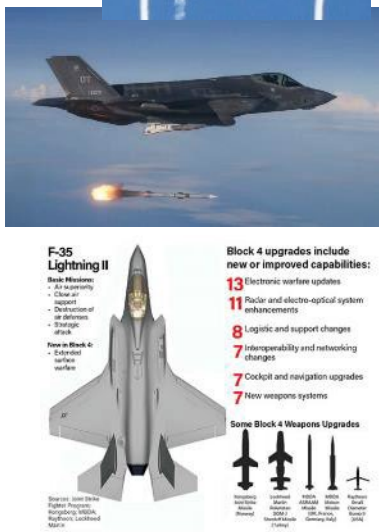
Increased Functional Density and Performance

- Modernization
  - Facilitated through SWaP-C improvements
  - Enables increased functional density of systems
    - Capabilities and performance continually augmented and fit into the same from factor

F35A 2006
1st Flight

Continuous enhancements and improvements will be made to increase capabilities that make the F-35 more lethal and survivable

Current
Block 4



53 improvements to counter both air- and ground-based threats

Increasing the number of separate subsystems into ever more tightly integrated packages → Increased Function, Performance, Capabilities

Summary

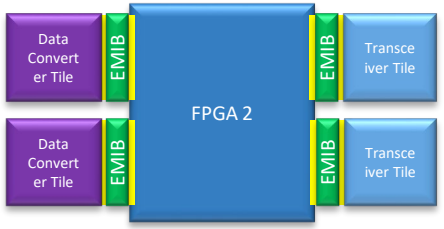
- **SHIP Model**
- Self sustained business model for access DoD customized SOTA parts using the standard commercial flow
- The prototypes are a tool to test the model, not the end goal

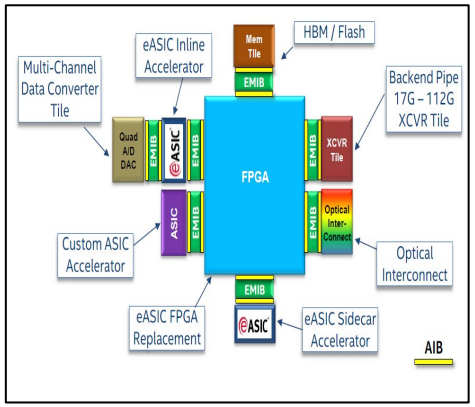
DIB Engagement

- Pathway to programs for coordination
- Transition into program portfolios
- Building the ecosystem

Prototypes

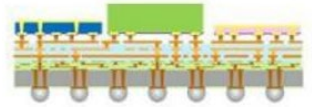
- Currently in design
- Delivery starting in FY22



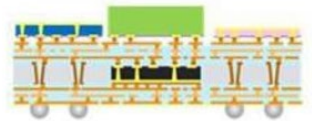


Transition Strategy

- Reuse of technology and components enables rapid system development and deployment
- Custom configurations to meet performance of a particular system specification



2D Silicon RF SiP



2D/3D Rigid RF SiP