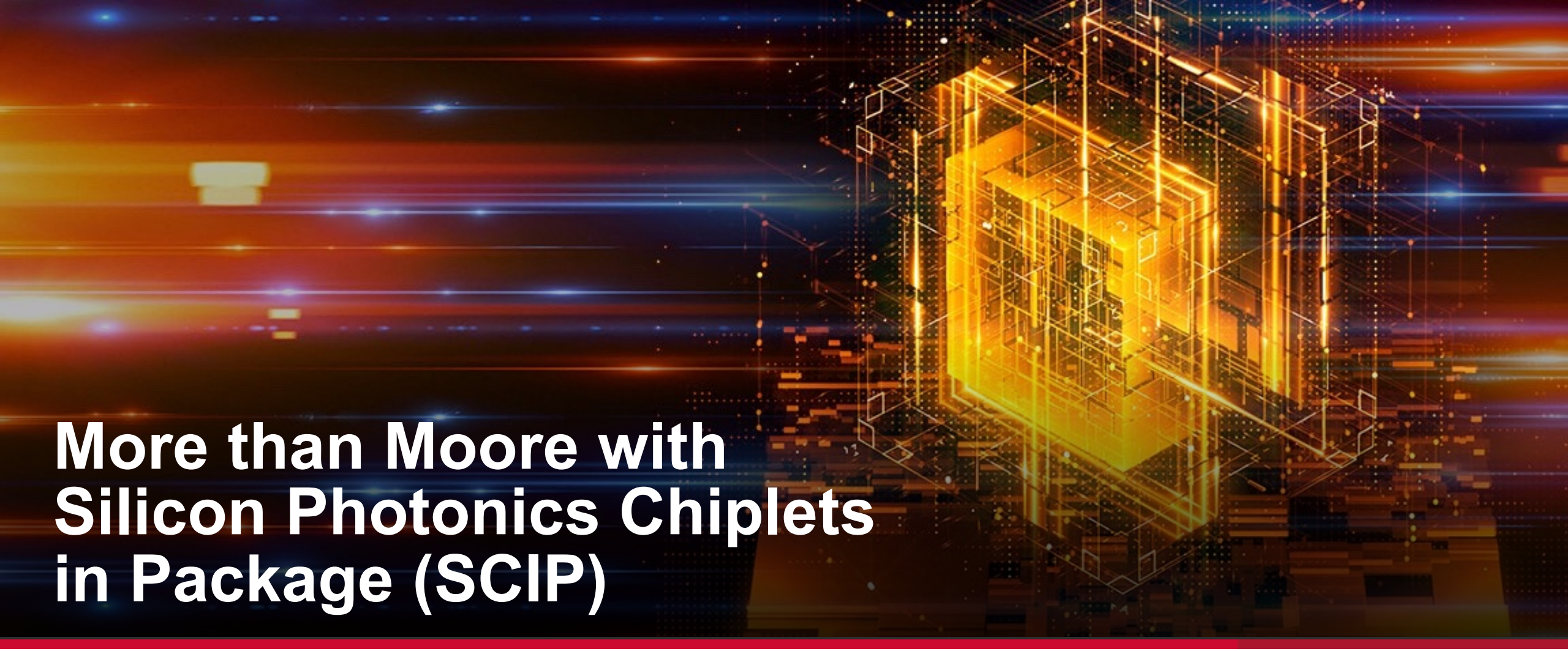

More than Moore with Silicon Photonics Chiplets in Package (SCIP)

Vivek Raghunathan
Senior Principal Engineer & Product Architect, Silicon Photonics
Optical Systems Division

Sukeshwar Kannan
Principal Engineer, Silicon Photonics Packaging
Optical Systems Division

Han Peng Goh
Director, Platform Development, Silicon Photonics
Opticals Systems Division

Reza Sharifi
Sr. Manager , Packaging Global Operations

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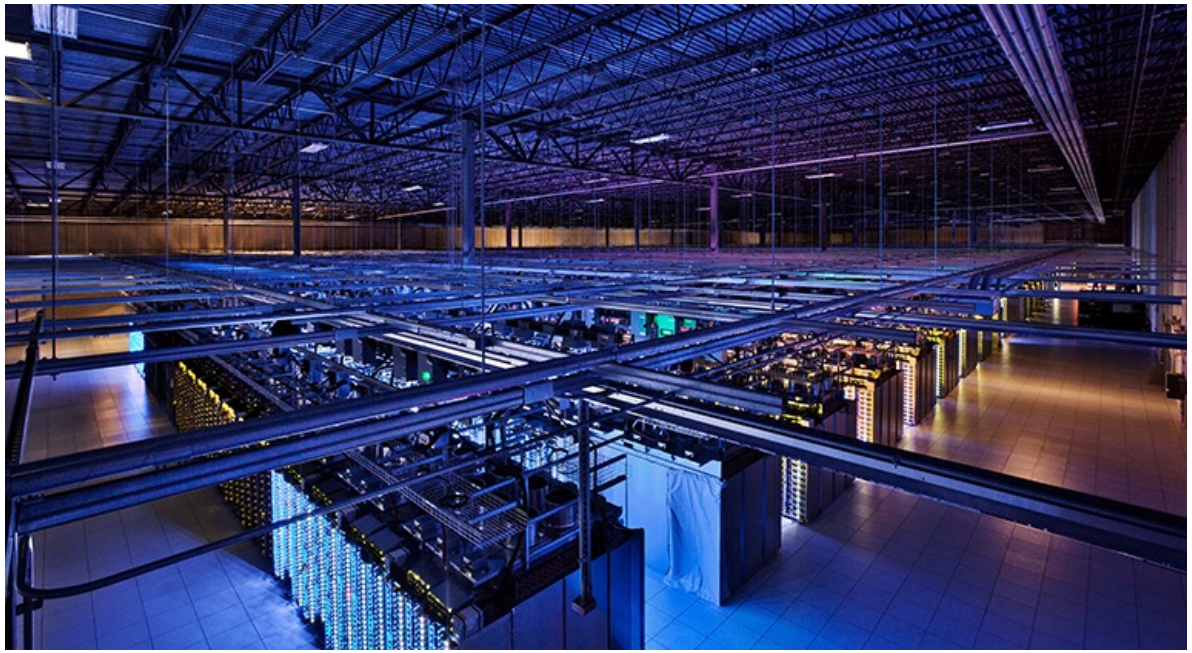
Datacenters: Powering Everyday Cloud Applications



$100B Annual Capex Spend by Cloud with 15% CAGR[1]

19.5 Zettabytes of Cloud Data Movement[2]

Per hyperscale datacenter
> 100k Servers
> 10k Switches
> 1M Optical Interconnects

Source:
1. 650 Group, Cloud Total Market and Forecast Report
2. Cisco Global Cloud Index, https://blogs.cisco.com/news/acceleration-of-multicloud-era
3. Left: Digital Realty's Loudoun Three campus in Ashburn, Virginia. Photo courtesy of Digital Realty
4. Right: Google's Council Bluffs, Iowa Data Center. Photo courtesy of Google

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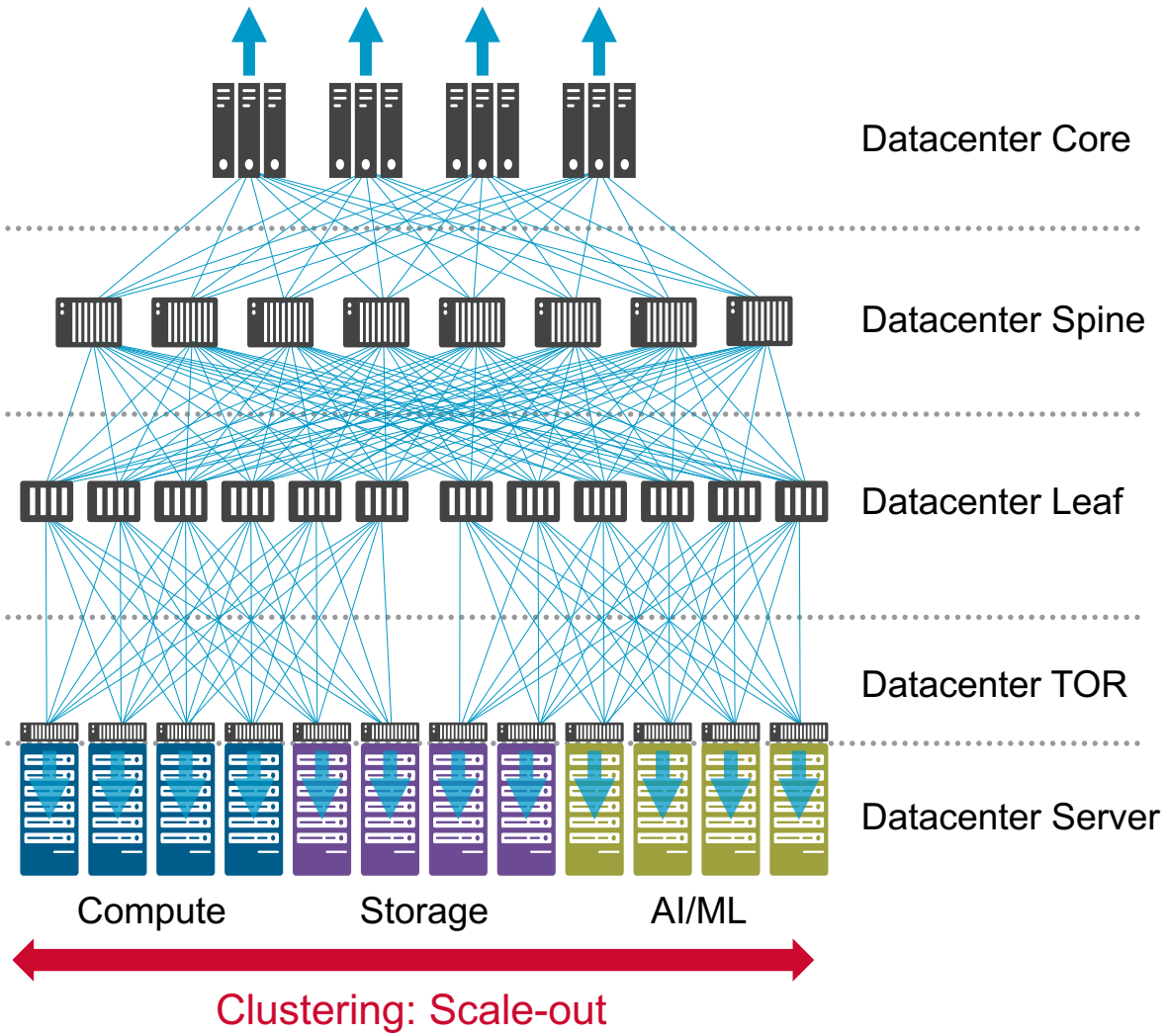
Datacenter Scale-out Requires Massive Fabric Connectivity



>25%

annual growth for intra-datacenter traffic*

- Compute and storage resources pooled within datacenter and across regional zones
- Requires long-reach, low-latency interconnects
- Fabric increasing as % spend and power consumption of infrastructure

* Source: CRN, https://www.crn.com/news/data-center/why-public-cloud-data-center-spending-is-at-an-all-time-high

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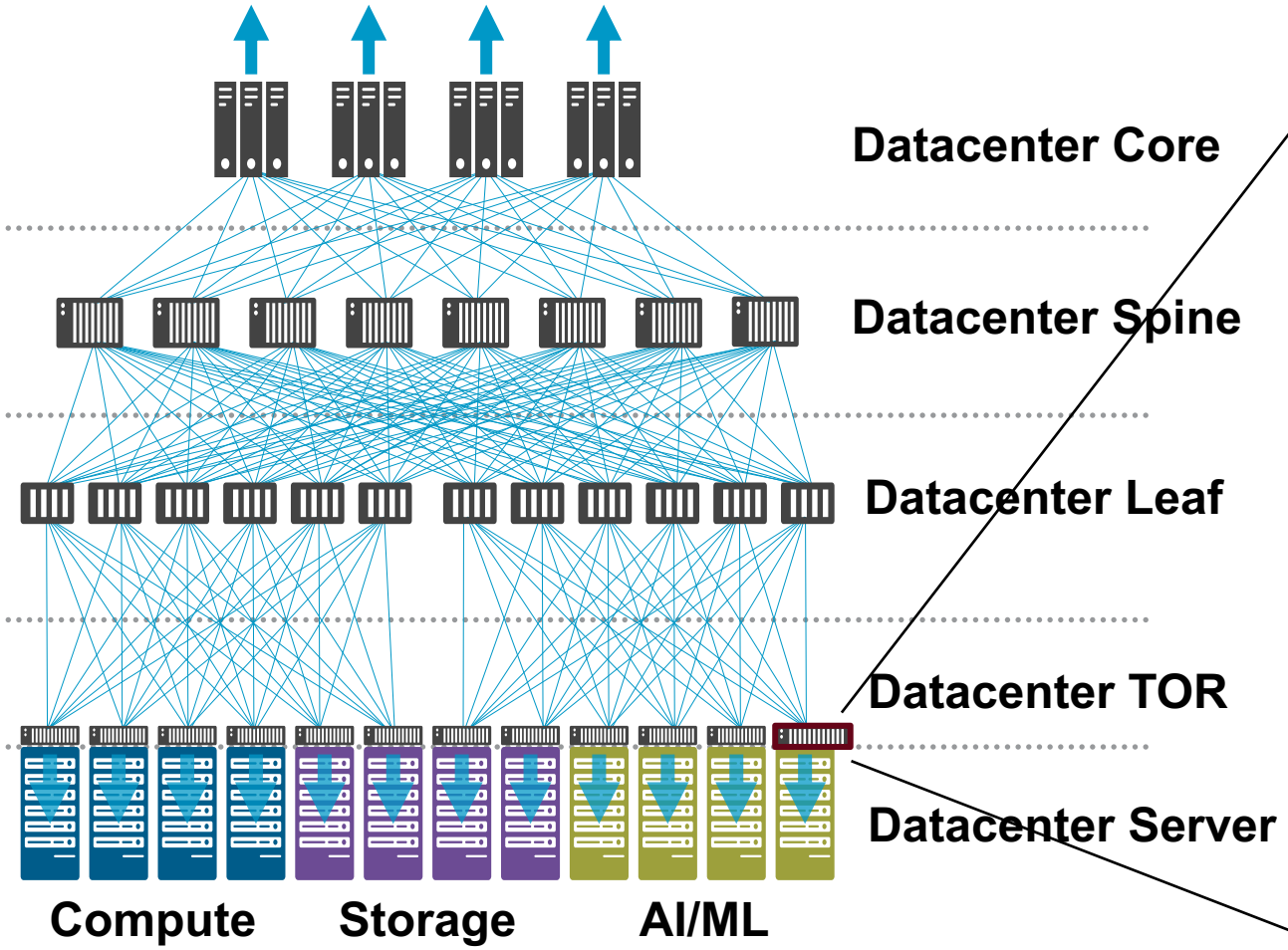
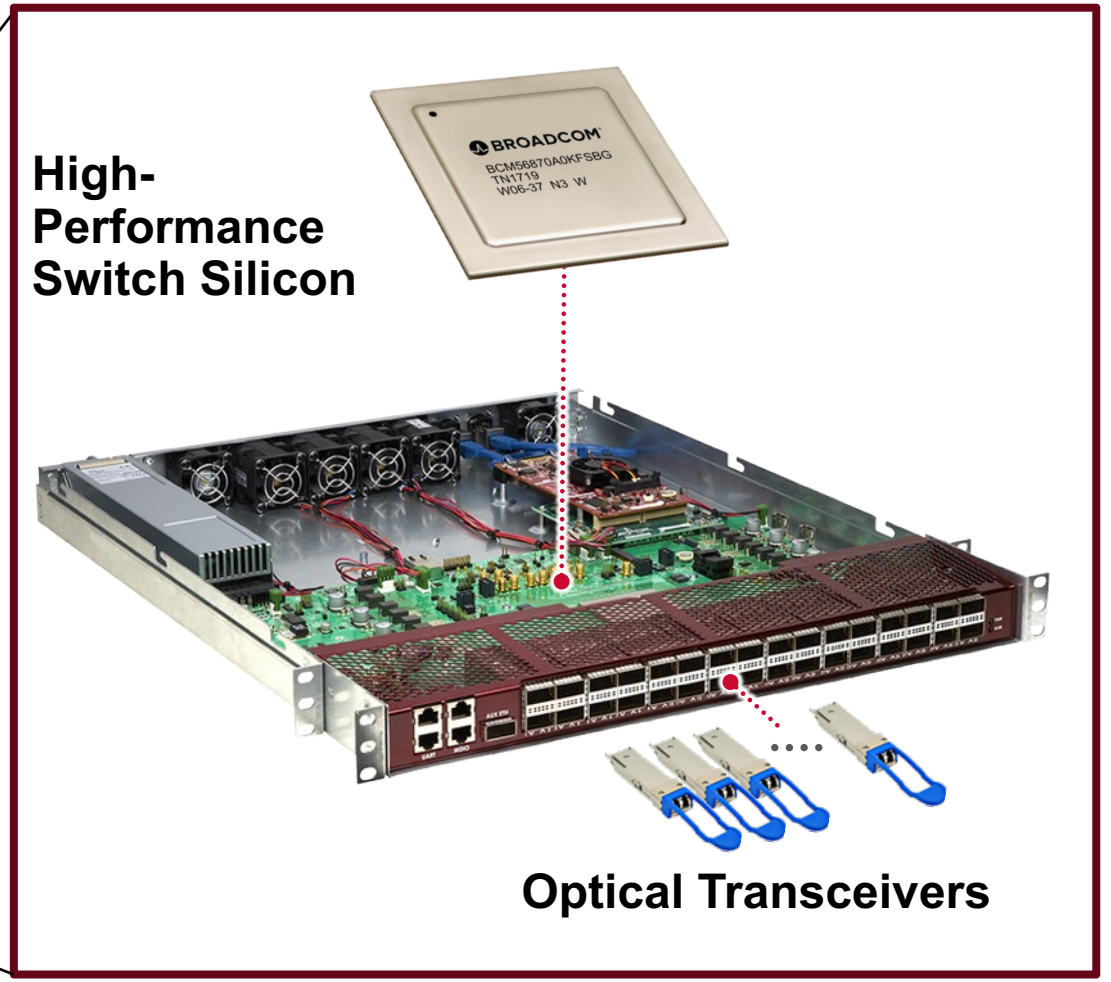
Datacenter Scale-out Requires Massive Fabric Connectivity





* Source: CRN, https://www.crn.com/news/data-center/why-public-cloud-data-center-spending-is-at-an-all-time-high

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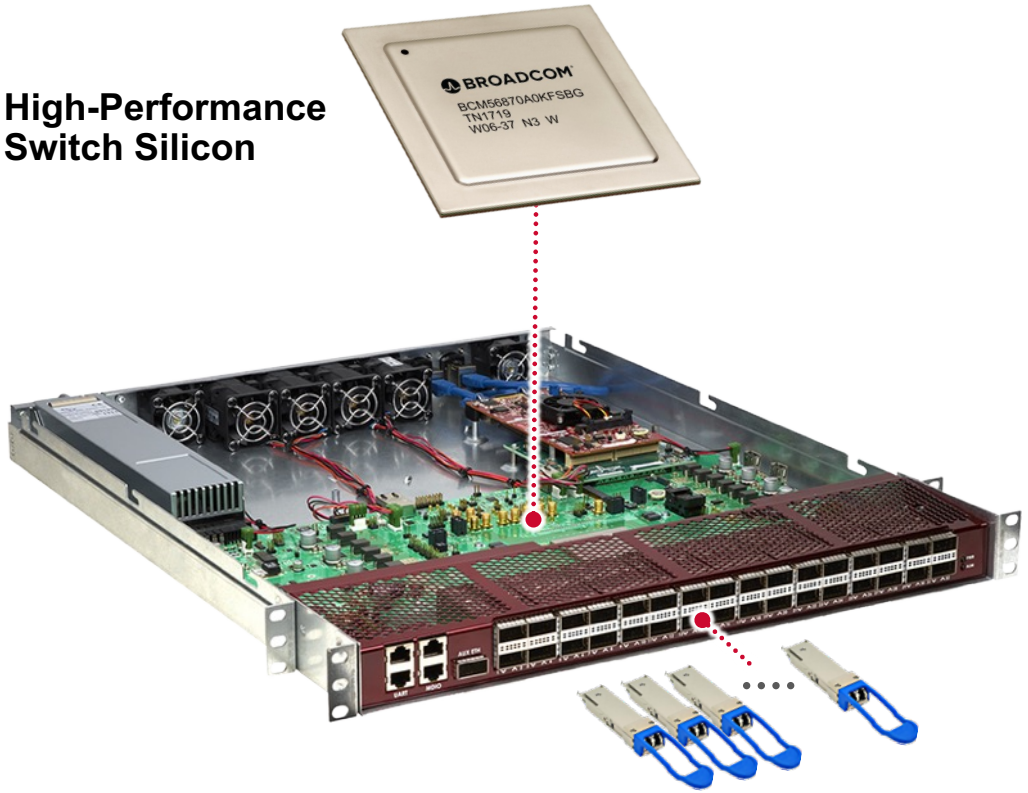
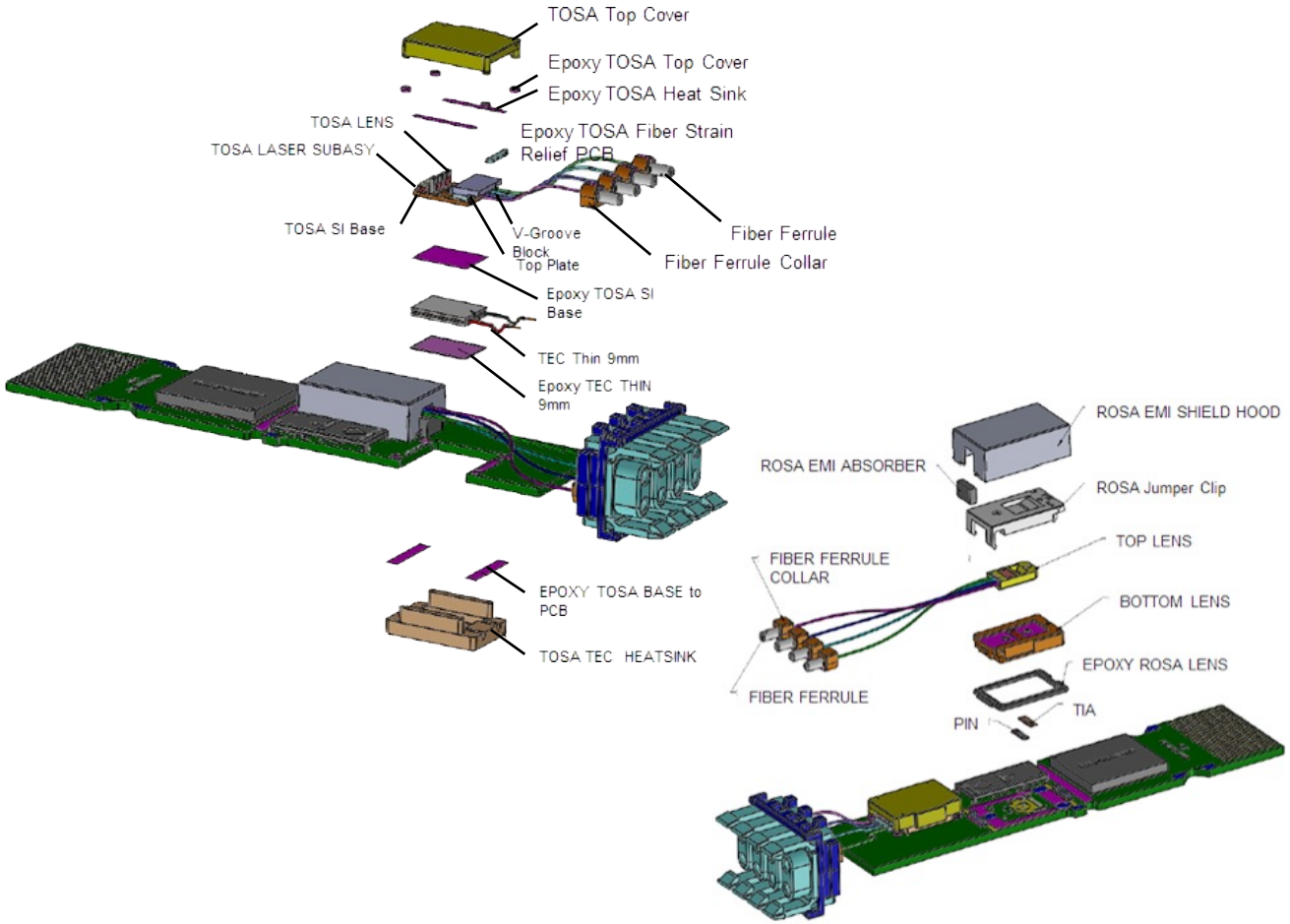
Complexity of Each Rack Unit Box in the Datacenter

High-Performance Switch Silicon



Optical Transceivers



600M Ports Shipped in 2020[1]

150M Units Shipped in 2020[2]

1. E16A_Ethernet_Switch_Layer_2&3_WW_Tables_1Q21
2. LightCounting 2Q21 Quarterly Market Update, 17 June, 2021

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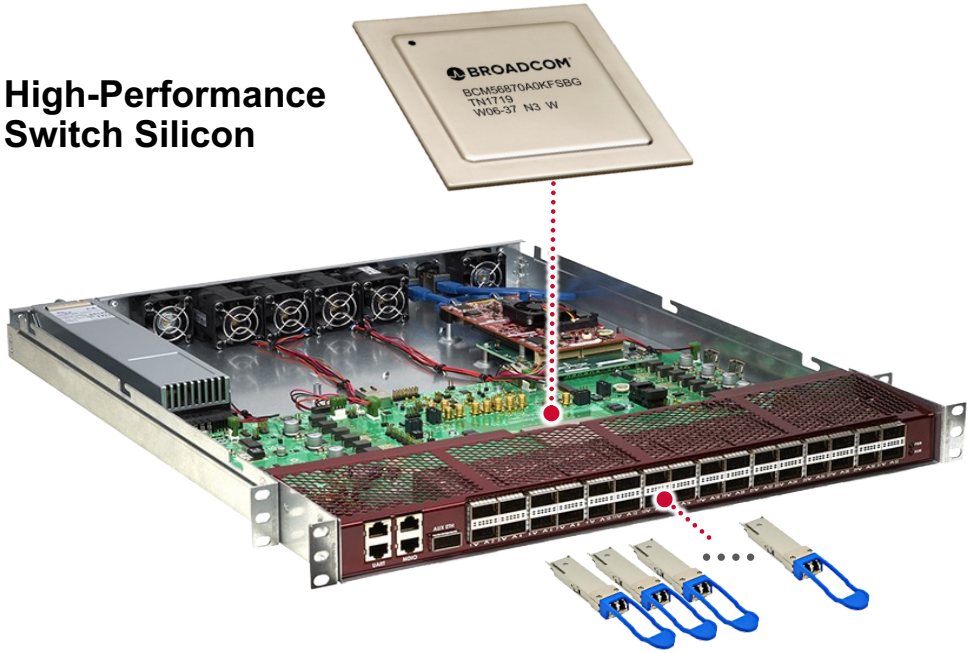
Traditional Rack Unit System Design Does Not Scale Efficiently

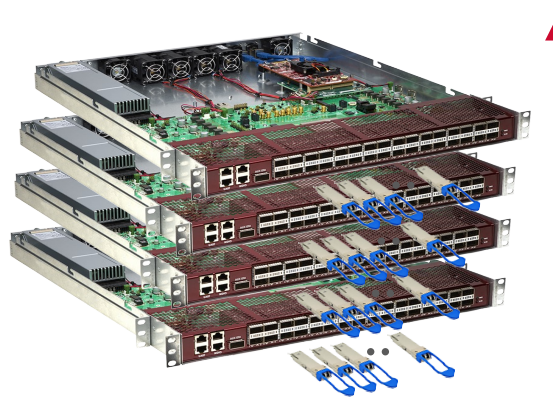
High-Performance Switch Silicon



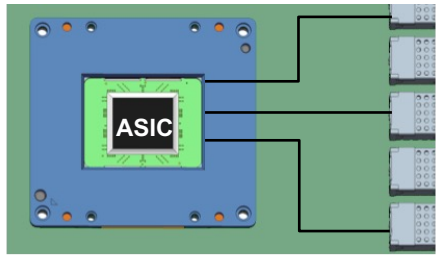
Optical Transceivers

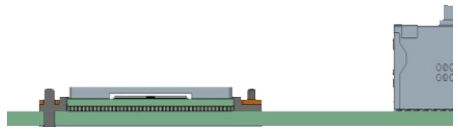
Front plane pluggable (FPP)

How do you **scale bandwidth?**



Stack more rack units





Increase Cu channel speed

Traditional Scaling Approaches Introduces Undesirable Inefficiencies in Power, Size and Cost

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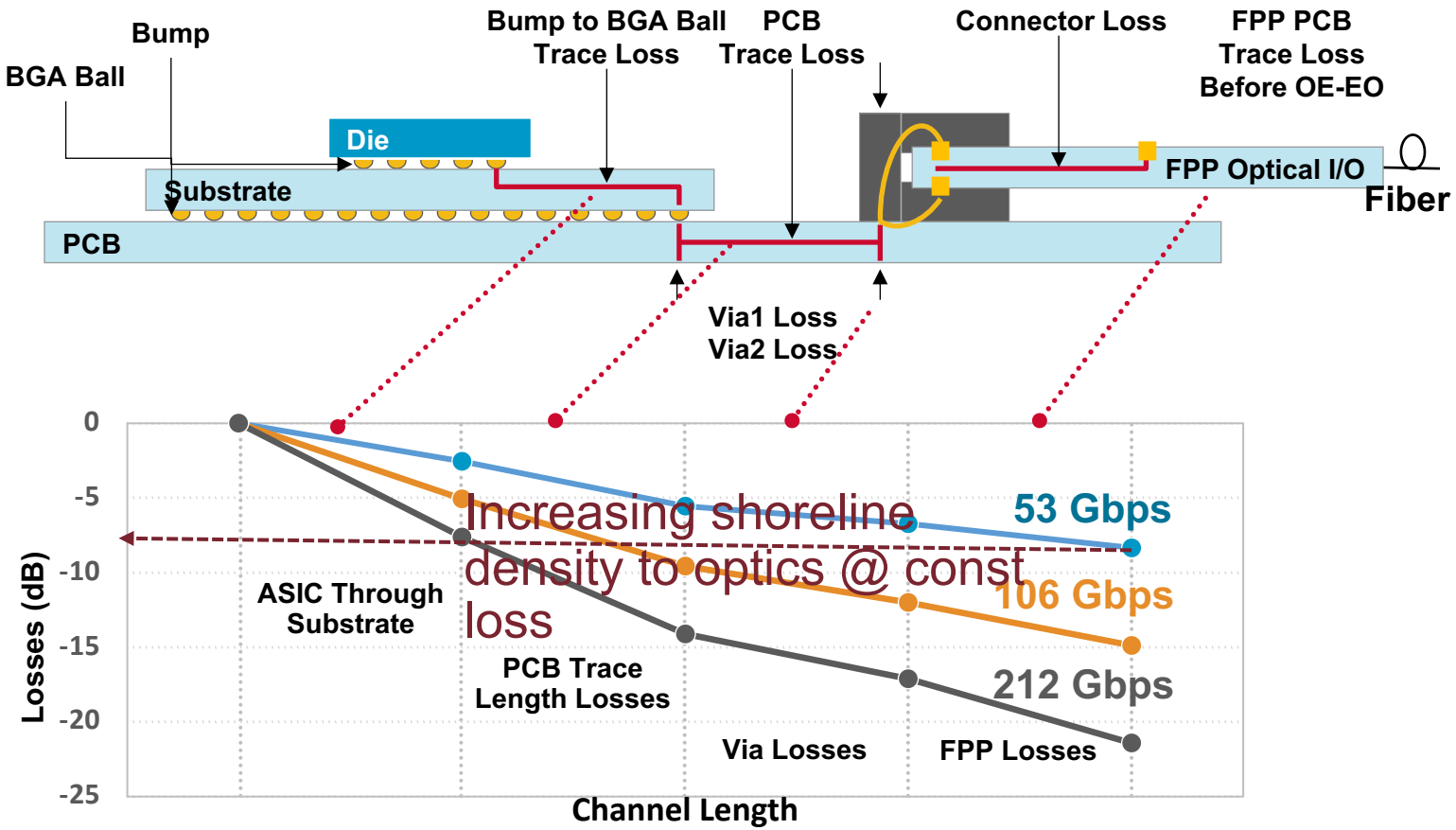
Copper I/O Approaching a Limit



A. Björlin, "Breaking the Bandwidth Barrier: Silicon Photonics Optical I/O", SEMI Americas Virtual Forum, 2021

Each interface in the link between ASIC and Optics adds *analog* loss, requiring additional SerDes Power

The losses grow with each generation of interface speed, but analog efficiency is quickly falling behind Moore's Law.

Most importantly, the system doesn't scale efficiently with channel count and BW

Highly Dense, Short RF Channel Connection between ASIC and Optics is more Power Efficient

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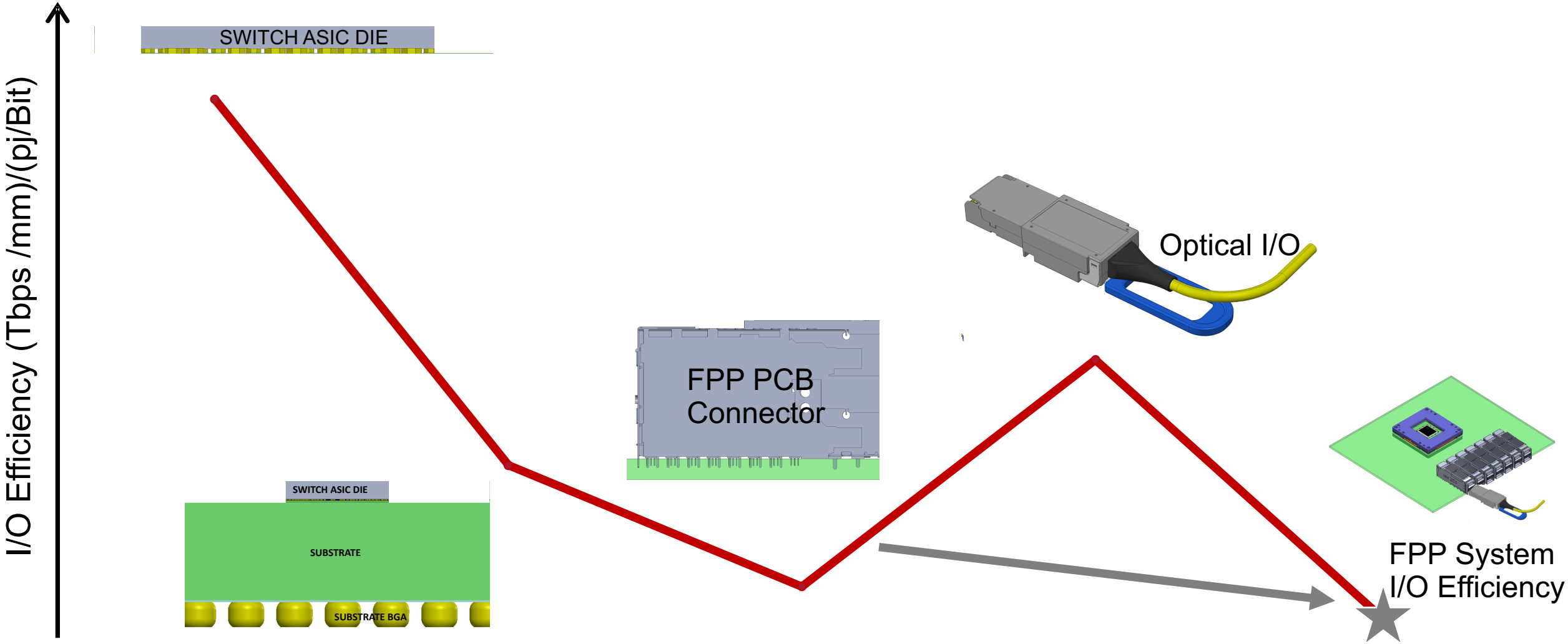
Analog I/O Efficiency of the Front Plate Pluggable (FPP) System



I/O Efficiency for the FPP System is limited by the FPP PCB Connector

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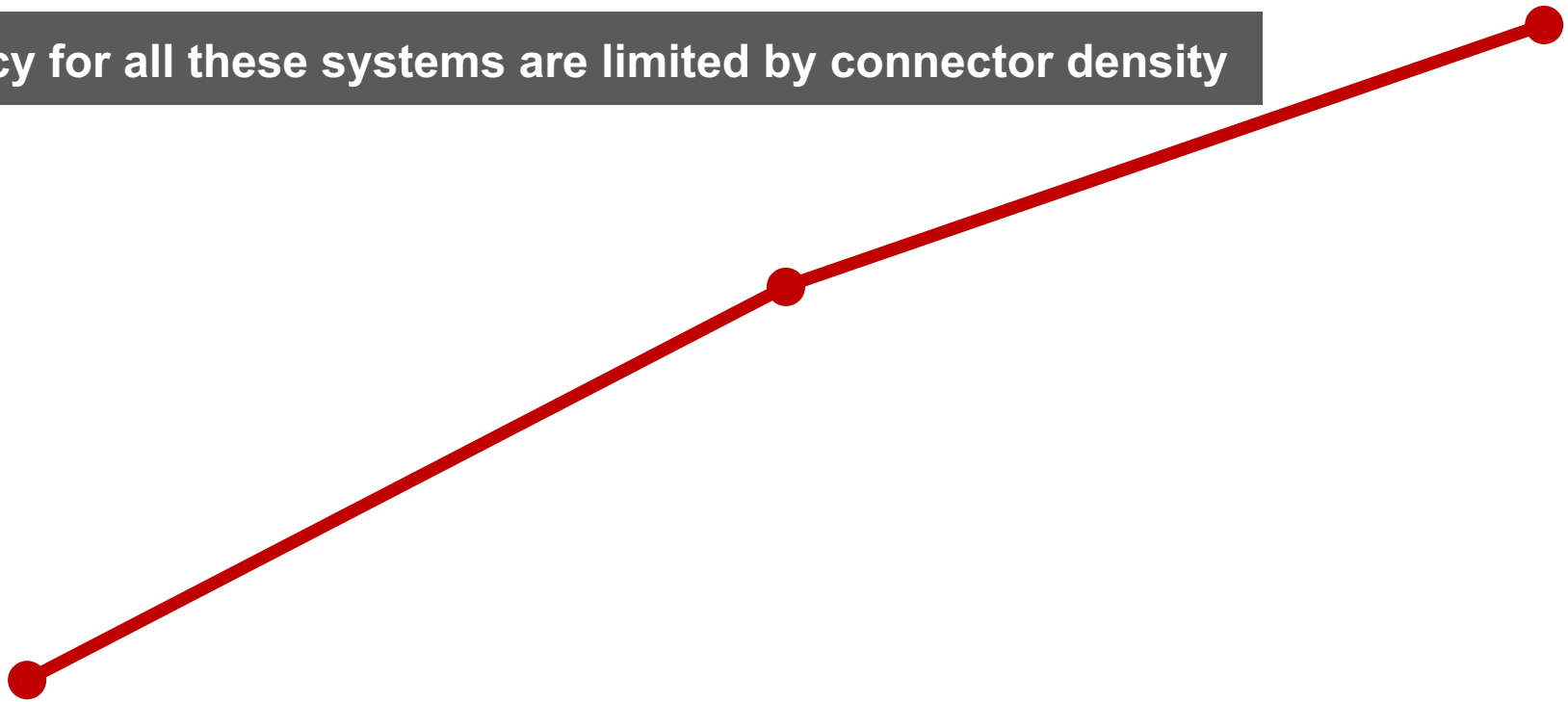
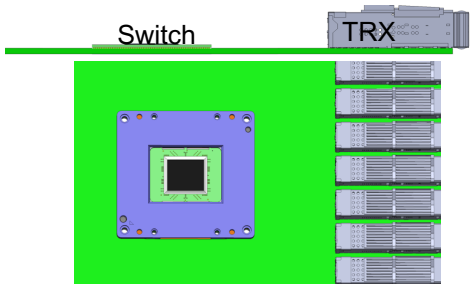
Moving Optics Closer Improves I/O Efficiency

I/O Efficiency for all these systems are limited by connector density

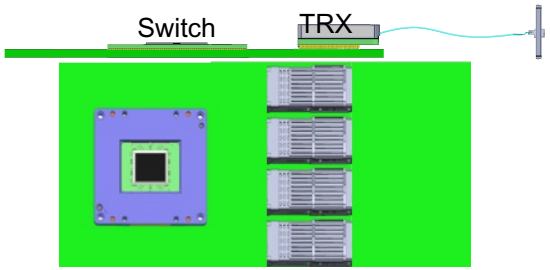
I/O Efficiency (Tbps /mm)/(pj/Bit)



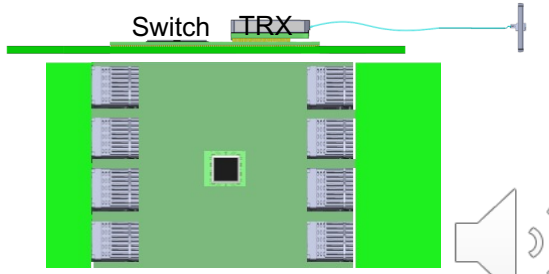
FPP



On board optics (OBO)



NEXT GEN OBO



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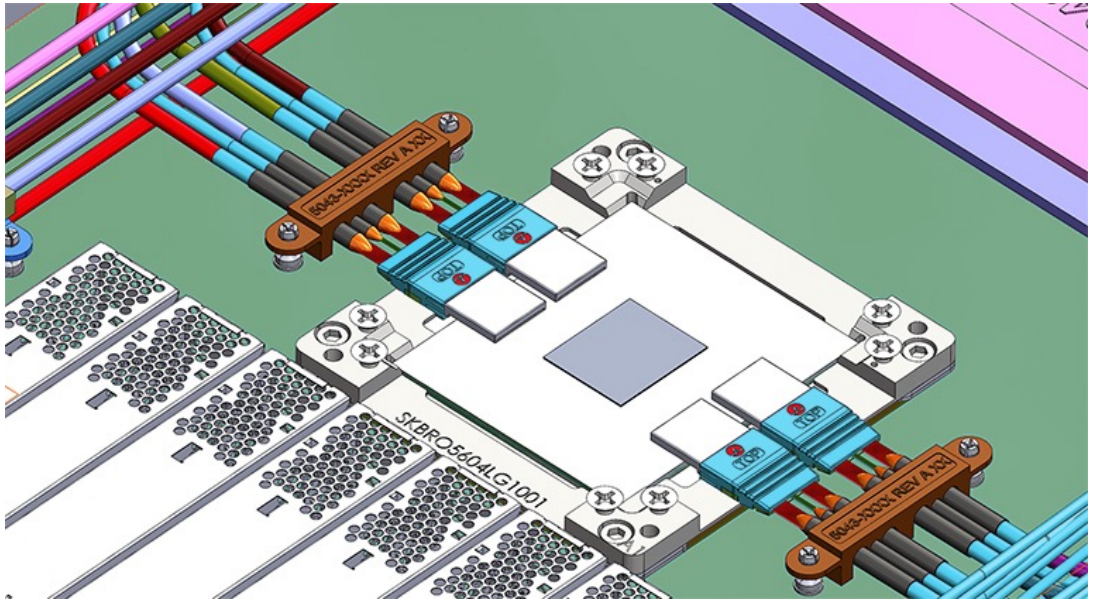
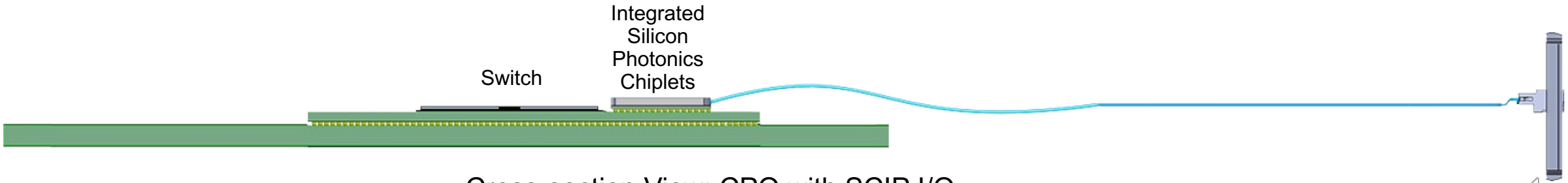
Co-packaged Optics (CPO) with Silicon Photonics Chiplets



Top View: Multi-Chip Package with ASIC die and Silicon Photonics Chiplets in Package (SCIP) providing optical I/O



Cross-section View: CPO with SCIP I/O

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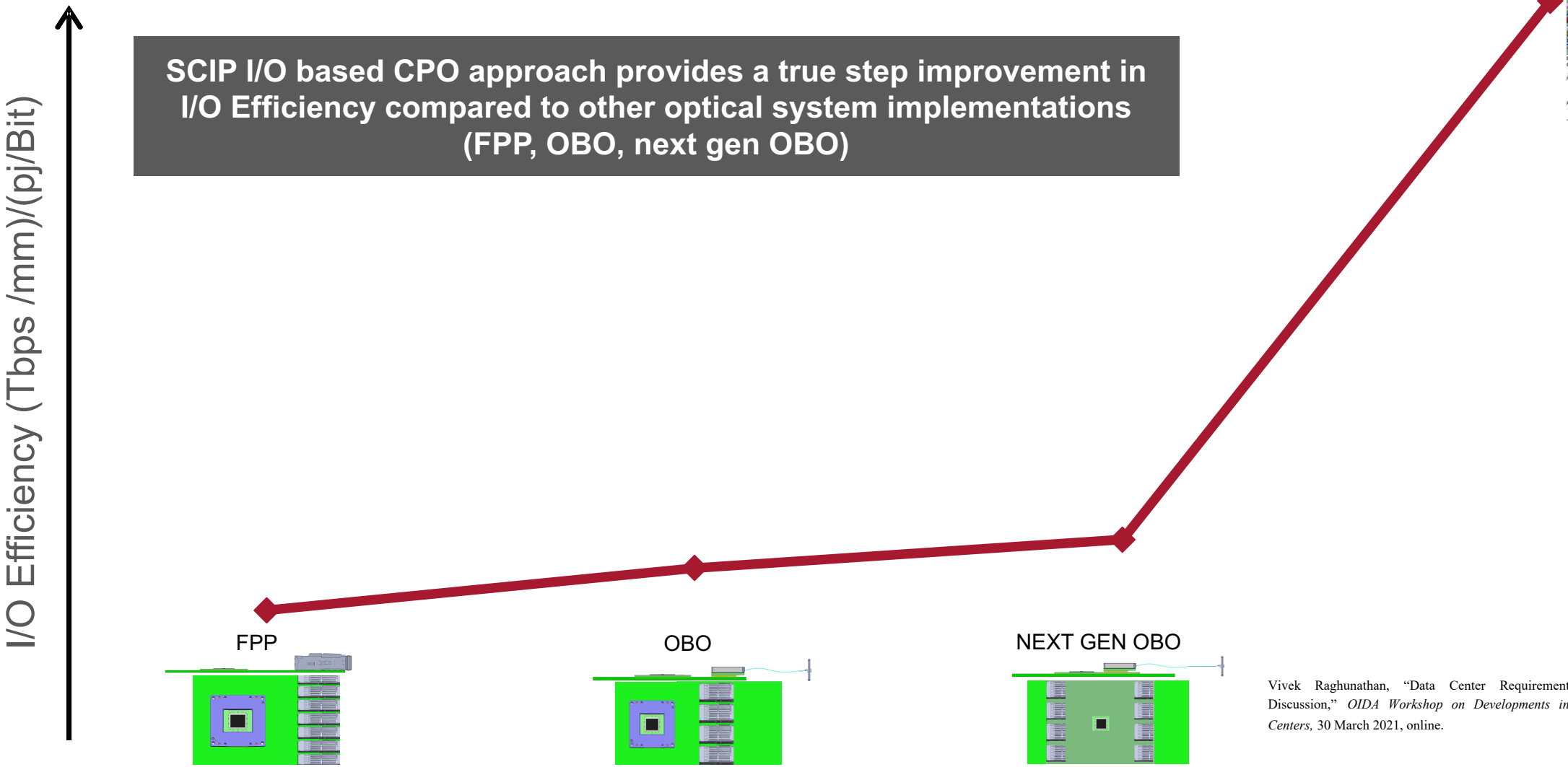
SCIP based CPO for I/O Efficiency Improvement

SCIP I/O based CPO approach provides a true step improvement in I/O Efficiency compared to other optical system implementations (FPP, OBO, next gen OBO)



Vivek Raghunathan, "Data Center Requirements and Technology Roadmap Panel Discussion," *OIDA Workshop on Developments in Co-Packaging Technologies for Data Centers,* 30 March 2021, online.

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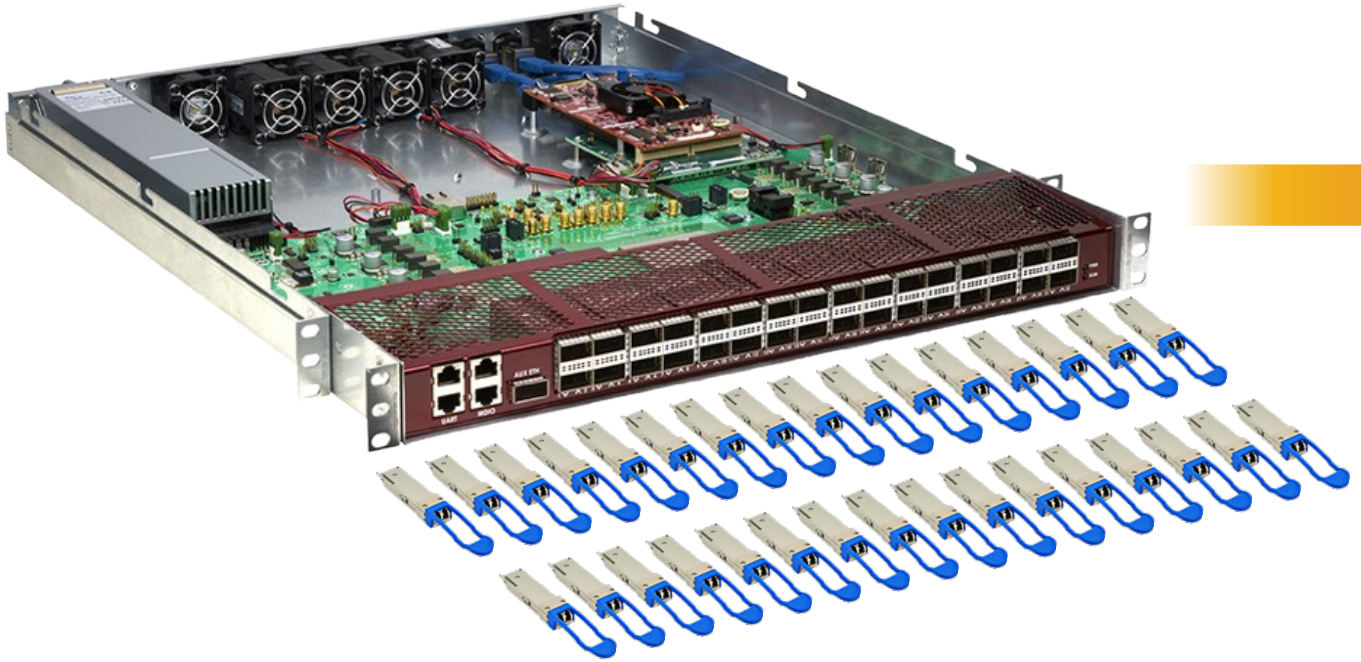
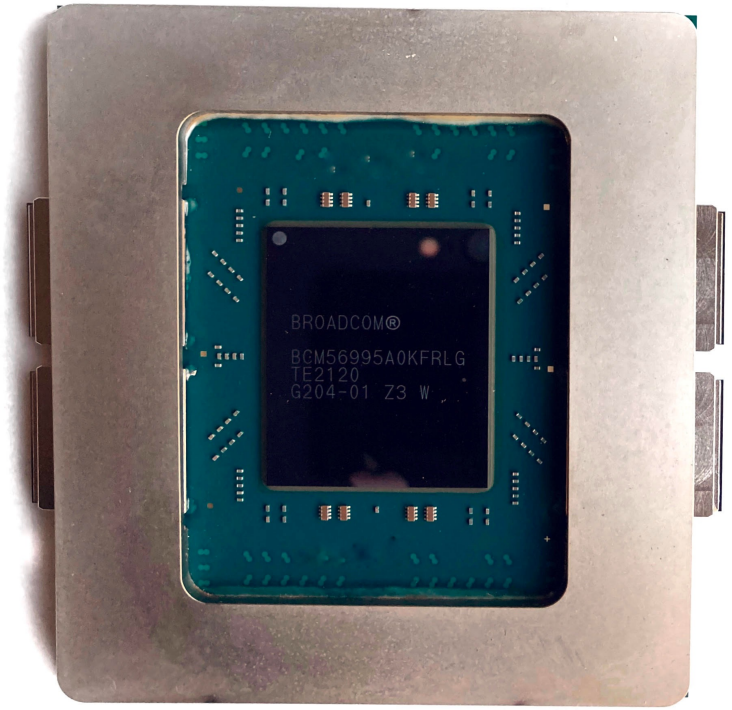
SCIP Integration Enables High Density System Design





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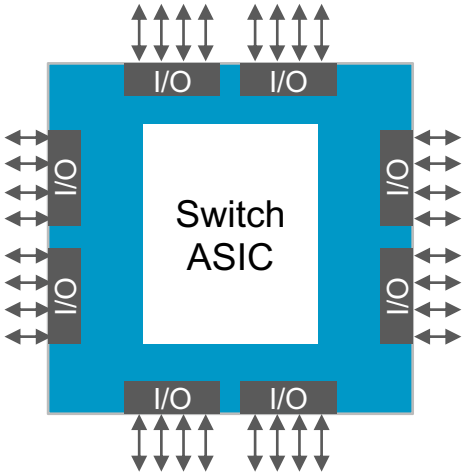
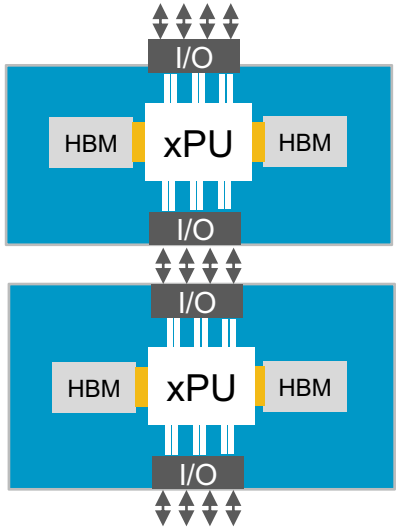
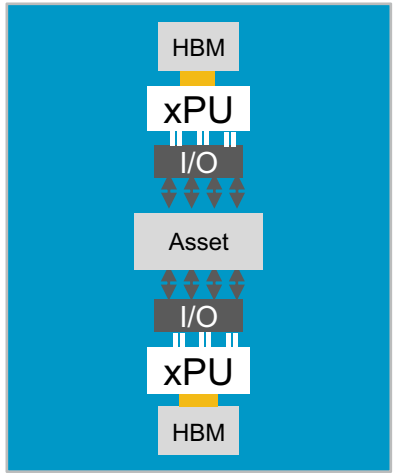
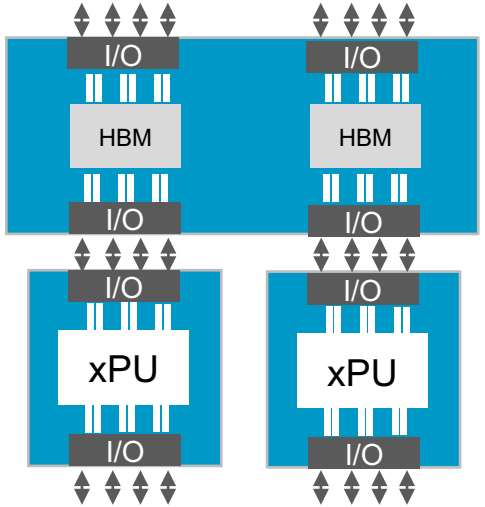
Architectural Migrations Enabled by SCIP I/O

	High-Density Switch interconnect	GPU to GPU Interconnect	Resource Pooling	Memory Disaggregation
				
Bandwidth	25.6-51.2Tb/s	2.4-4.8Tb/s	8Tb/s	8Tb/s
Power Density	< 10 pJ/bit	< 5 pJ/bit	< 5 pJ/bit	< 5 pJ/bit
Latency	µs	µs	µs	100s ns

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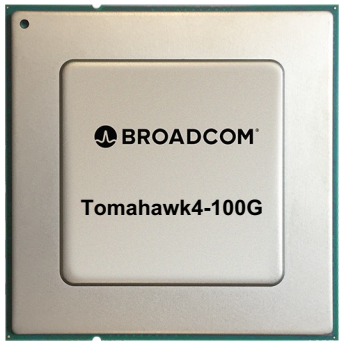
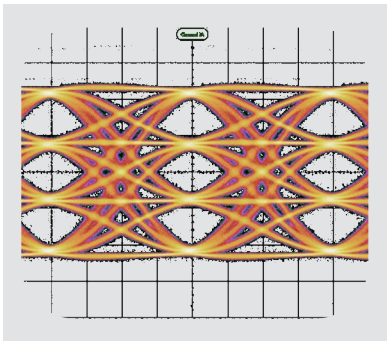
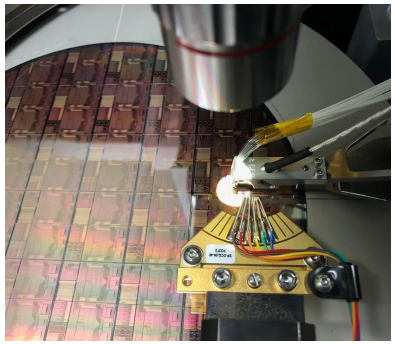
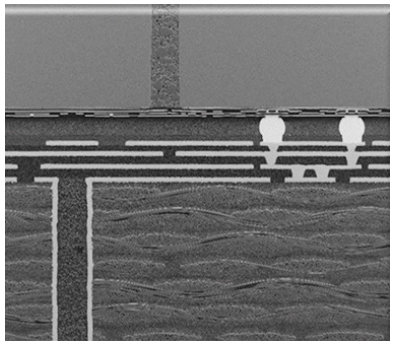
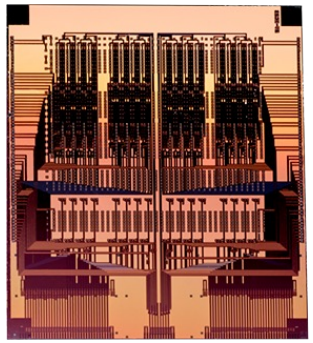
SCIP I/O Platform Building Blocks











ASIC Silicon	Mixed Signal IC	Optical Devices & Fabs	Advanced Packaging & Test	Silicon Photonics
• Core switch, SerDes and DSP in leading node • Sustained generational differentiation	• Power and performance optimized in both SiGe and CMOS	• 50M lasers/year from internal fabs • High-volume optical manufacturing • High-power, multi-wavelength sources	• TSV/2.5D/3D integration • CoW/CoC Assy • MCM Packaging • Reflow compatible optics assembly • Wafer-level test • Fiber Connector	• High-density Photonics Integrated Circuit (PIC) design • Modulators and PDs in silicon • Low-loss SOI waveguides

Key Technology Integration needs to maximize I/O efficiency

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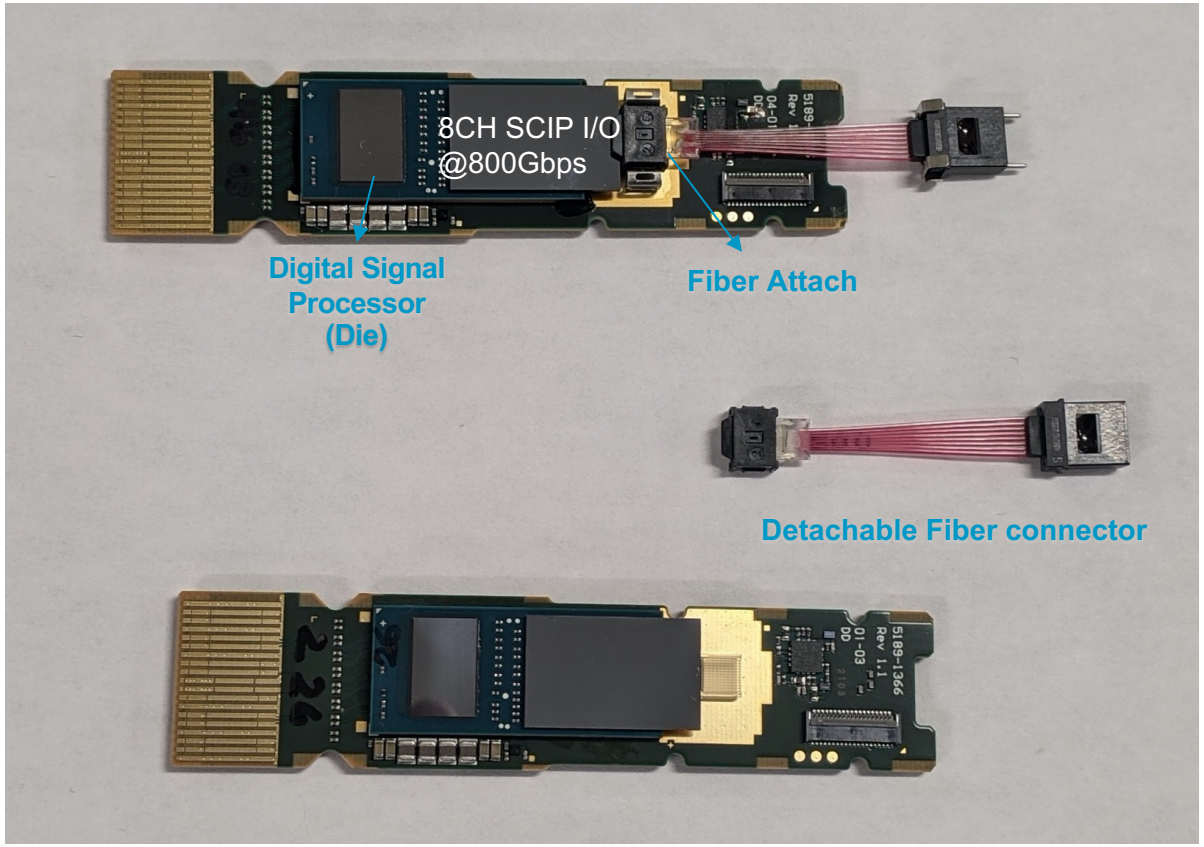
8CH SCIP I/O in a traditional transceiver form factor



- 8CH SCIP CPO in a Transceiver Module
- Silicon Photonics engine is co-packaged with a Digital Signal Processor die
- 100Gb/s Serial Interface between DSP and Silicon Photonics Engine Chiplet
- ~12mm x 26mm MCM Package
- Integrated laser with custom detachable optical connector interface
- 8CH SCIP based CPO is solder reflowed to the PCB demonstrating the reflow capability of Broadcom's optical I/O.

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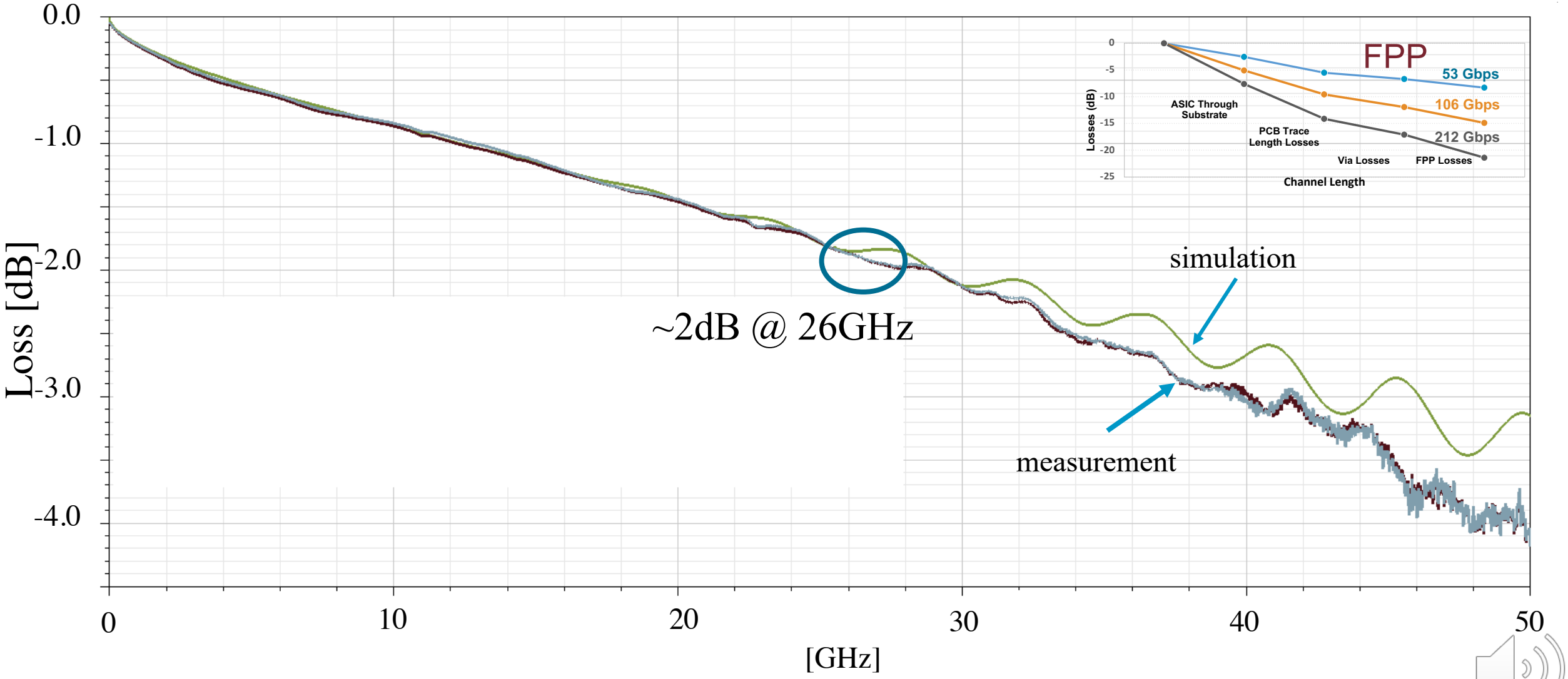
Channel Tx – Diff IL : 2dB for SCIP vs 16dB for an FPP



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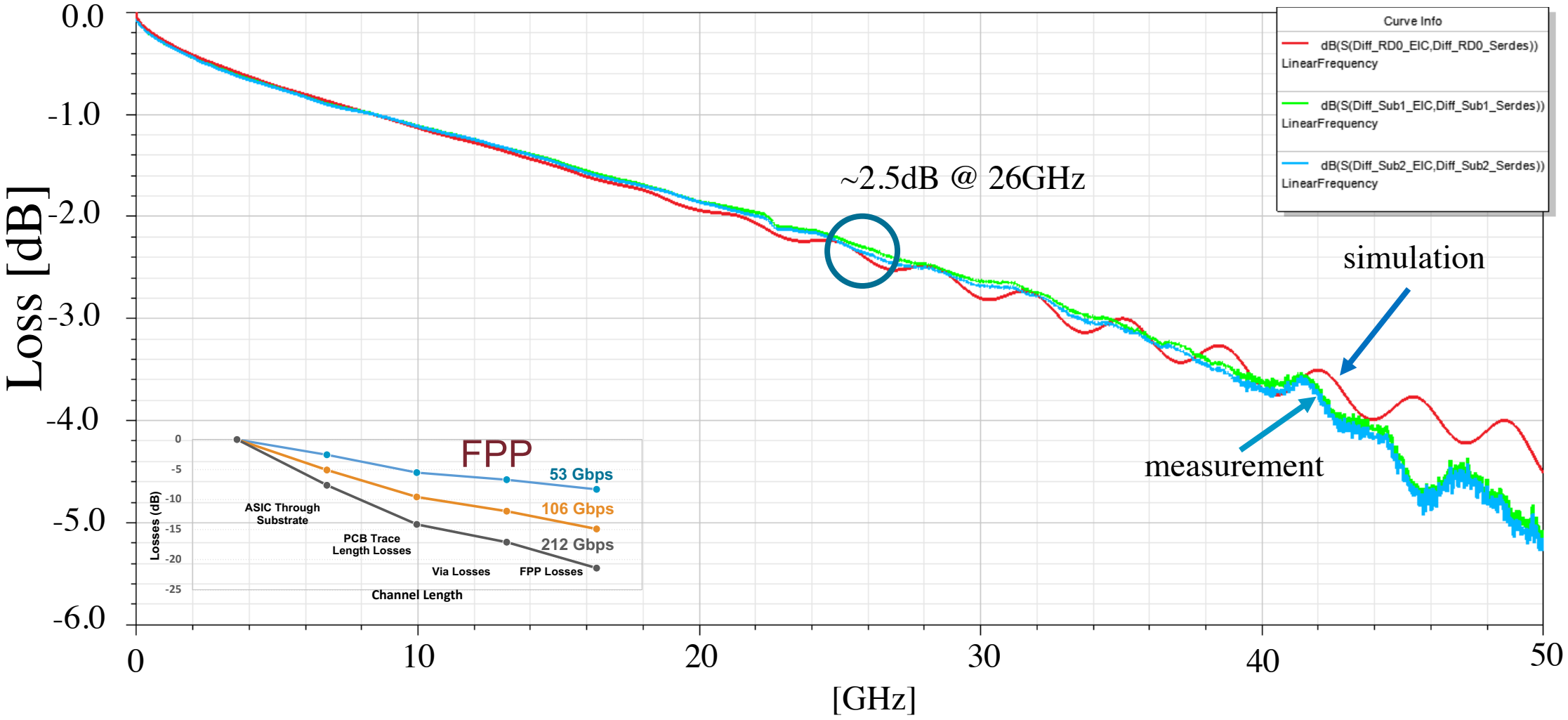
Channel Rx – Diff IL: 2.5dB for SCIP vs 16dB for an FPP



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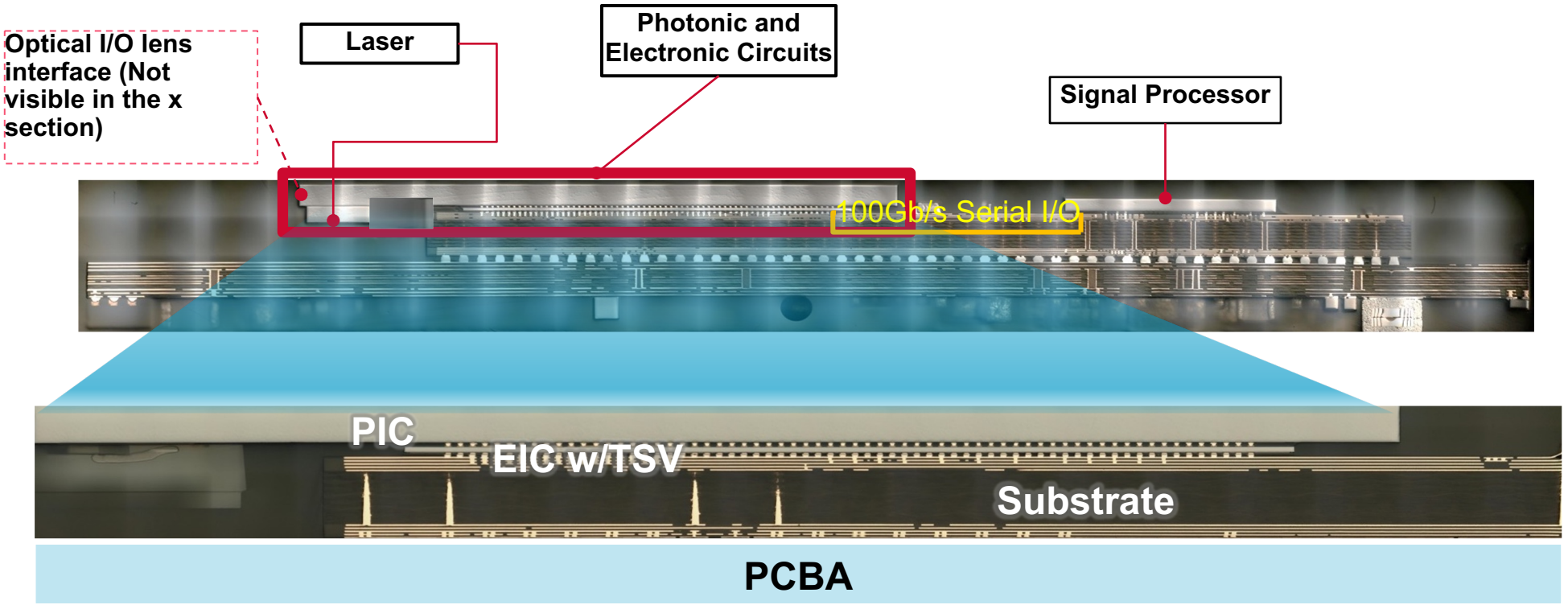
The Anatomy of a Fully Integrated 8CH Silicon Photonics Engine



Alexis Björlin, "Breaking the Bandwidth Barrier: Silicon Photonics Optical I/O", SEMI Americas Virtual Forum, 2021

- Digital Signal Processor with 8 x 100Gbps Analog Serial I/O to SCIP
- Silicon Photonics Chiplets in Package (SCIP) Include
  - Photonic Integrated Circuits (PIC) for optical light modulation and light detection
  - EIC w/TSV Chiplet for Electrical to Optical Conversion and Optical to Electrical Conversion
  - Laser for Optical power supply
  - Optical I/O lens interface for light coupling in and out of the detachable fiber connector

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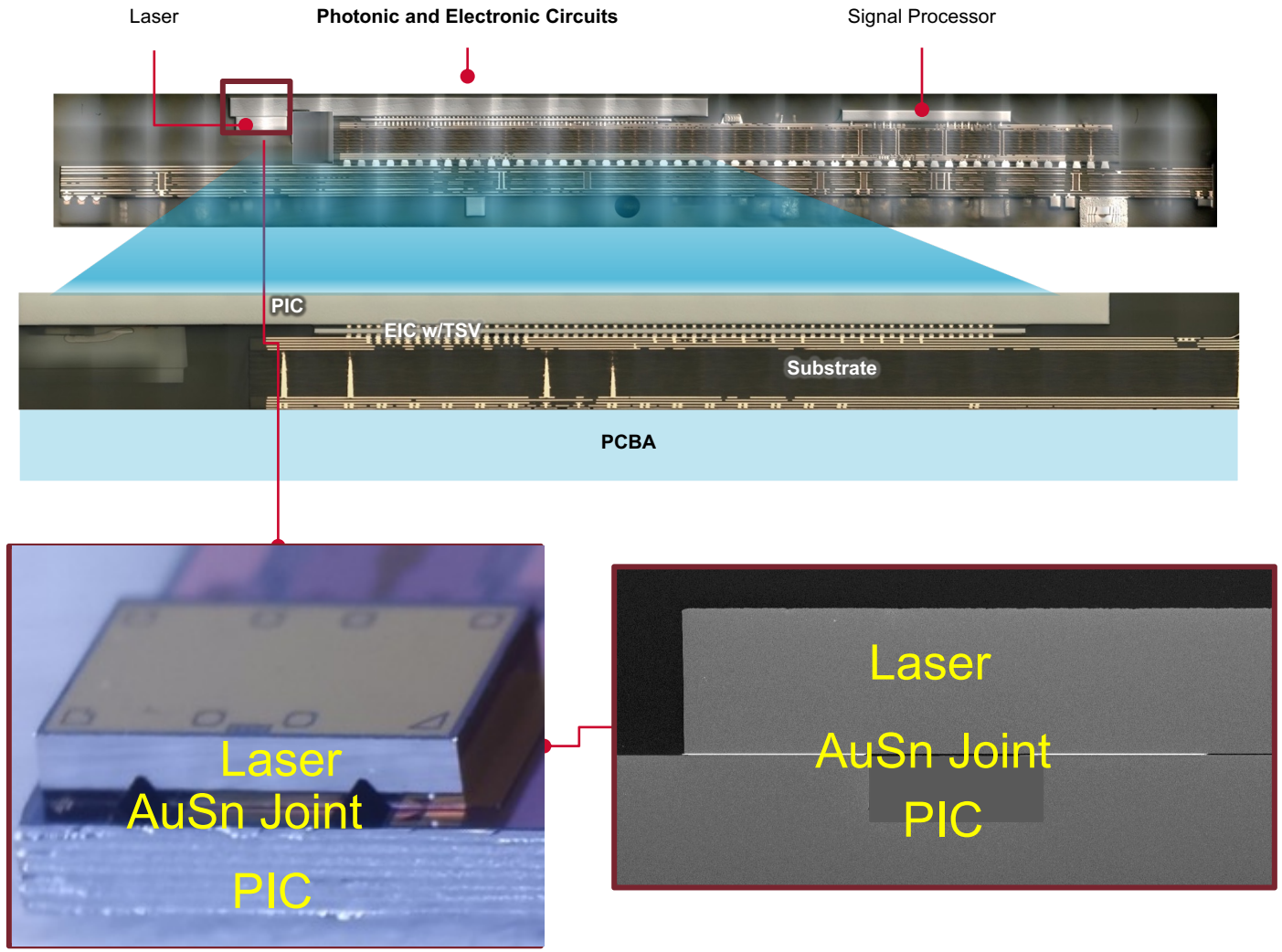
SCIP I/O: Advanced Packaging Technology Building Block

Laser Integration



- Hybrid Integration of III-V Laser on a PIC wafer
- Chip on Wafer of Laser to PIC wafer
- AuSn Eutectic bonding process

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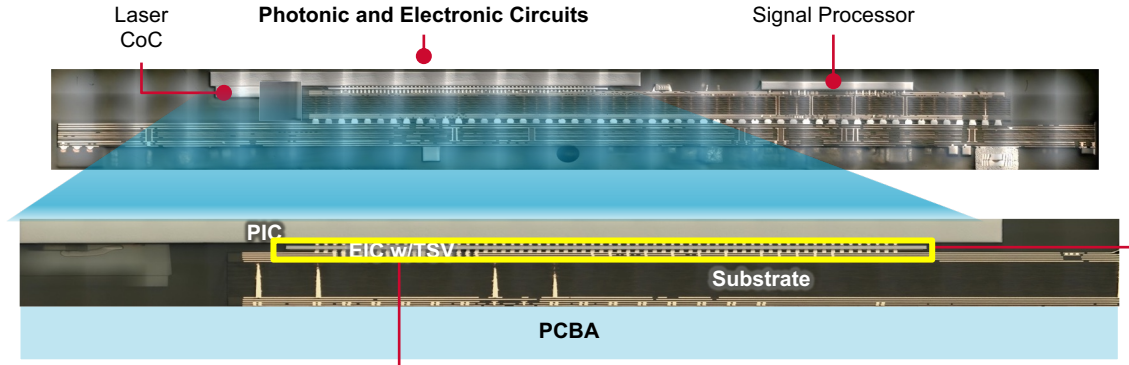
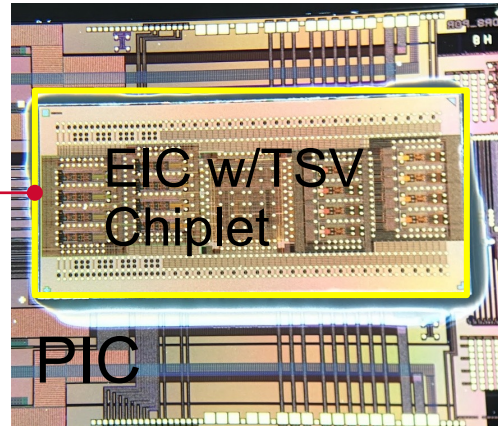
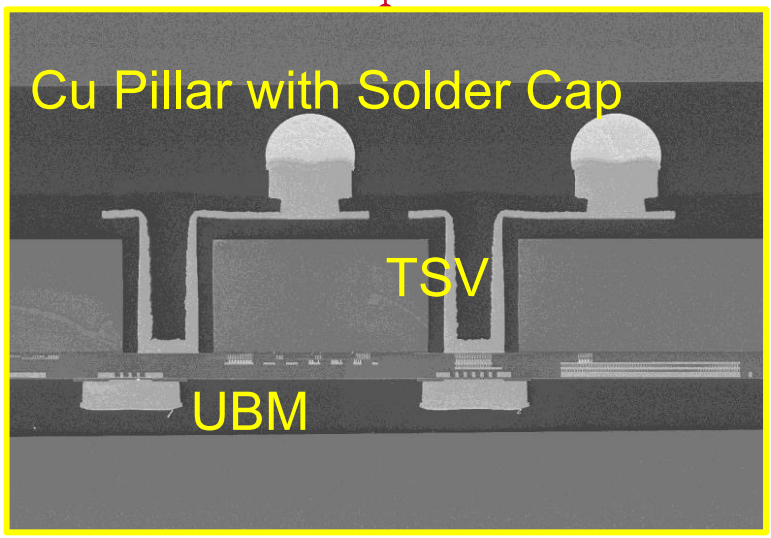
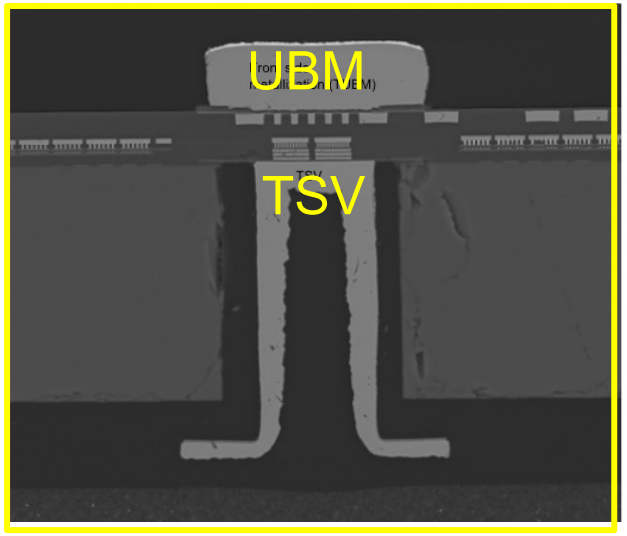
SCIP I/O: Advanced Packaging Technology Building Block

EIC w/ TSV Chiplet









- TSV Last Integration on BiCMOS wafer for 3D integration
- ~75 um thin wafer
- 1L RDL and Cu pillar w/ Solder Cap on one side and UBM on the other side

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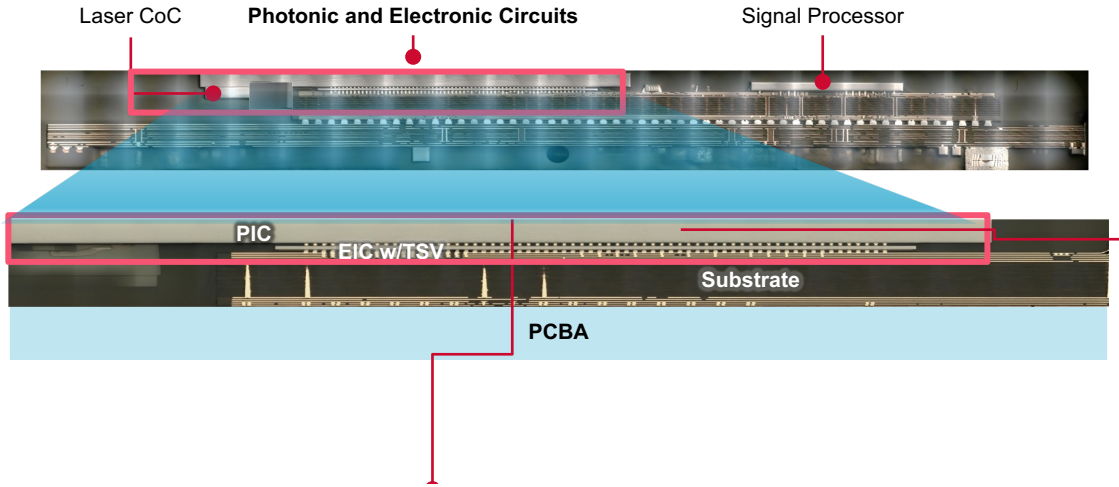
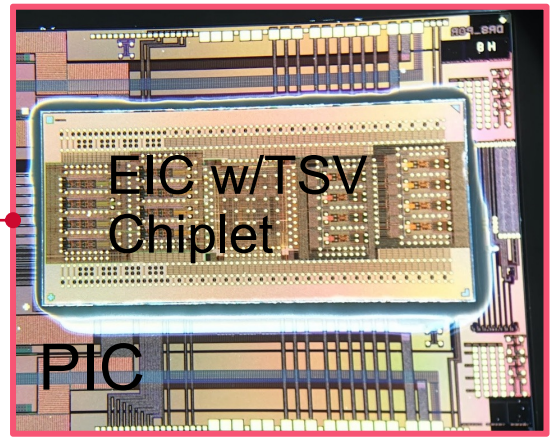
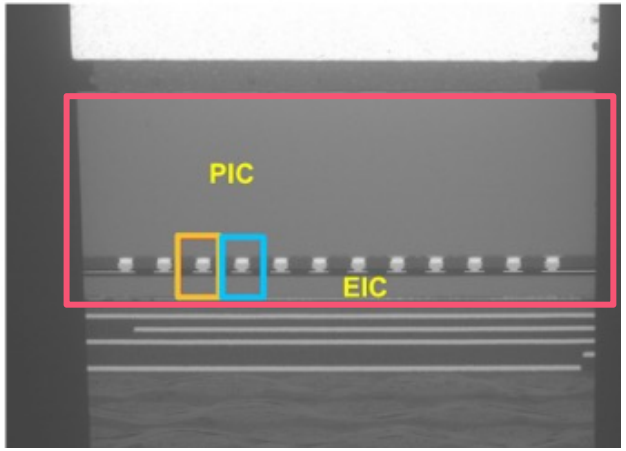
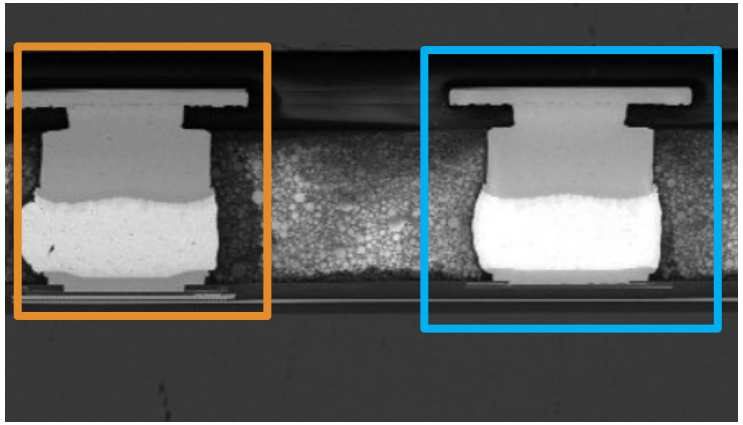
SCIP I/O: Advanced Packaging Technology Building Block

PIC-EIC CoC









- CoC bonding of EIC-PIC using TC-CUF Process to form a Silicon Photonics Engine Chiplet (SCIP I/O)
- 130um min bump pitch

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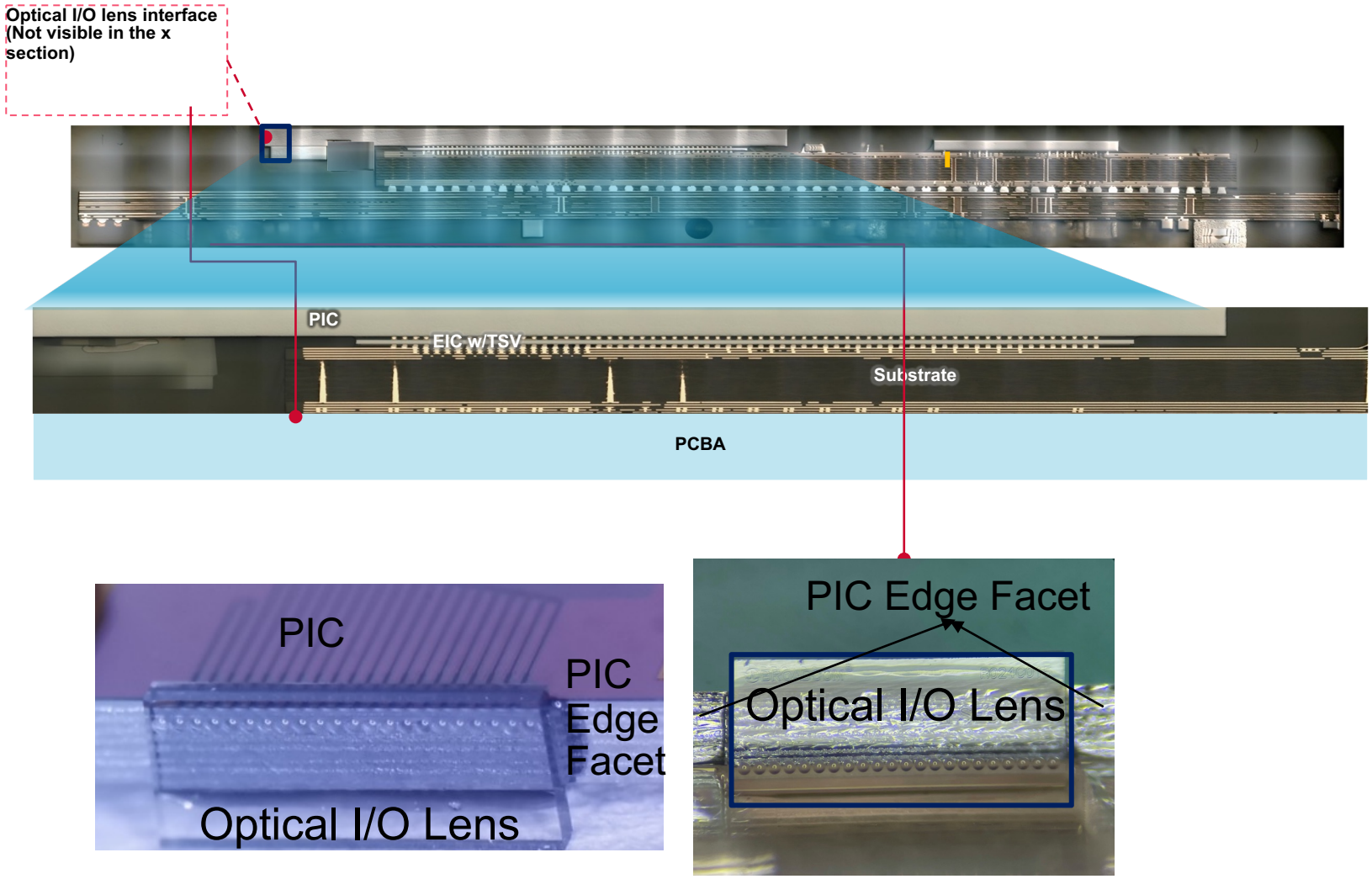
SCIP I/O: Advanced Packaging Technology Building Block

Optical I/O Lens



- Optical I/O lens assembled to PIC edge facet using Epoxy
- Light Coupling interface for fiber connector
- 127 um I/O Lens/ Fiber Channel pitch
- Reflow compatible optical lens assembly

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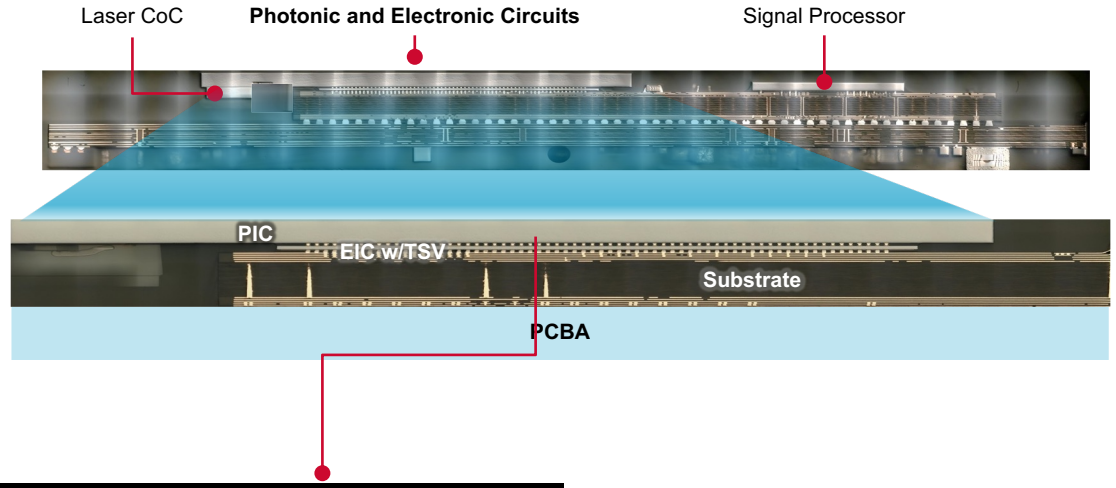
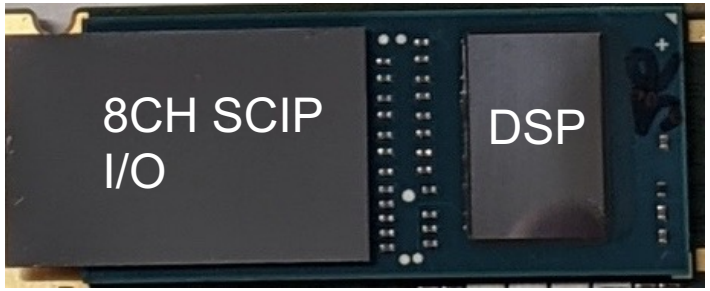
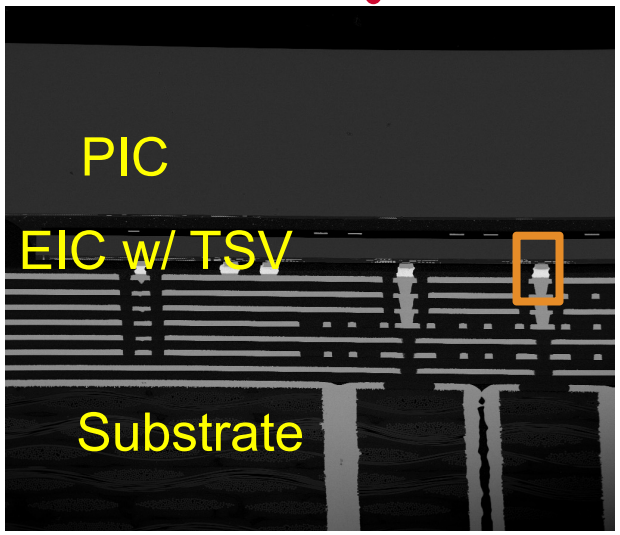
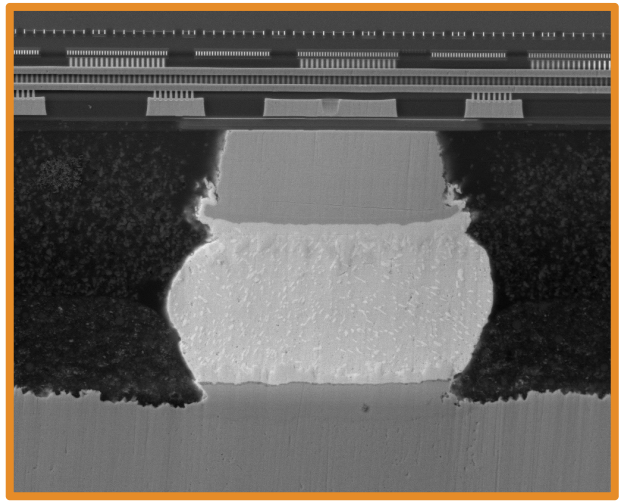
SCIP I/O: Advanced Packaging Technology Building Block: MCM Packaging

MCM Packaging









- Co-packaging 8CH Silicon Photonics Engine Chiplets with Digital Signal Processing (DSP) Chiplet
- 8 x 100Gbps Serial Interface between the DSP and SCIP
- 2 Die MCM Assembly using standard reflow process
- 150um min bump pitch

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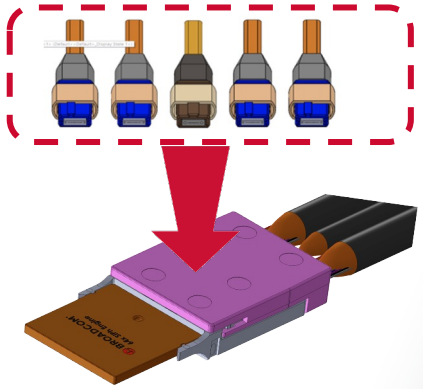
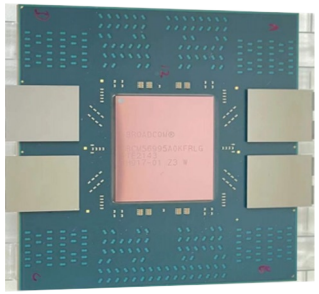
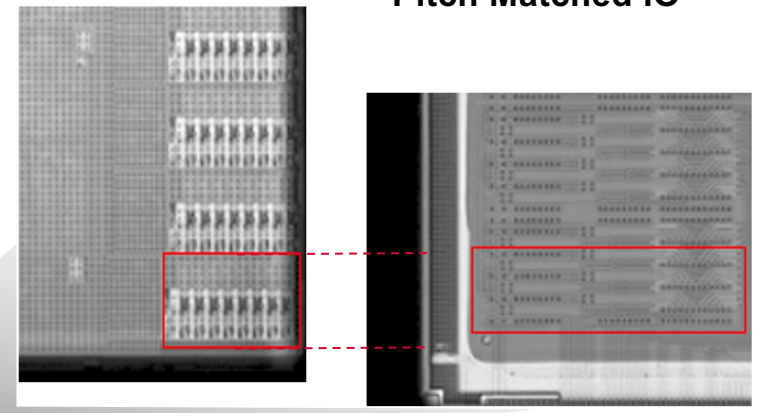
Scaling Core Technologies for 32CH SCIP in a 5 Die MCM

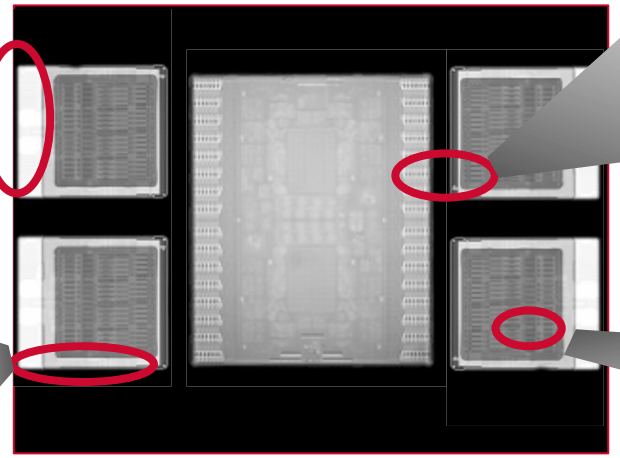
High Density Optical Connector

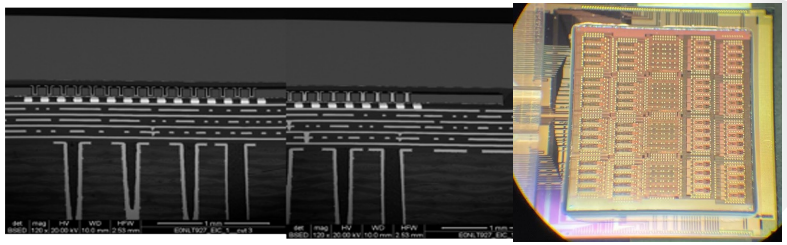




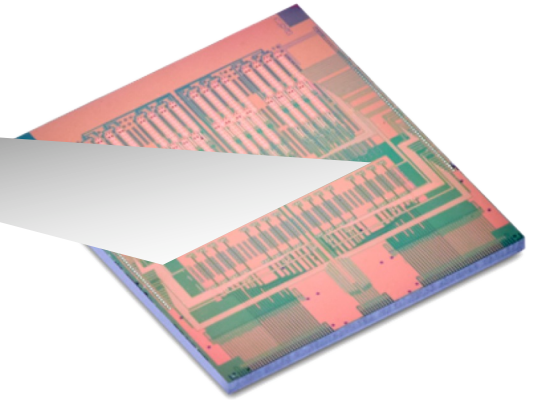
Pitch Matched IO







High Density Integration
(reduced Interconnect length)



High Density Optical Component

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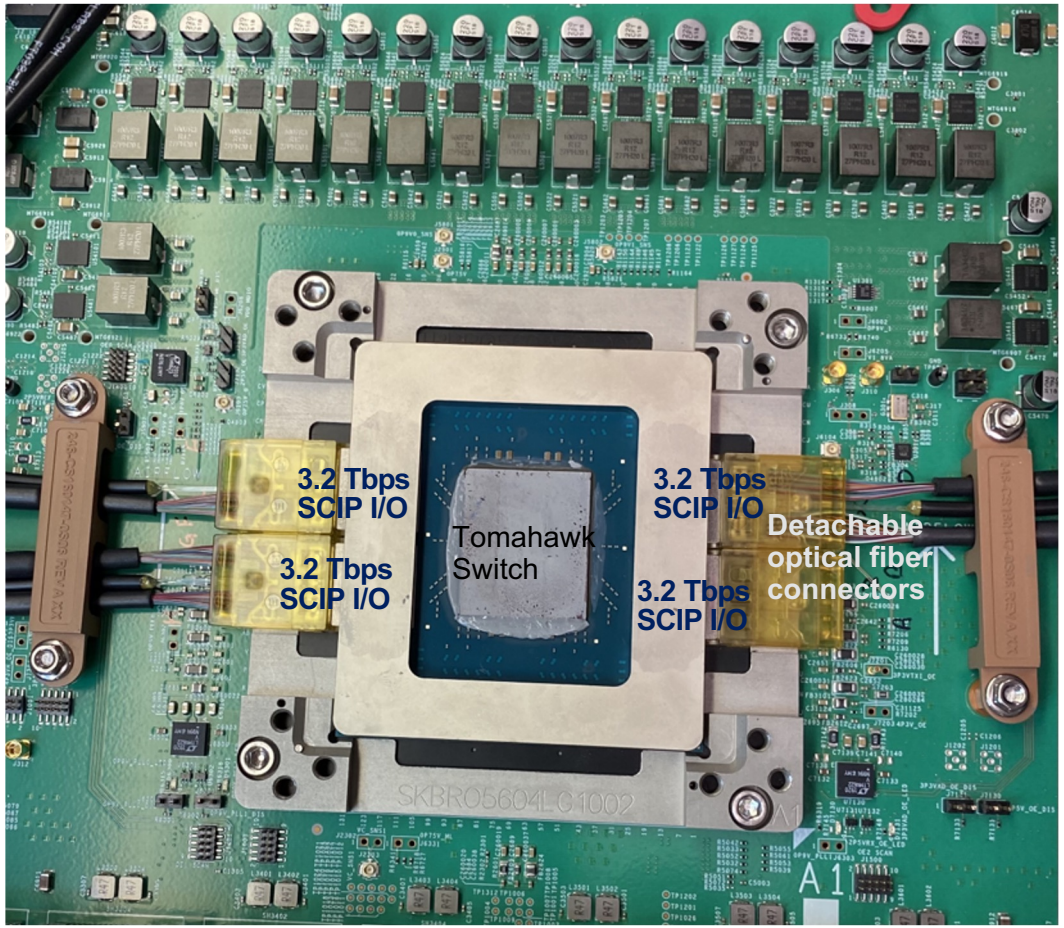
Platform Scaling to 128 CH using 4 x 32 CH SCIP I/O



- CPO Switch with 256 Channels of 100G Serial I/O in “Half Electrical I/O” and “Half Optical I/O” configuration with 128 Channels each
- 4 x 32CH Silicon Photonics engine is co-packaged with a Tomahawk4 Switch ASIC to provide optical I/O
- 67.5 mm x 75mm MCM Package
- External Laser Providing Optical Power to Silicon Photonic chiplets
- Detachable Fiber connectors with 3 different fiber types for Tx, Rx and Laser

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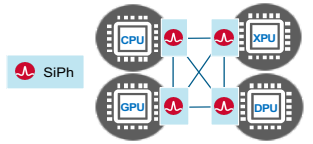
Scaling SCIP I/O based CPO

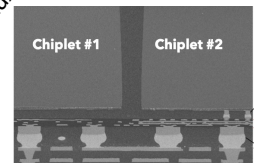
SCIP CPO with integrated SiPh offers 3 independent vectors for scaling:
- **Integrated λ mux/demux**
- **Electrical I/O density scaling with advanced packaging**
- **Power-Performance-Area scaling w/ CMOS node**

I/O Efficiency (Tbps /mm)/(pj/Bit)



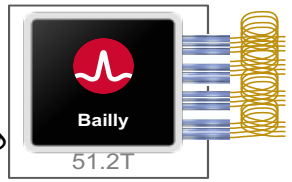
XPUs w/ Optical IOs

Optical IO density scaling with λ mux/demux



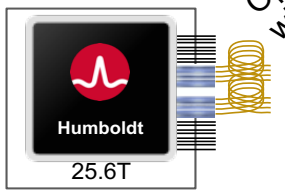
Electrical IO scaling with **CMOS node** and Advanced Packaging

CMOS w/ Electrical I/O



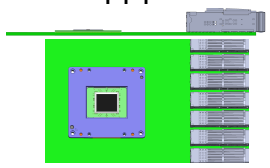
CMOS w/ Optical IOs (CPO Gen 2)

Optical IO density scaling with λ mux/demux

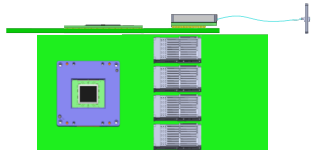


CMOS w/ Optical IOs (CPO Gen 1)

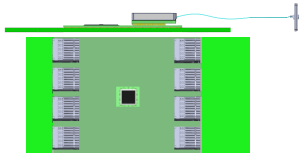
FPP



OBO



NEXT GEN OBO



Vivek Raghunathan, "Data Center Requirements and Technology Roadmap Panel Discussion," *OIDA Workshop on Developments in Co-Packaging Technologies for Data Centers,* 30 March 2021, online.

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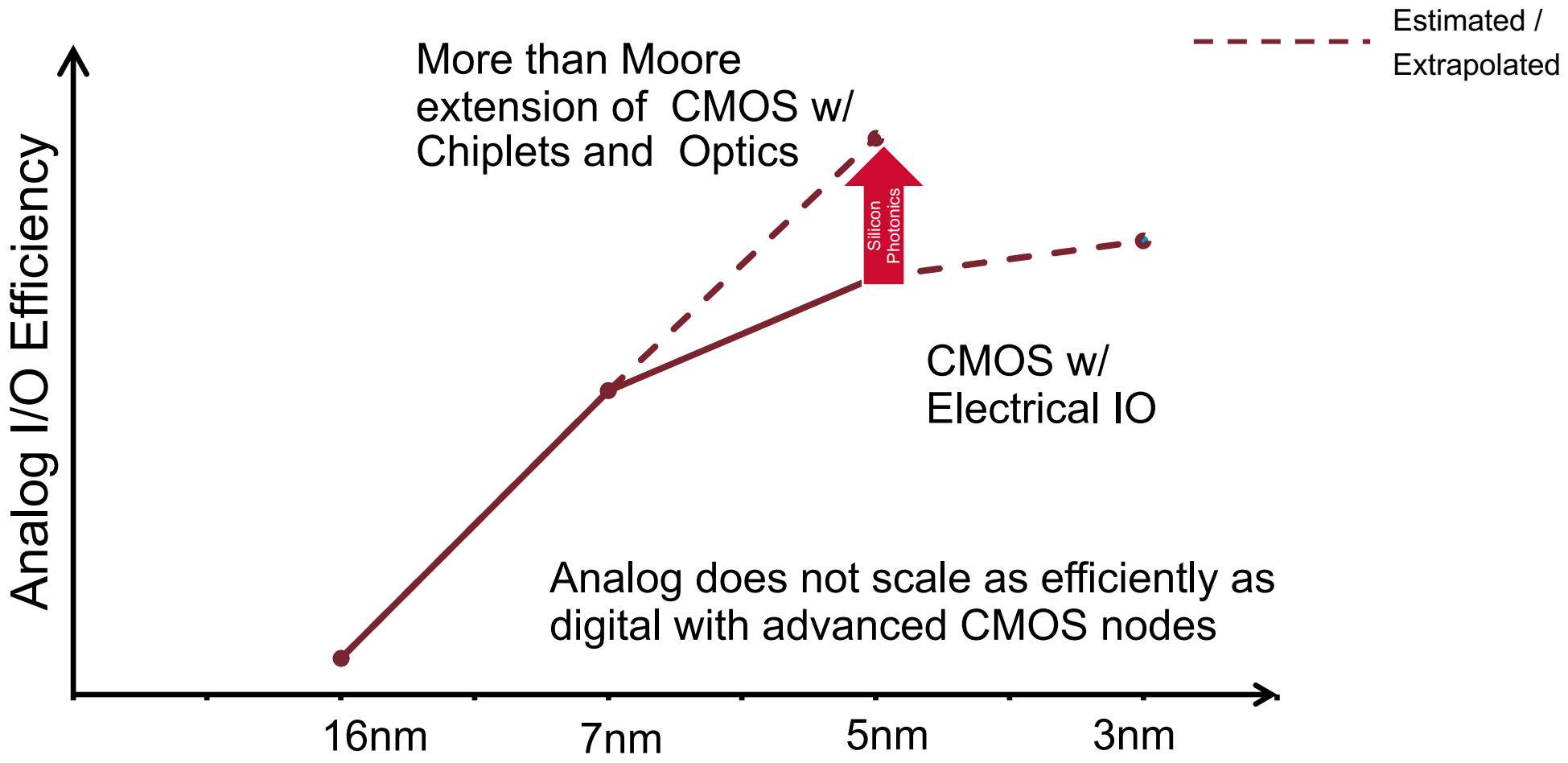
SCIP Leading ‘More than Moore’ CMOS IO Scaling



Silicon Photonics platform provides “More than Moore” approach to improve Analog I/O efficiency

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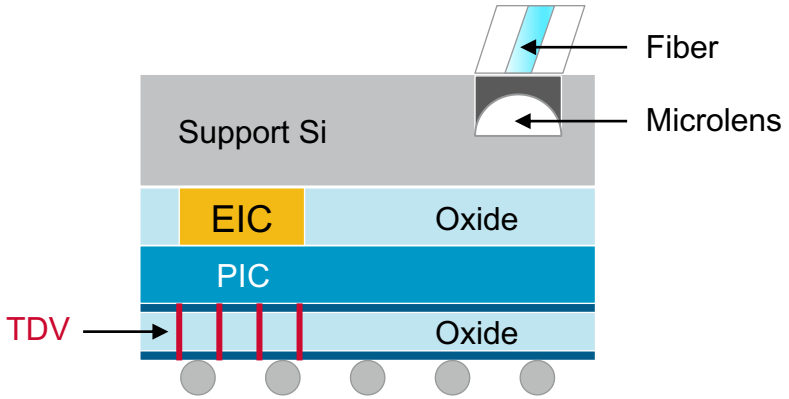
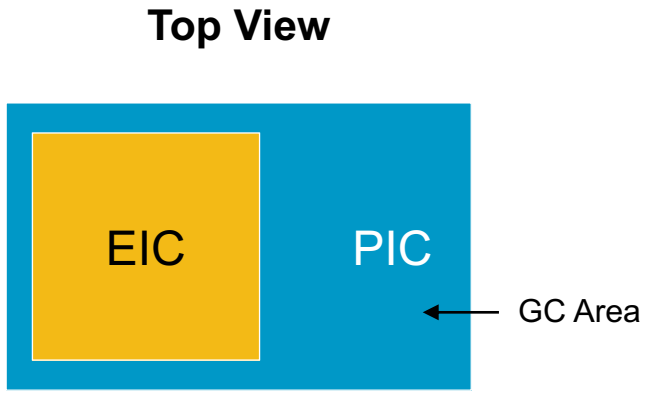
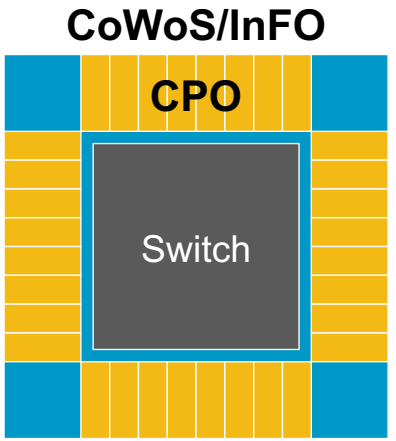
Silicon Photonics Packaging– Foundry Investment Trends

- Low insertion loss SoIC interface (hybrid bonding) between EIC/PIC & TDV (through dielectric via) in PIC
- Exciting development and investment in chip stacking – wafer to wafer and chip to wafer bonding





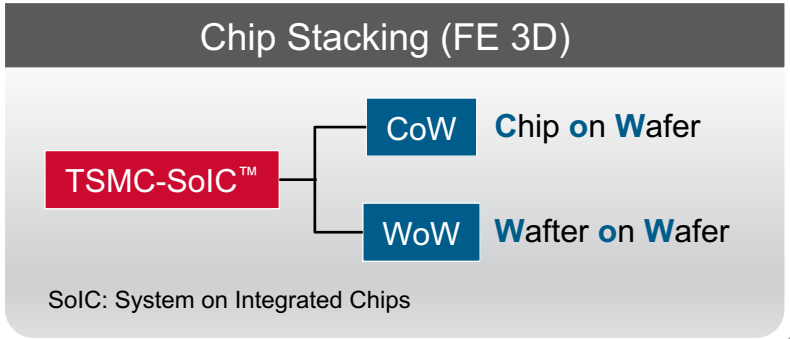


Source: TSMC – Hotchips 2021

GlobalFoundries, Arm Close in on 3D Chip Integration ›3D interconnects could shorten delays within processor cores

BY SAMUEL K. MOORE | 20 AUG 2019 | 3 MIN READ |

Source: GF – Face-to-face Hybrid Wafer Bonding



Source: TSMC – 3DFabric

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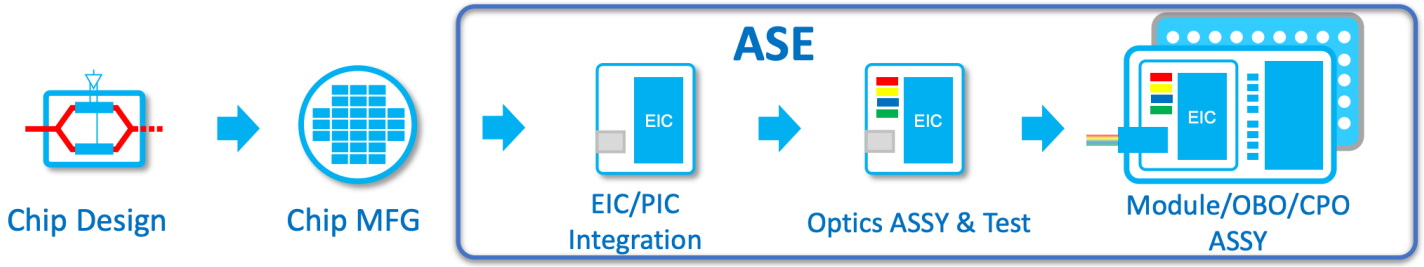
Packaging is King – Silicon Photonics OSAT Investment Trends

- OSATs increasing investments in processes specific to optical chiplet packaging
- Examples: KOH V-groove, fan-outs, fiber attach



Post-CMOS Process

- Cu-pillar bumping
- UBM metallization
- WL dam process
- Oxide etching & DRIE
- Au mirror process
- AuSn process
- ARC film process
- KOH V-groove
- Via last process
- Fanout process

Wafer Level Assembly

- CoW process
- Wafer level WB assembly
- High accuracy laser attachment
- Optical components placement

Wafer Level Test

- Wafer sorting
- Probe card design
- Test program service
- WL optical test

oEngine Assembly

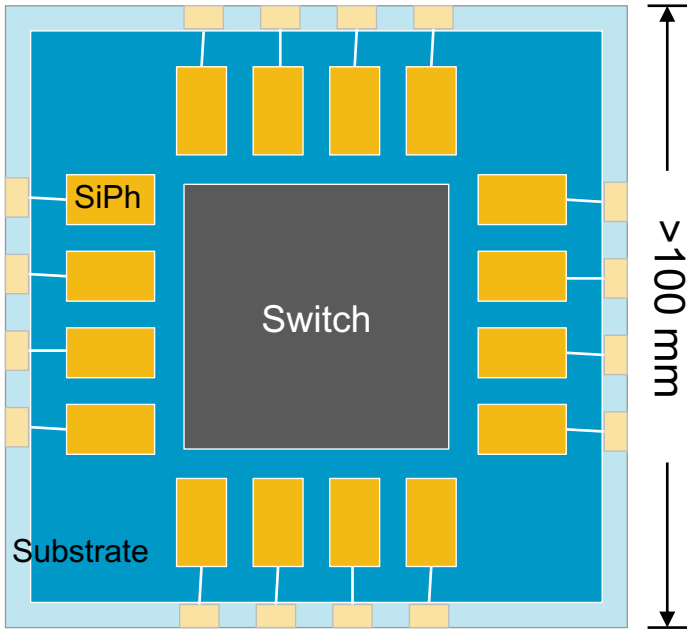
- SMT process
- Substrate level FC/WB
- Encapsulation
- Fiber attachment
- Housing assembly
- Module test

Lab Service

- Electrical/Optical
- Thermal/Stress
- Material/Chemical/FA

Blue = Specific for optical packaging

Integrated on Substrate



Co-package Optics

Source: ASE – EPIC 2020

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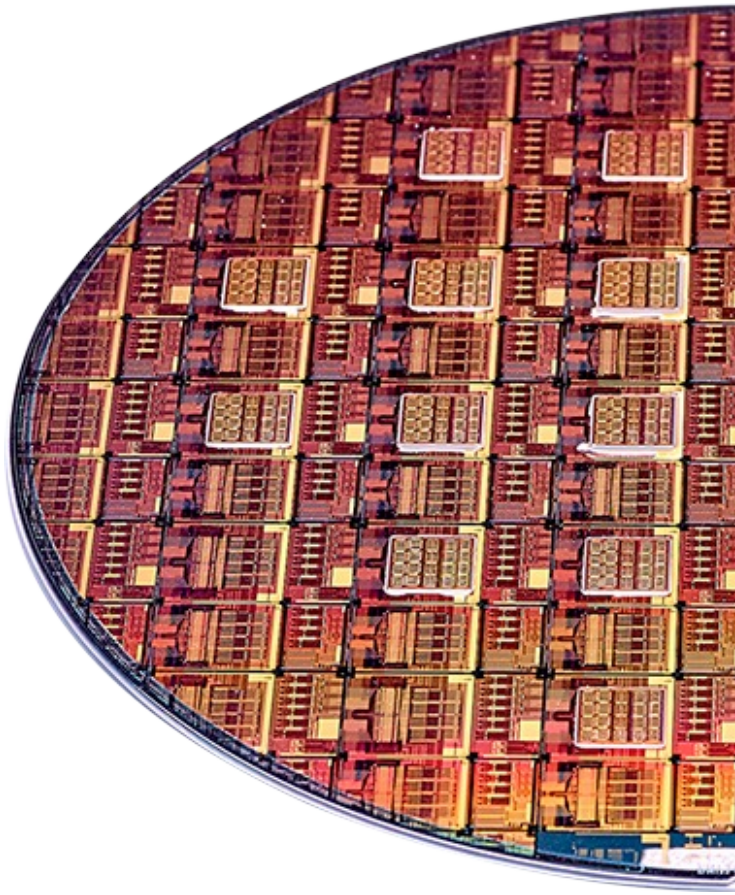
Summary and Ecosystem Call-to-Action

- SCIP based CPO with integrated silicon photonics provides a step improvement in I/O efficiency of next gen high speed interfaces
- Chiplet ecosystem partner investment in Foundry, EDA, Assembly and Test is crucial
- SCIP platform can scale to serve the I/O needs beyond ethernet switching to next generation compute and memory system connectivity



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