Advanced Packaging Technology for High Density Silicon Photonics Transceiver Engines

Peter De Dobbelaere
Cisco Systems, Inc.
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Overview

- **Silicon Photonics Technology**
- History & Outlook for Intra Datacenter Interconnect
- Requirements for Future Silicon Photonics Solutions
- 3D Silicon Photonics
- Summary

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Silicon Photonics

The Promise

- Leverage IC industry design, manufacturing and test methods/infrastructure
- Advanced photonic device libraries (high efficiency, high BW)
- Seamless integration with electronics by mature 2.5 & 3D technology
- Power of integration (functionality & density)
- Enables highly automated assembly
- External modulation:
  - High fidelity modulation relative to directly modulated laser diodes (DML)
  - Enables remote light sources (RLS)

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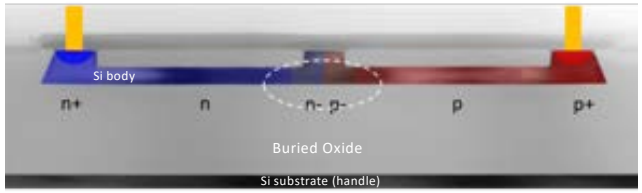
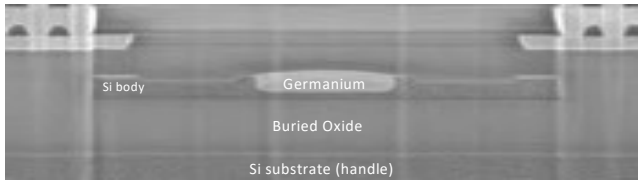
The Challenges

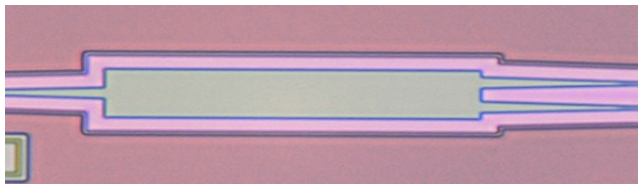
- Coupling of light in/out of Si chip:
  - Grating couplers: Low loss, relatively easy to integrate, high density (2D), but limited optical wavelength bandwidth
  - Edge coupling: Low loss, more complicated to integrate, density limited (1D), broad optical wavelength bandwidth
- Light source integration:
  - No native light source solution
  - Multiple solutions developed: heterogeneous, FC,…
- Low wafer volume compared to electronics:
  - Need suitable business deal for foundries/fabs
  - Mitigation: Enable multiple products from technology platform
- Longer design cycles:
  - Photonic and electronic IC design are concurrent
  - Mitigation: Enable multiple products from single mask set/technology node

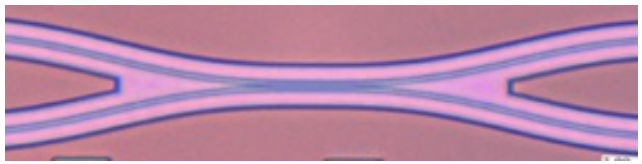
Silicon Photonics Technology: Integrated Optics

- Silicon Photonics wafer foundry:
  Currently Cisco/Luxtera uses TSMC as foundry for silicon photonic wafers for multiple transceiver products
- Key process attributes:
  - Fine CD etch for various passive optical structures
  - Ge epi for high BW photodetectors
  - Implants for active devices
  - 6 metal layer BOEL + TSV
- Advanced library of photonic devices:
  Carrier depletion/injection modulators, grating couplers, low loss waveguides, high responsivity & BW photodetectors, precision taps,…
- Process & Library maturity:
  Qualified and in full production mode: in-line metrology in place, agreed upon E/O-WAT tests for silicon photonic wafers
- Advanced Photonic PDK:
  Device library, layout, DRC, LVS, behavioral models for full link corner simulation (process, T, voltage,…)









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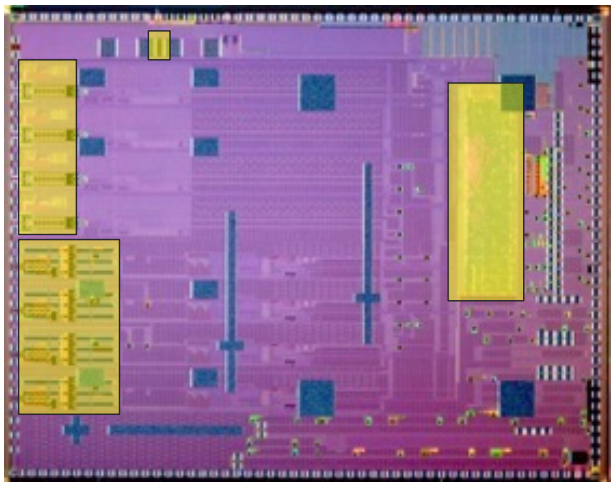
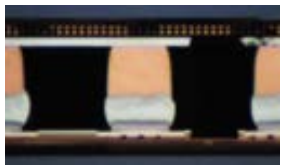
Integration Photonics & Electronics



Monolithic Photonic-Electronic IC (4x14 Gbps)

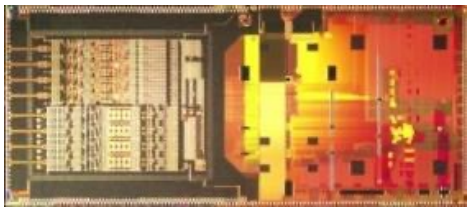
Electronic IC

+

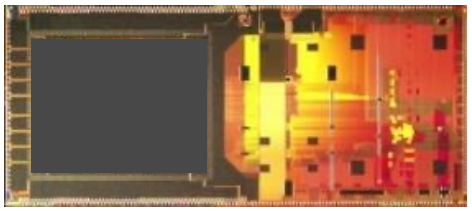


Micro bumps

+



Photonic IC



Hybrid Electronic + Photonic IC (4x25Gbps)

We commercialized both monolithic and hybrid integrated products, each approach has its merits and challenges:

- Monolithic: Less assembly steps (+), low interconnect parasitics (+), development cost (-), non-standard E-PDK (-), product cost
- Hybrid: Platform development cost (+), business/supply chain considerations (+), interconnect parasitics (-)

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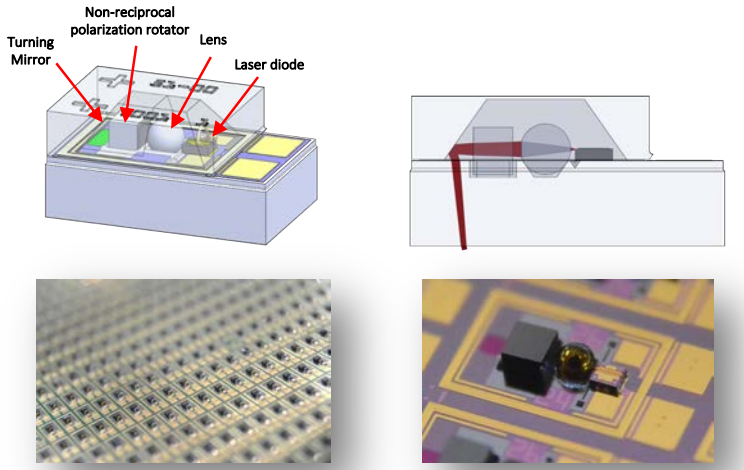
Light Source: Laser Micro-Package (LaMP)

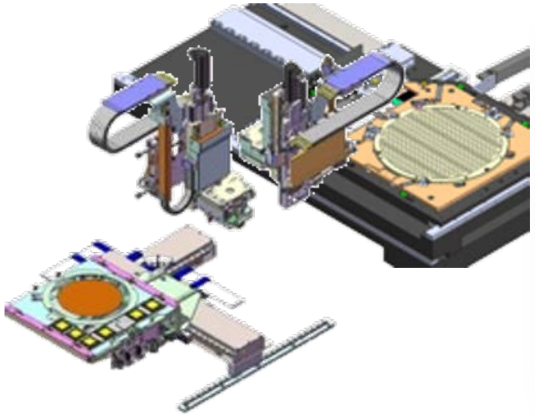
Miniaturized hermetic package for laser diodes:

- Use of conventional InP DFB laser diodes
- Integrated with coupling optics and optical isolation
- Suitable for coupling into silicon photonics die by surface coupling (grating coupler)
- Wafer level assembly, test and burn-in



Alignment & Attachment Known Good LaMPs on CoW:

- Fully automated wafer level process with mapping
- Active alignment using features in the Si P chip
- Attach is by heat curing adhesive: local heating for adhesive curing by laser illumination from the back of the wafer



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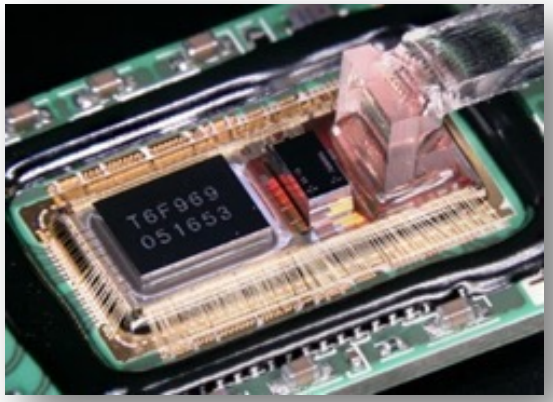
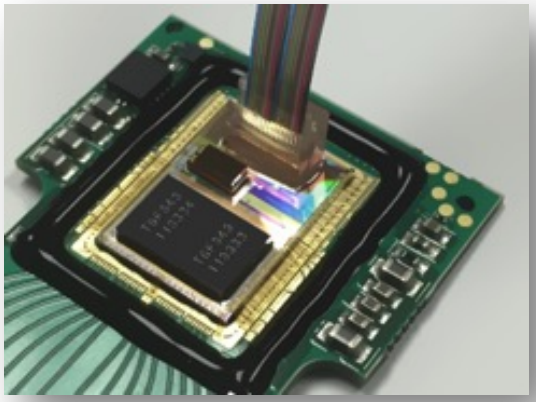
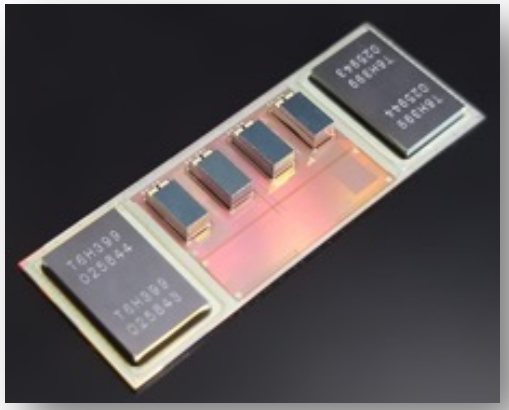
Silicon Photonics Chipsets (25 Gbaud NRZ)



100G (4x25Gb/s)



200G (8x25Gb/s)



400G (16x25Gb/s)

Photonic IC PIC25G / luxtsv:

- Modulators + controls
- Photodetectors (high-speed + monitor)

Electronic IC (N28):

- Electrical interfaces (CTLE/CDR/…, 2-wire low speed)
- Modulator drivers/TIA
- MCU, …

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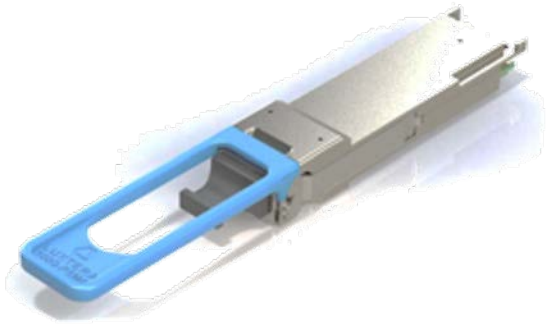
Light source:

- Laser MicroPackage (LaMP)
- Wafer level assembly, test and burn-in
- LaMP delivered to chipset line as KG device

Test strategy:

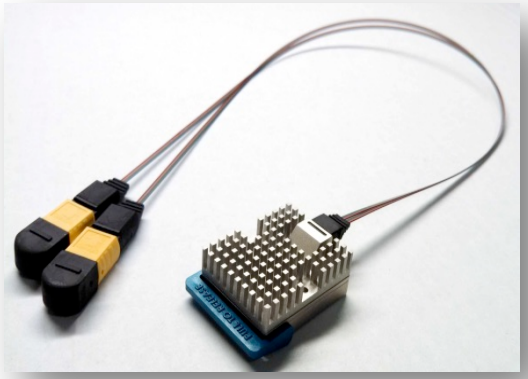
- KGD approach
- BIST & diagnostics built into photonic and electronic IC
- Chipset delivered to module assembly line as a KG element

Silicon Photonics Modules (25 Gbaud NRZ)



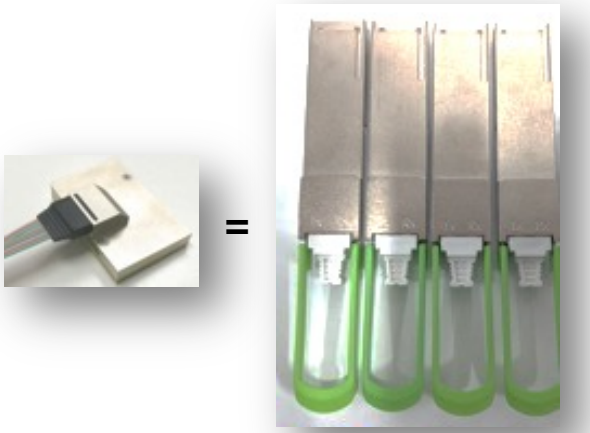
100G (4x25Gb/s) QSFP28 Module (PSM4 & CWDM4)

- MSA compliant module
- Multiple millions shipped
- Field proven high reliability
- Low profile fiber array for optical interface



200G (8x25Gb/s) OBO Module

- Custom On-Board-Optics module
- Optical I/O PSM4 MSA compliant
- Single light source for eight 25 G channels
- Fiber array for optical interface



400G (16x25Gb/s) OBO Module

- Custom On-Board-Optics module
- Custom Optical I/O
- Fiber array for optical interface
- Reduced formfactor (~4.5x): same functionality as 4 QSFP28 modules

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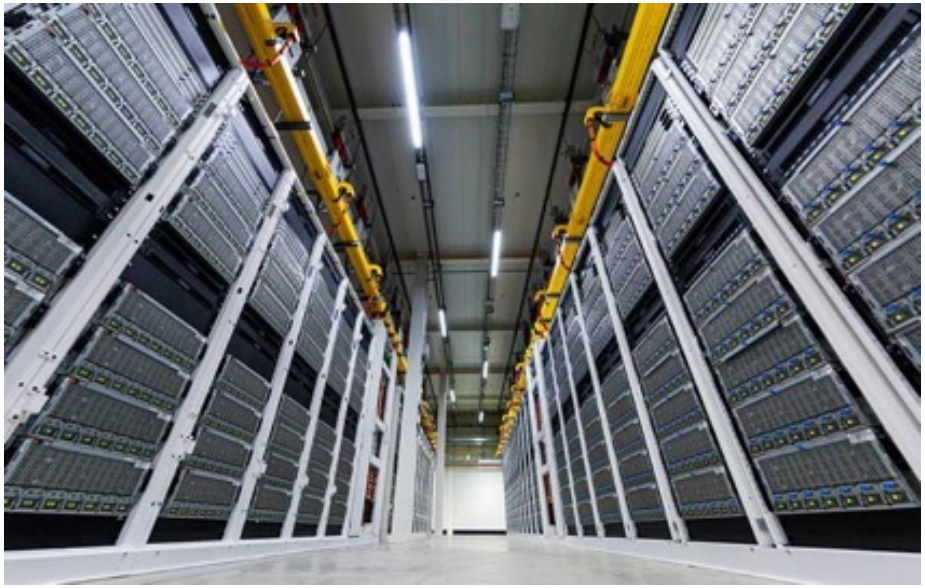
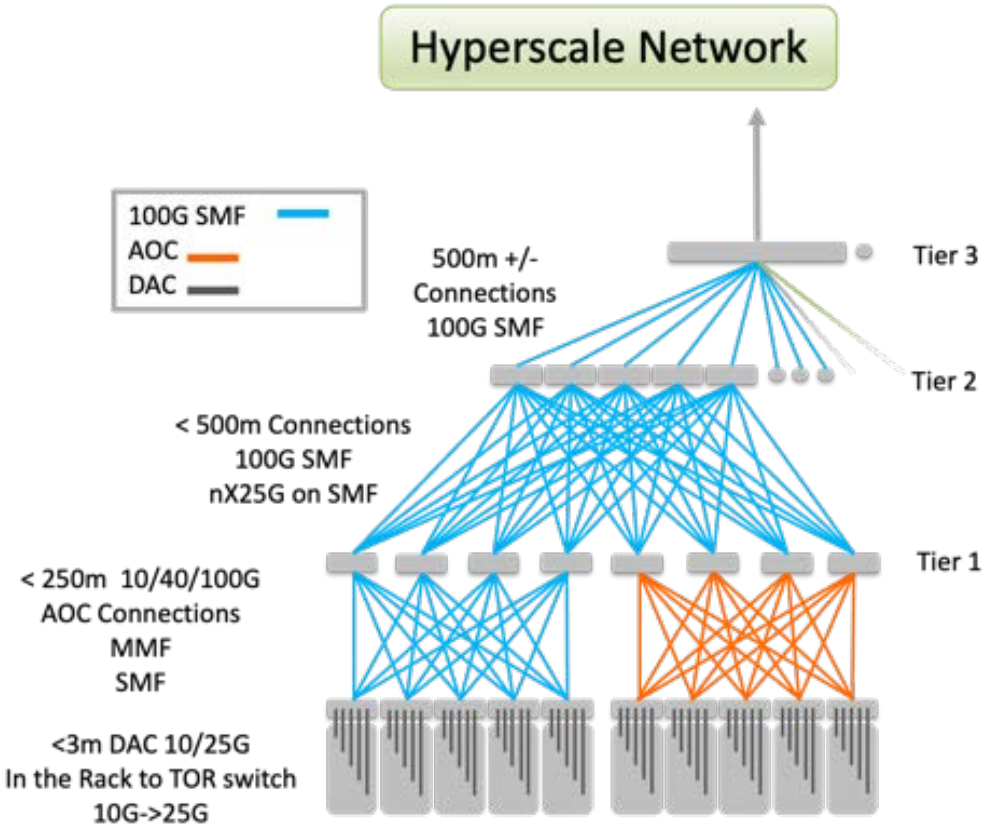
Hyperscale Datacenters



> 100,000 Servers

> 10,000 Switches

> 1,000,000 Optical Interconnects



Need for low-cost single-mode fiber interconnect initiated first high-volume deployment of silicon photonics transceivers.

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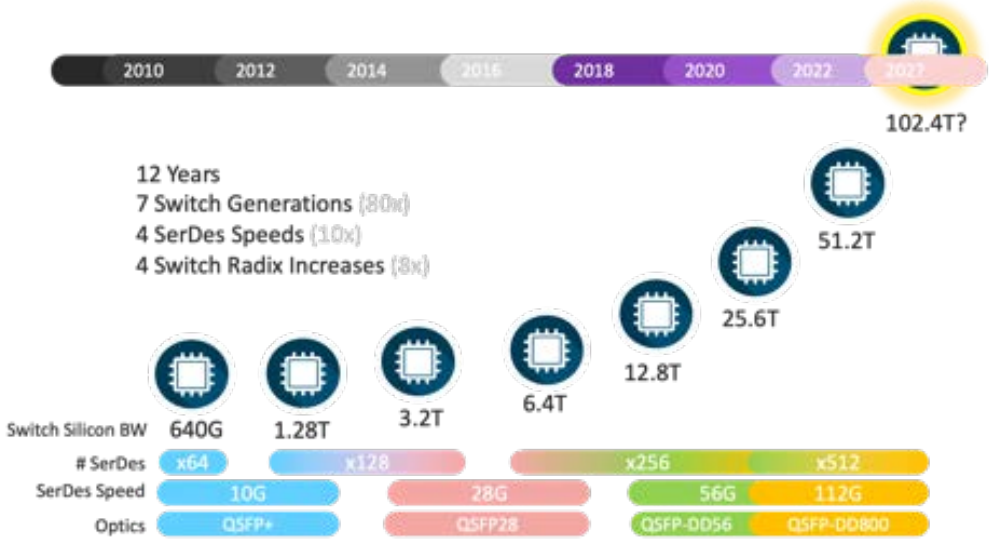
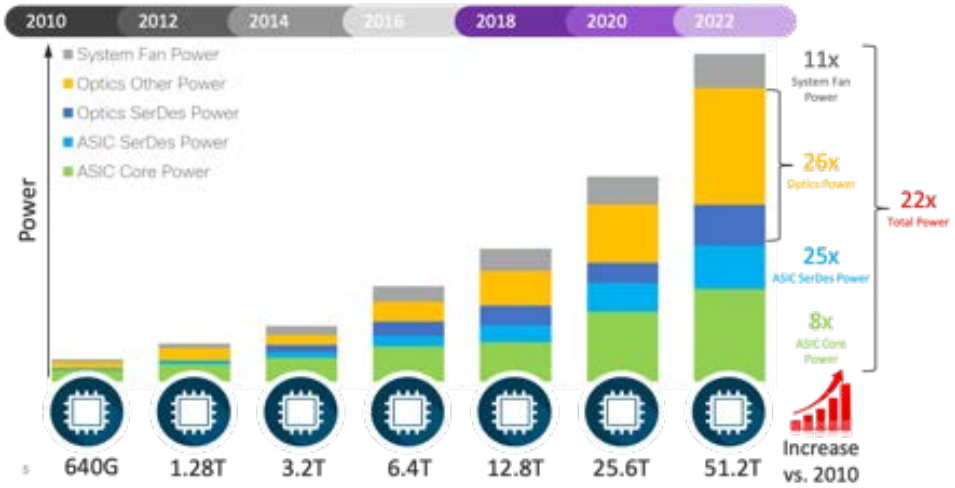
Trends in Ethernet Switching & Interconnect

Relentless increase in bandwidth



Growing power dissipation



80x increase in BW over 12 years

22x increase in power over 12 years

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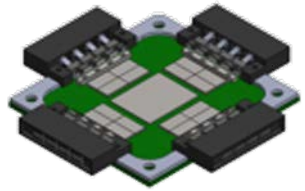
Optical Transceiver Rates and Implementations

- Evolution of data rates per lane IMDD (intensity modulation direct detect)

	100G/L	200G/L	400G/L
Final Standard‡	2017	≤ 2024	~ 2027
PMD Types	400G-DR4(+) 400G-FR4 400G-LR4	800G-DR4(+) 800G-FR4(+)	1600G-DR4(+) 1600G-FR4(+)
Modulation	53GBD-PAM4	112GBD-PAM4	224GBD-PAM4 (?) or 180GBD-PAM6 (?)
Analog BW (GHz)	40	85	170
Receiver Sensitivity (dBm)†	-4.6 dBm	≤ -3.6 dBm (?)	≤ -3.6 dBm (?)



‡ First samples usually lead final standard by 1-2 years
† For 2km WDM4 solution, measured at module compliance point

- Coherent modulation becomes attractive for reaches > 10 km
- Front pluggable modules remain the most attractive transceiver form factor. Key purpose of near-packaged and co-packaged solutions is to reduce power dissipation.

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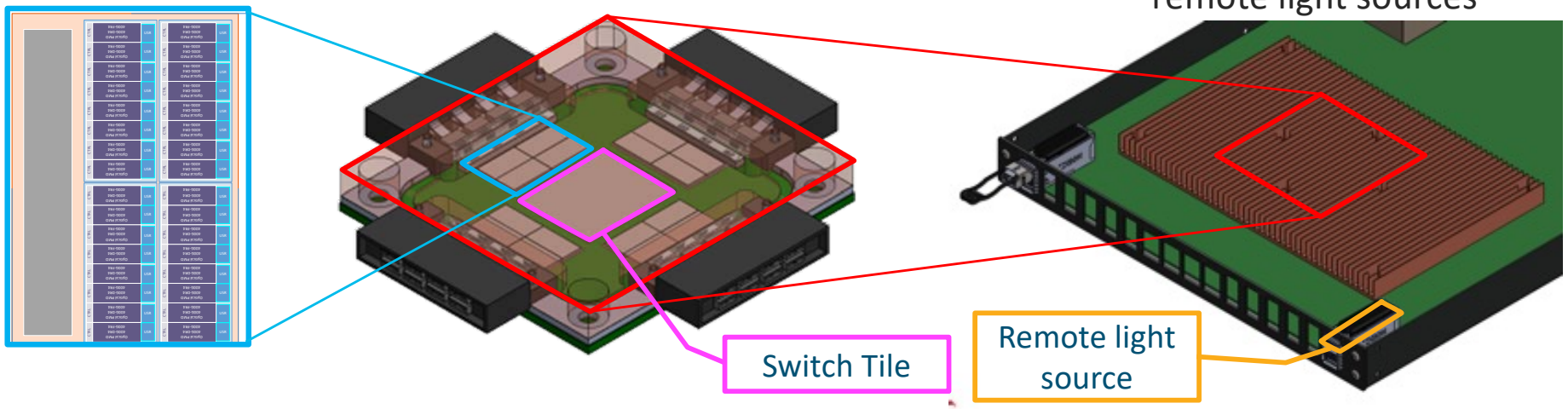
Co-Packaged Optics for lower power dissipation

Optical Tile

Multichip Module

MCM integrated on host board with remote light sources



- Main purpose co-packaged optics: reduce power by moving optical transceivers closer to switch core
- Routing and Signal-Integrity challenges require higher density optical transceivers (more Gbps/mm2) on large high-performance substrates. 3.2T, 6.4T, 12.8T per photonic engine.
- Proximity of optics and switch ASIC results in significant heat sinking challenges prompting use of remote light sources.

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Silicon Photonics Technology Requirements for Current and Future Transceiver Applications

Product Requirements	Technology Requirements
Increasing electrical and optical bit rate: • Electrical: 28 G -> 56 G -> 112 G -> 224 G • Optical: 25 G -> 100 G -> 200G -> 400G	• High BW modulators & photo detectors (50GHz -> 100 GHz) • Support advanced CMOS N7 -> N5 -> N3 • Lower parasitics (R, L, C): TSV/TDV, smaller bumps, bump-less
Increasing integration level (cumulative data rate / chipset): • Larger number of channels and optical I/Os • Higher density: Gb/mm2 • Higher density of power dissipation: heat sink challenge	• Denser interconnect (smaller bumps, bump-less, dense TSV/TDV) • Support larger P-die size (1x reticle sizes or more) & multiple E-die on P-die • Improved thermal interfaces • Support advanced CMOS N7 -> N5 -> N3
Increasing optical device performance requirements: • Support higher link penalties • More extensive use of WDM • High-power, low-noise light source (internal/external)	• Continue reducing insertion losses: grating & edge couplers, waveguides, passive devices • Integrated/external mux/demux • Efficient external light source
Manufacturing requirements: • High-volume, low-cost manufacturing • Time to market	• Leverage mature approaches & technologies • Automation • Minimize complexity

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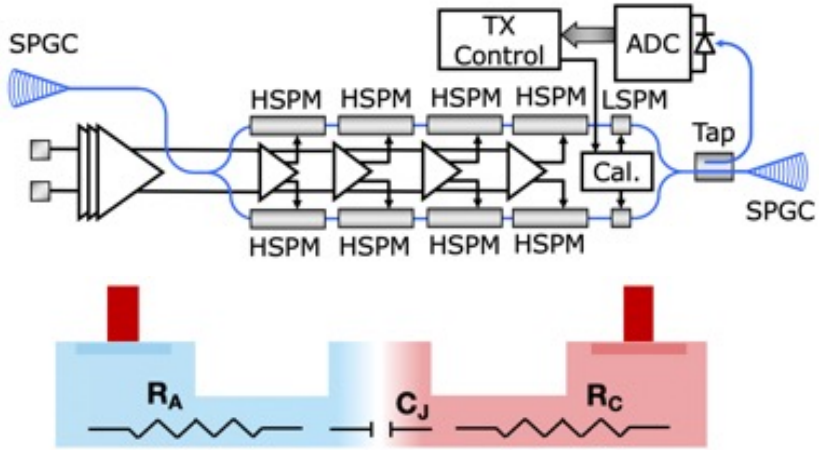
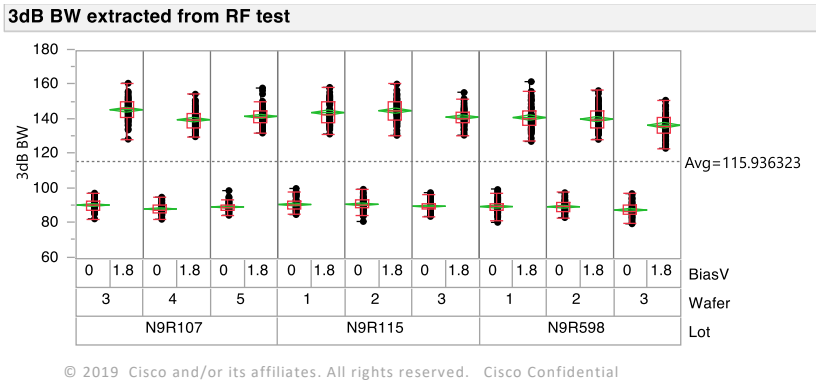
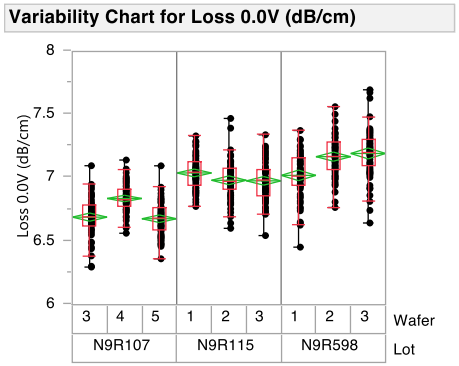
Advanced Silicon Photonics Devices: High-Speed Phase Modulators

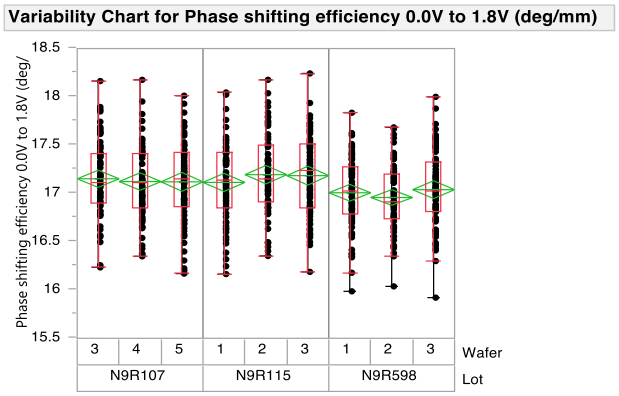
Phase modulator (key element of distributed MZI)

- PN junction carrier depletion, BW determined by dielectric relaxation time and access RC time constant.
- $V_\pi L_\pi$ < 1.9 V.cm (17 deg/mm at 1.8V)
- Insertion loss: ~0.7 dB/mm (passive)
- BW: ~ 116 GHz (RC time constant is dominant)









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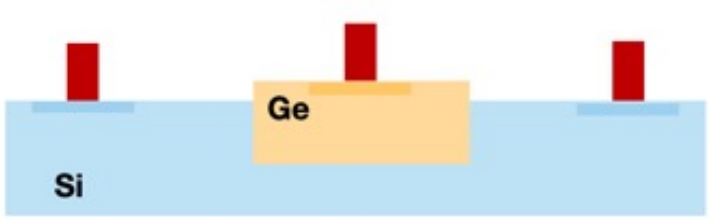
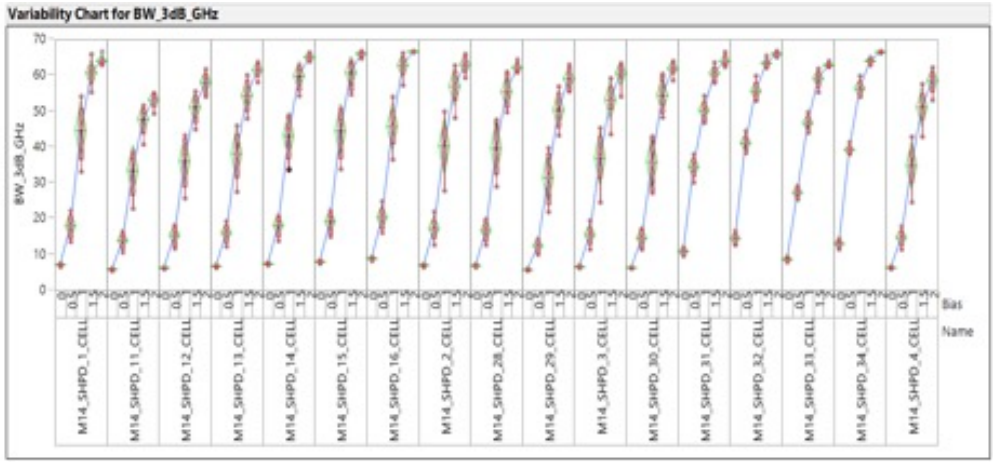
Advanced Silicon Photonics Devices: High-Speed Photodetector

Ge Waveguide Photodetector:

- Ge single-heterostructure photodetector reduces transit time compared to double-heterojunction designs
- Responsivity: 1 A/W
- BW: 65 GHz (2V bias)
- Idark: < 1 µA
- Capacitance: < 5 fF





SHPD DOE data with 67GHz LCA

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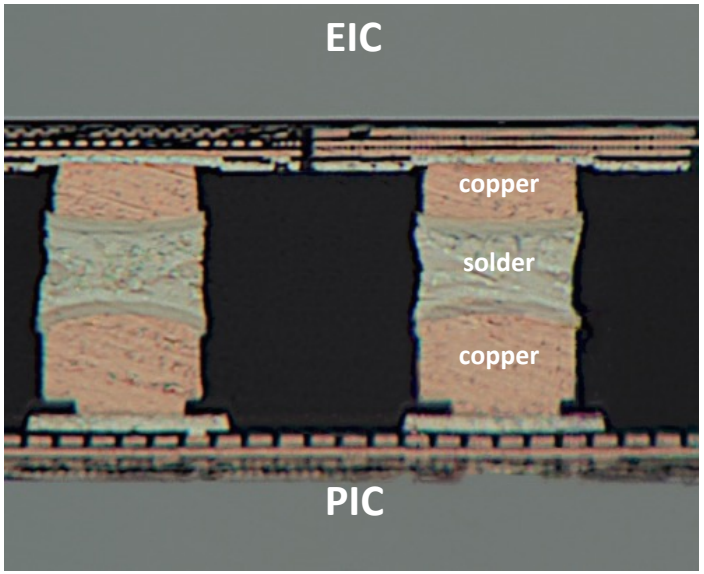
Importance of Packaging: Impact on RX sensitivity

- Receiver sensitivity is determined by transimpedance gain/noise vs bandwidth tradeoff:
  - Strongly affected by parasitic capacitance at the input of the TIA
  - This tradeoff gets even more important at higher data rates
- Hybrid integration between EIC and PIC by means of micro-bumps (CuPi):
  - TIA input capacitance composed of: C_{PD}, C_{pad1}, C_{pad2}, input cap TIA
  - Cu Pi interconnect has ~2 x capacitance of the photodetector
- Mitigation paths:
  - Tuning out parasitics with inductors?
  - Reduce micro-bump/pad size, bump-less bonding?
  - Monolithic integration?



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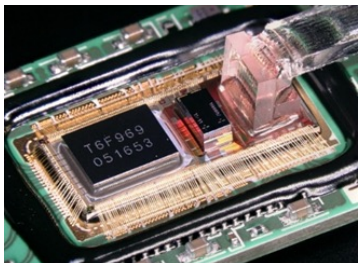
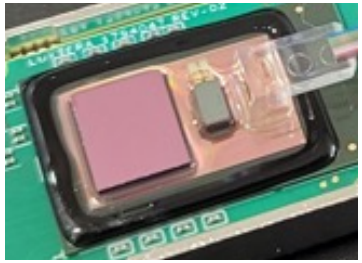
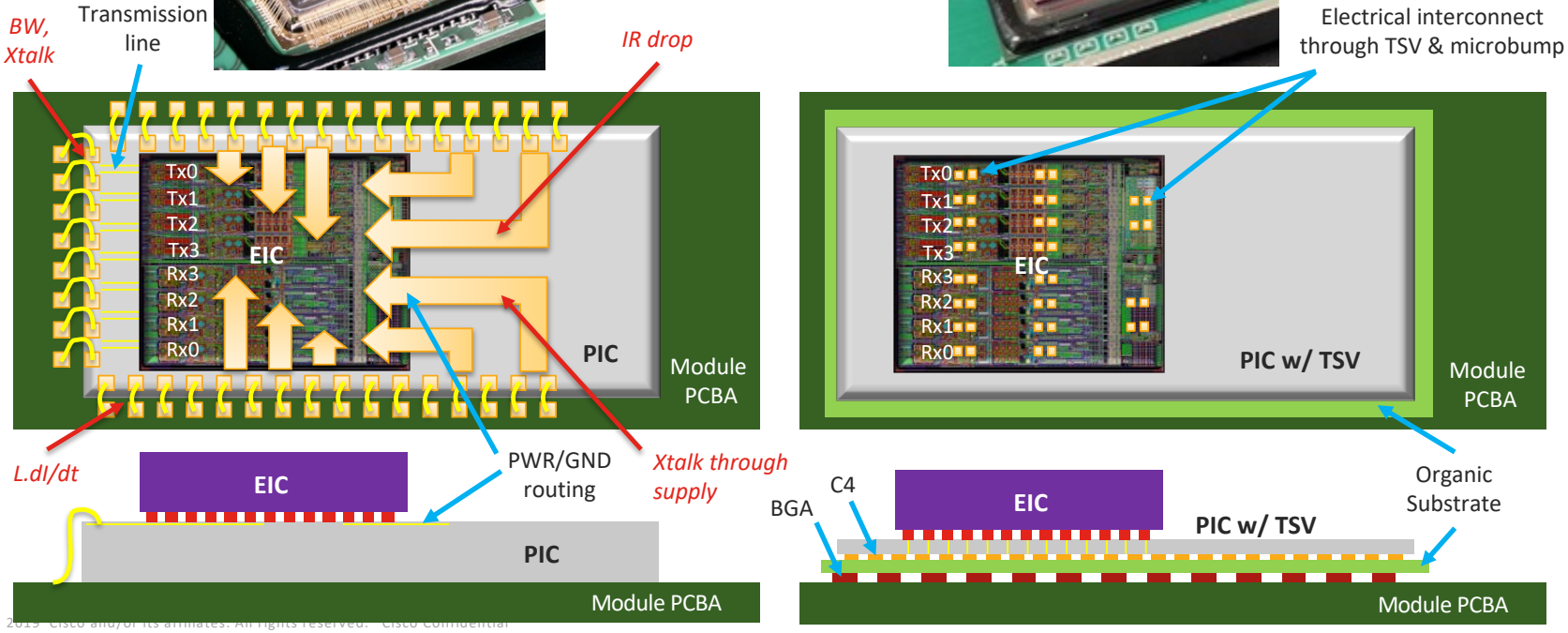
Importance of Packaging: Power Supply



100 Gbps Engine



400 Gbps Engine



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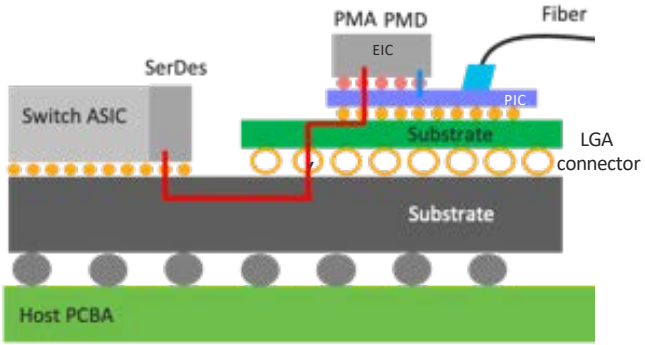
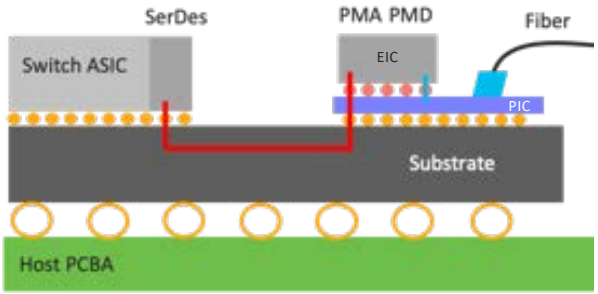
Options for 3D silicon Photonics Co-Packaged Optics

”Near Packaged” Optics by Optical Modules



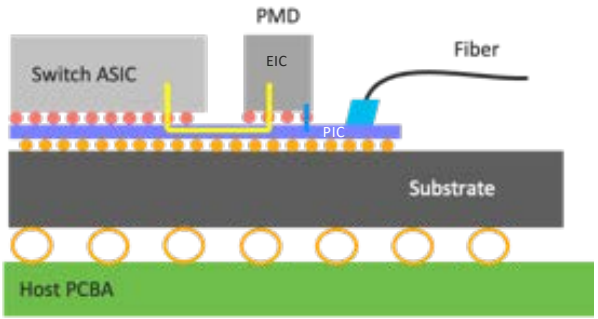
- Optical module: multiple suppliers
- Complex system integration: connectors, size constraints
- Longer traces + connector, not lowest power solution

Co-Packaged Optics by Electro-Optic MCM



- Leveraging existing technologies
- Integration at OSAT
- Shorter traces on substrate no connector, should allow lower power

Co-Packaged Optics by Silicon Photonic Interposer



- Leveraging existing technologies
- Integration at OSAT
- Shortest traces on silicon interposer, should allow lowest power

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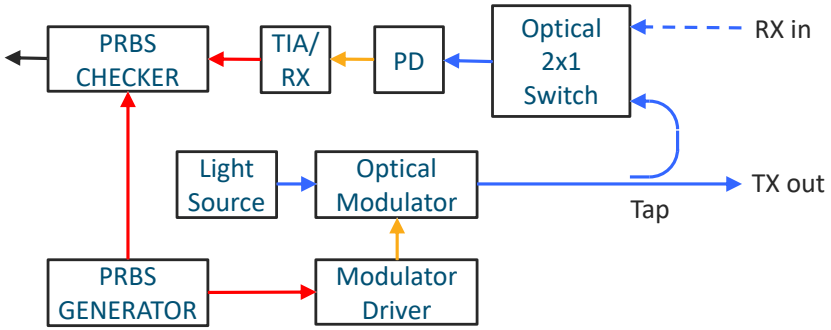
Test and Remote Light Source for Co-Packaged Optics

Co-Packaged Optics Test Flow:

- A test flow with sufficient coverage must be developed from chip to module/system
- Built-in self test for optical functionality
  - A must in high density transceivers (test time, cost,…)
  - Integrated optics allows for compact implementations of built-in self test



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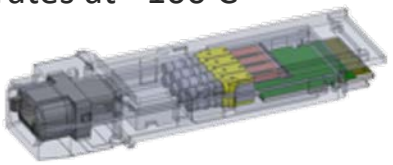
Remote Light Source for Co-Packaged Optics:

- Advantages:
  - Decoupling light source and transceiver allows the light source to operate efficiently and reliably while the transceiver operates at ~100 C
  - Field serviceability



- Standardization:
  - Formfactors & specifications under discussion
  - Bovington, et al. “External Laser Source Small Form Factor Pluggable Module Project Start”, OIF oif20-21.205.0, May 11, 2021

Overview

- Silicon Photonics Technology
- History & Outlook for Intra Datacenter Interconnect
- Requirements for Future Silicon Photonics Solutions
- **3D Silicon Photonics**
- Summary

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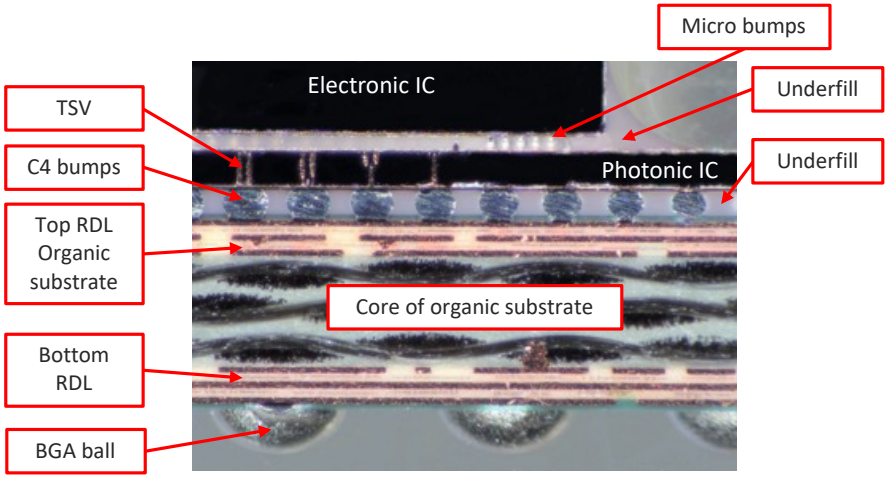
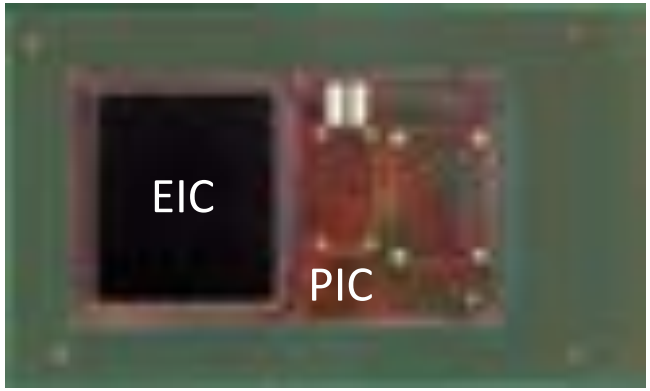
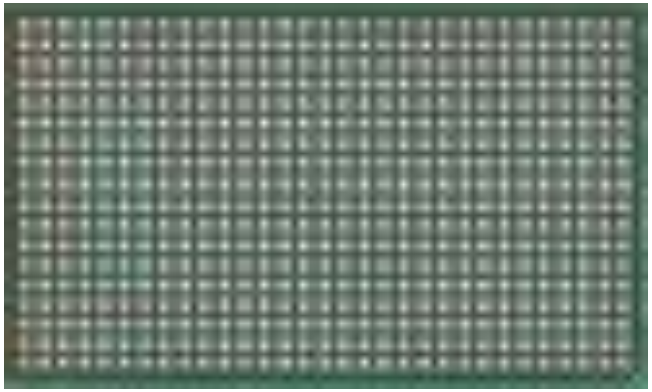
3D Silicon Photonics Technology Platform

- CoCoS: Organic substrate with PIC and EIC
- PIC has Through Substrate Vias (TSV) allowing electrical interconnect through the PIC
- EIC bonded to PIC by micro bumps
- PIC bonded to organic substrate by C4 bumps







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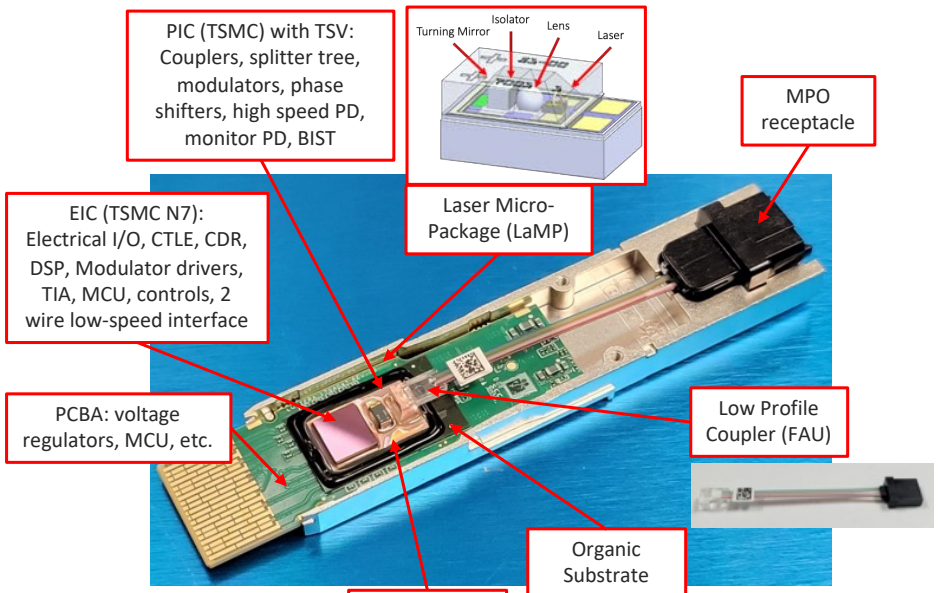
400G-DR4 QSFPDD Module: 3D Silicon Photonics vs Conventional Transceiver Technology:

Silicon Photonics (Cisco)



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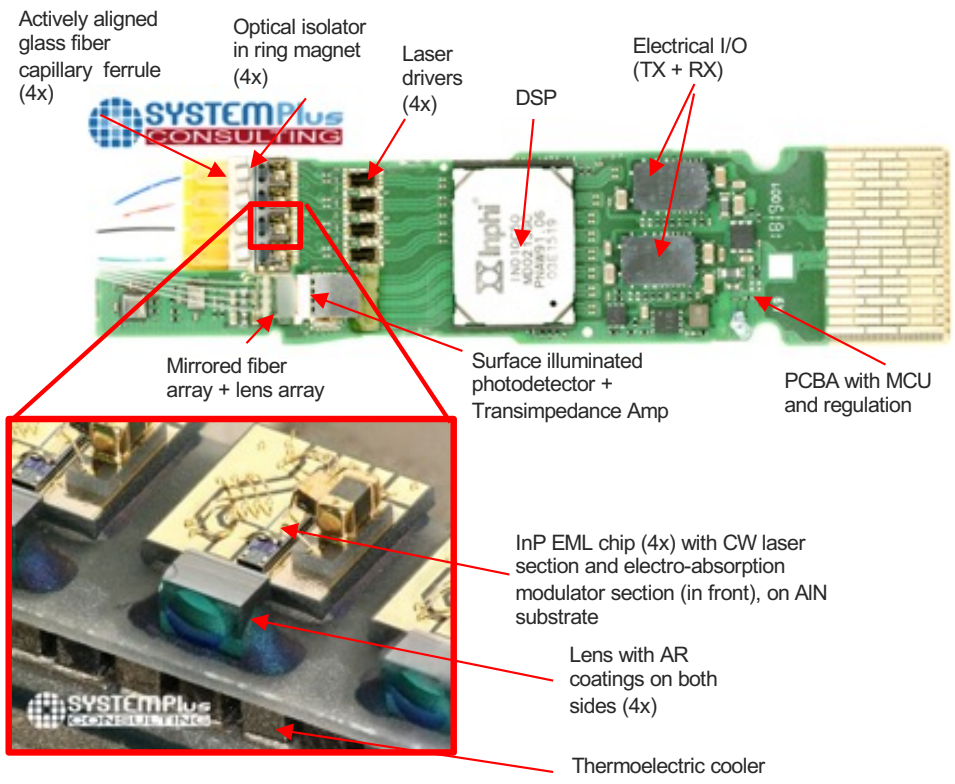
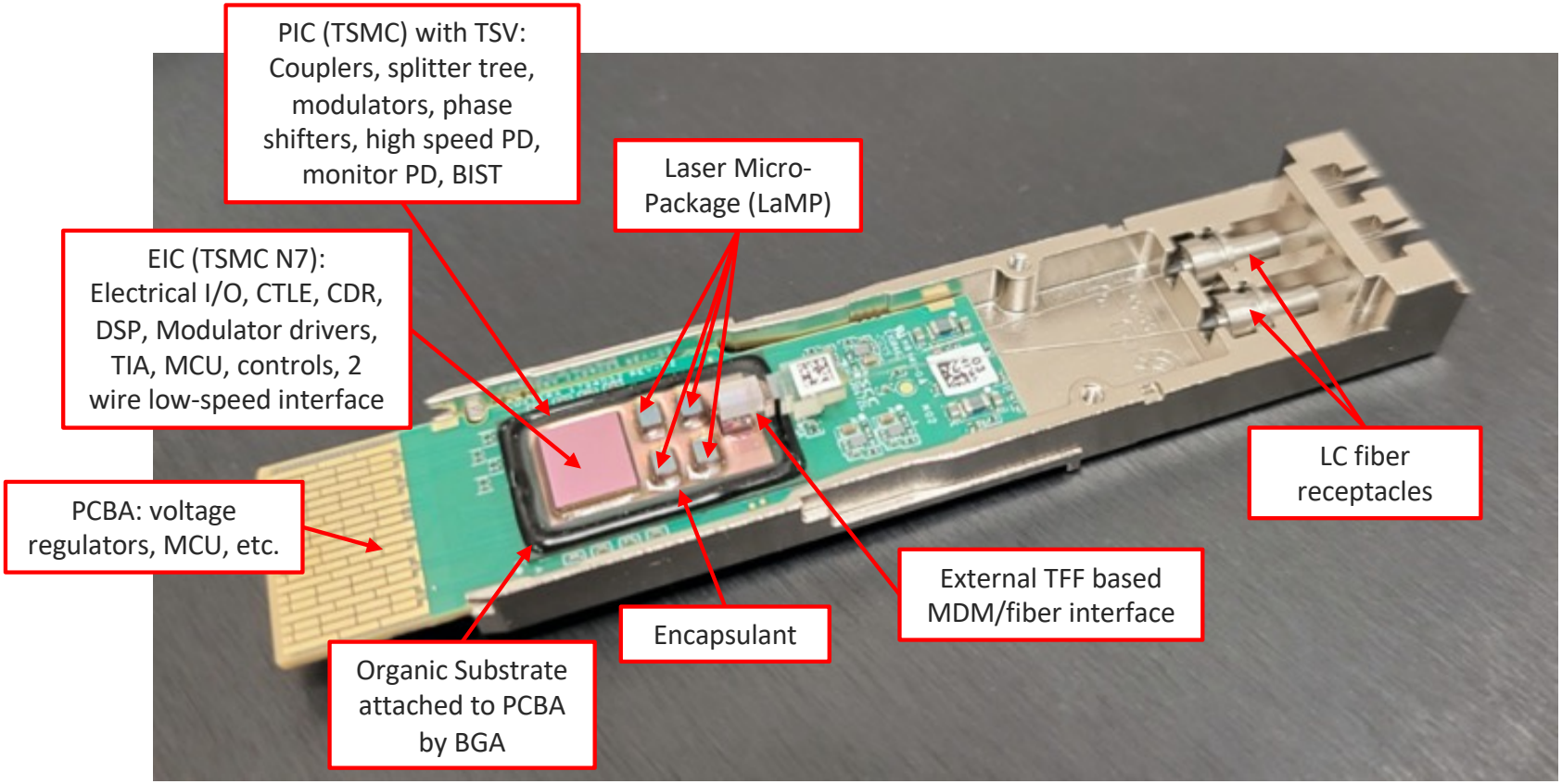
Conventional EML (Innolight)



3D Silicon Photonics 400G-FR4 QSFP-DD Module



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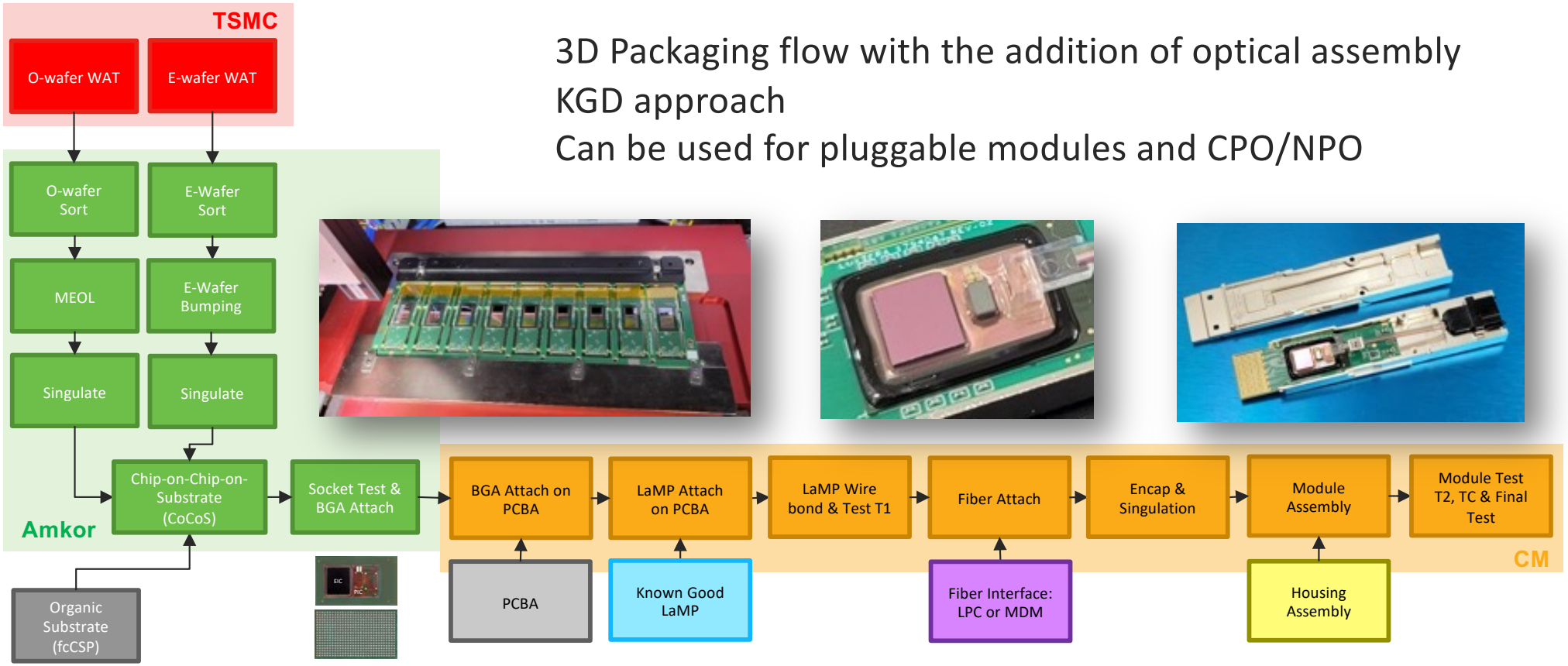
3D Silicon Photonics Manufacturing Flow



3D Packaging flow with the addition of optical assembly

KGD approach

Can be used for pluggable modules and CPO/NPO

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Summary

- Over the last decade Silicon Photonics has gained significant momentum in HV production of optical transceivers addressing Hyperscale DC, High-Performance computing, Mobile and Enterprise applications.
- As data rates per lane keep increasing: 25 G/l, 100 G/l, 200G/l, 400G/l, the technology needs to to be augmented by introducing more advanced optoelectronic devices and new packaging technologies.
- Silicon photonics in combination with 3D advanced packaging can support the data rate and density optical interconnect roadmaps demanded by the industry.

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