CU WIREBOND TECHNOLOGY IN 16FFC HIGH PERFORMANCE AUTOMOTIVE RADAR PROCESSOR WITH IR DROP REDUCTION METHODOLOGY

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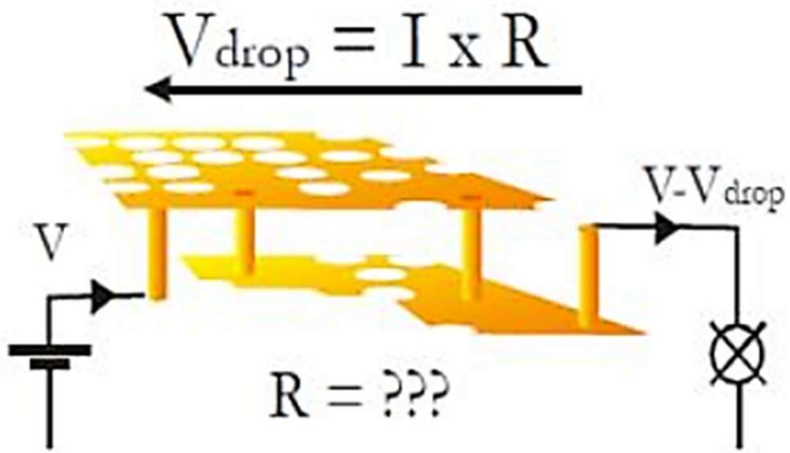
SECURE CONNECTIONS FOR A SMARTER WORLD

PUBLIC

CONTENT

- What is IR drop?
- Methods for IR drop reduction
- IR drop simulation and results
- SSB (Stand-off stitch bond) development & challenges
- Product package reliability
- Board level reliability (BLR)
- Summary

IR DROP



Interconnect Scaling → Interconnect Width ↘ → Interconnect Resistance ↗

Large Die → Interconnect Length ↗ → Interconnect Resistance ↗

Interconnect Resistance ↗ → IR ↗ → Speed and Functionality ↘

Increased Functionality per Area → Supply Voltage ↘ → $\frac{V_{Actual}}{V_{Ideal}}$ ↘ → Speed and Functionality ↘

STATIC IR DROP REDUCTION METHODS

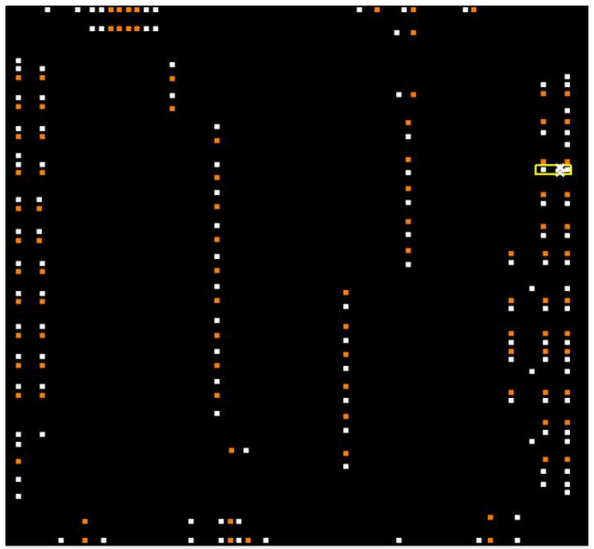
Die Level

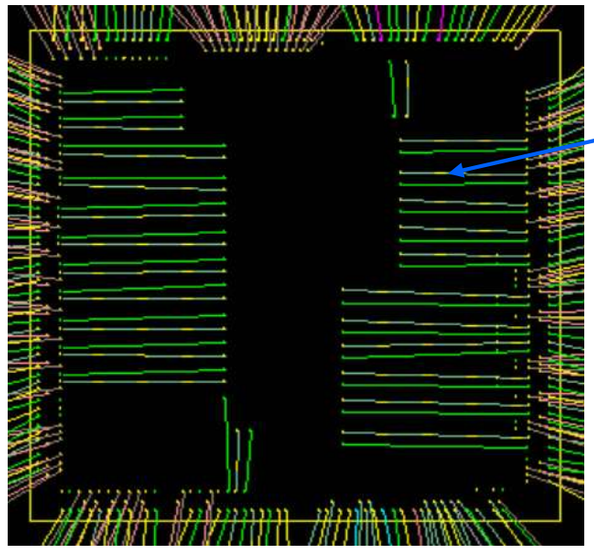
- Increase metal width of supply connections
- Increase BEOL wiring layers
- Increase BEOL thickness
- Increase Al pad thickness

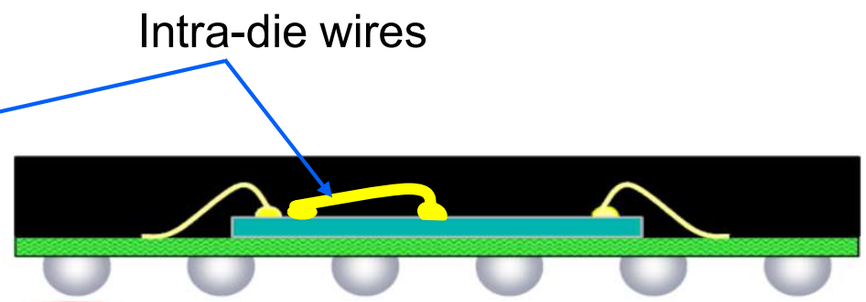
Package Level

- Flip chip: Bumps or Cu pillars across PDN
- Wire Bond: Add intra-die wires to connect peripheral supply pads to active devices in die core area

PRODUCT DESCRIPTION







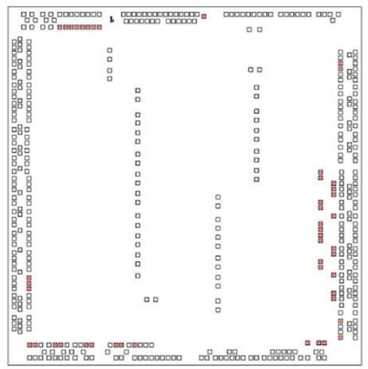
- Function: Auto radar processor
- Die: 30mm2 in 16FFc
- Power: 2W
- IR drop 30% off target
- Intra-die bond pads added at periphery and die core area

- 49 intra-die wires (24 VDD and 25 VSS)

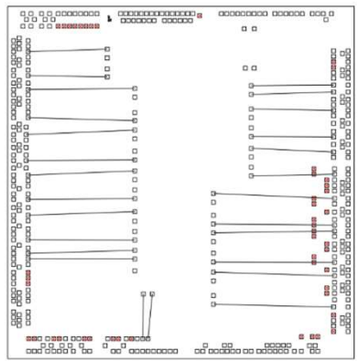
- Package: 14x14mm MAPBGA
- Substrate: 2-layer
- Wire: 20um Pd-Cu

IR DROP SIMULATIONS

Quantity of Intra-die Wires



0%



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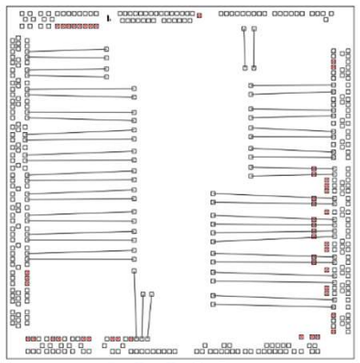
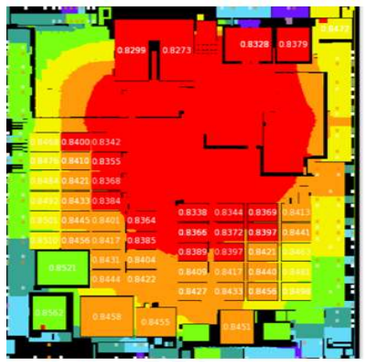


100%

IR Drop Mapping Simulation



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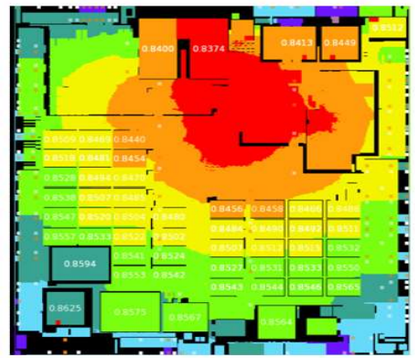

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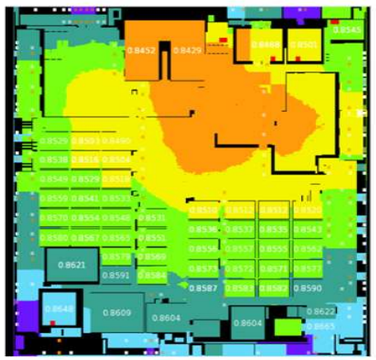


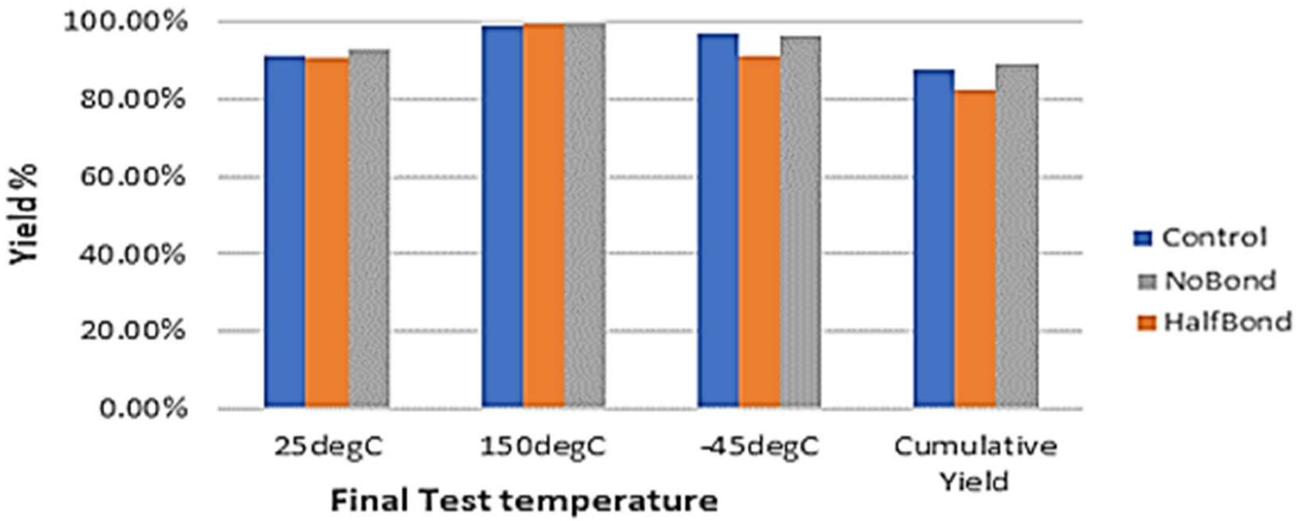
100%

Intra-die Wire Quantity	Intra-die Wirebond Count	No. of Instances > 40mV	Worst IR Drop (VDD+VSS) (mV)
0%	0	100K +	56.6
50%	26	100K +	46.2
100%	49	30	40.4

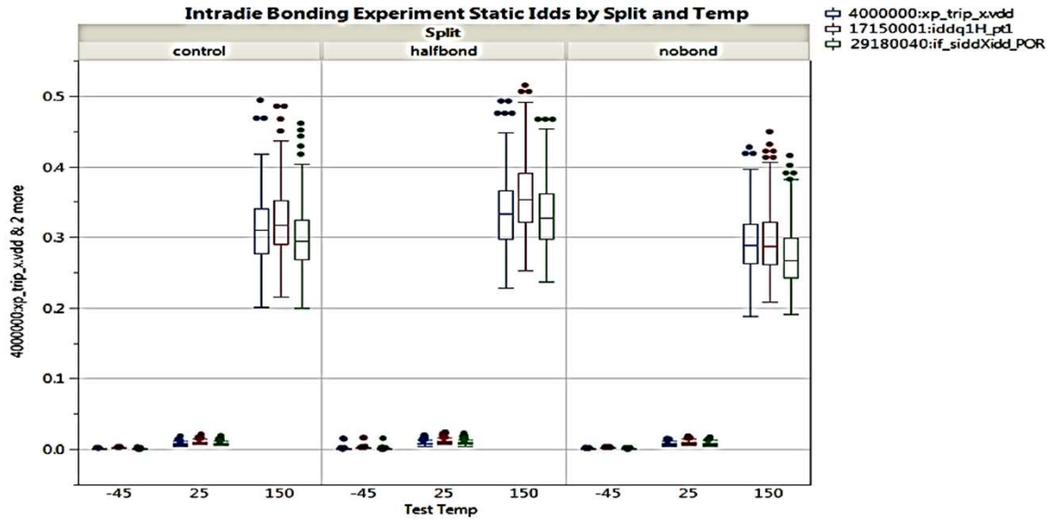
Adding 49 intra die wires enables 30% IR drop reduction.

IR DROP EMPIRICAL RESULTS

Final Test Yield



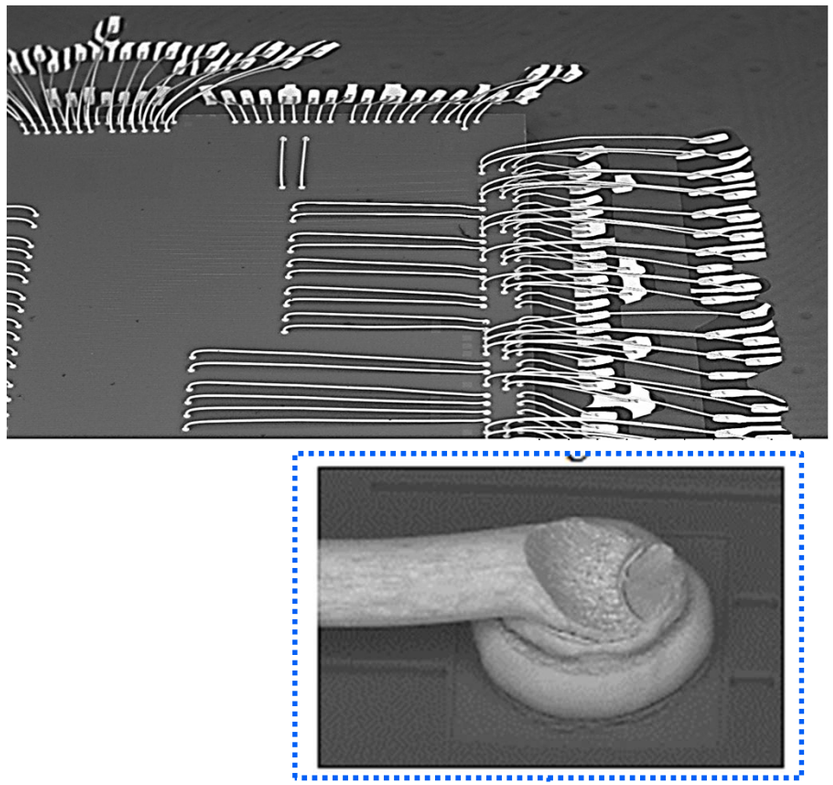
Trip Idd, iddq, Static Idd



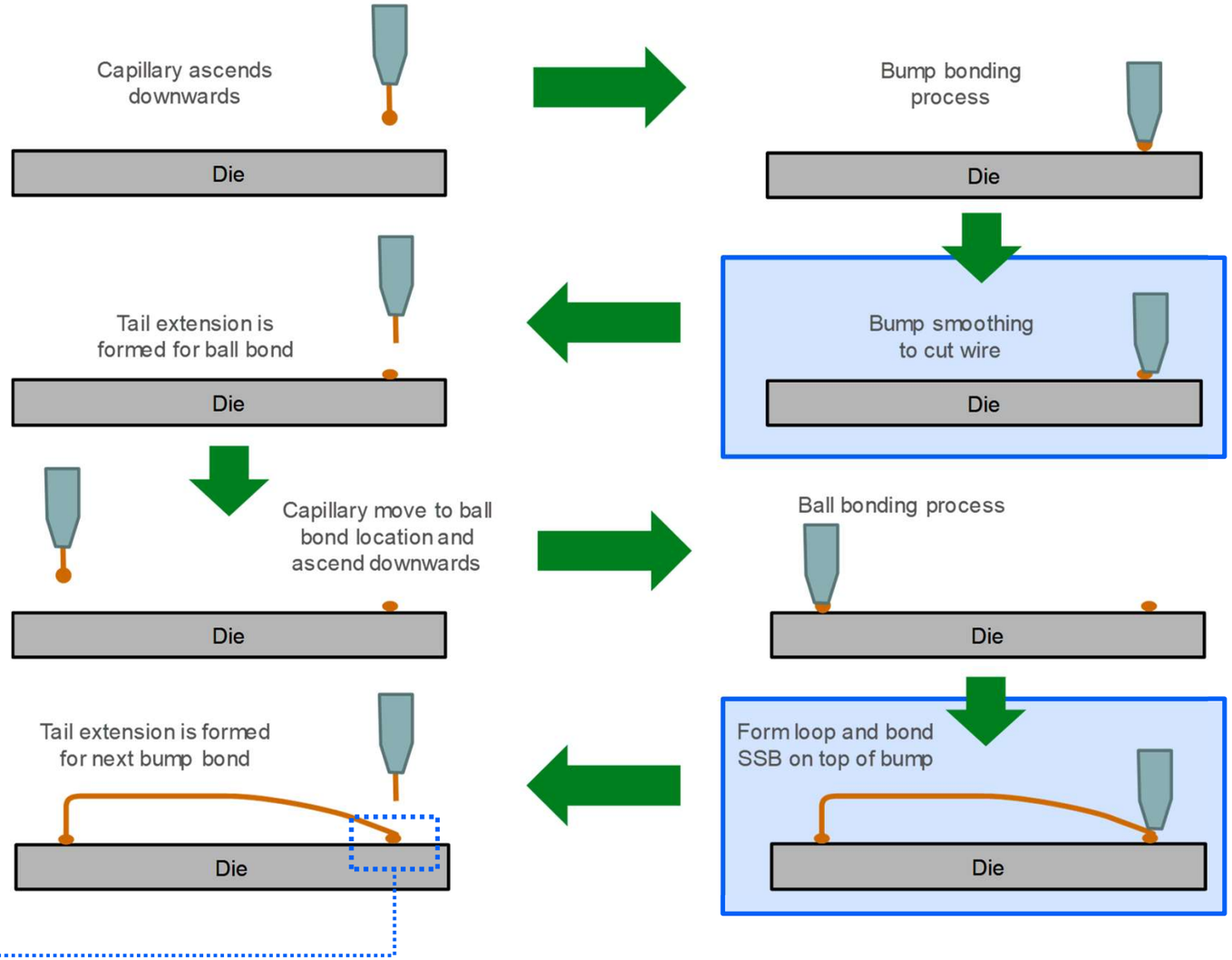
- Actual parts with 0%, 50% and 100% intra-die bonds did not show significant differences in test yield or parametric characterization.
- Nominal wafer was used. IR drop would have been more significant if worst case wafer was used.
- Intra-die wires are kept in the radar processor to provide better IR drop margin.

SSB (STAND-OFF STITCH BOND) PROCESS

SSB bonding is required when a design has “2nd bond” that needs to be placed on the die.

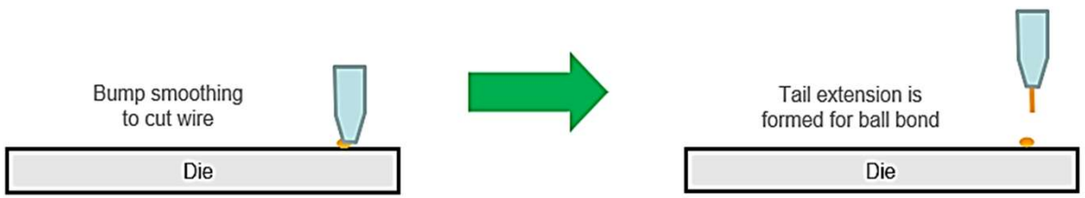


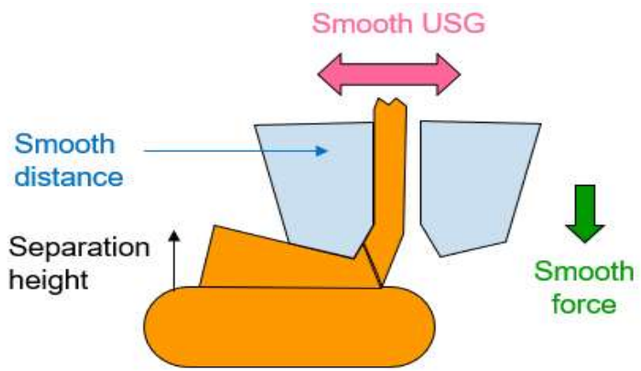
SSB Wire Bonding Process



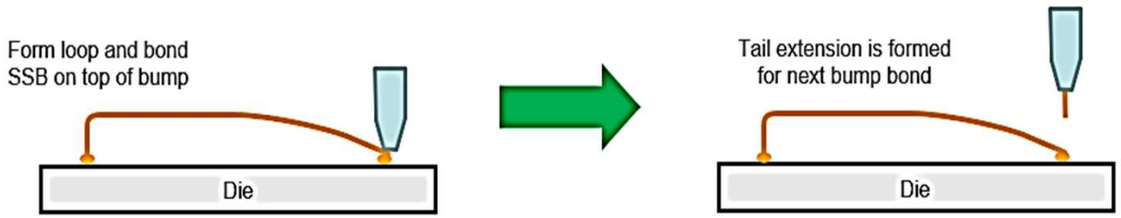
SSB DEVELOPMENT

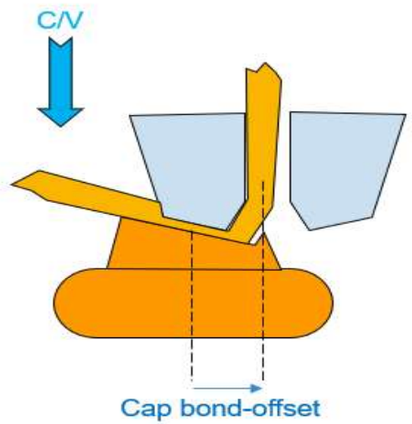
Bump Smoothing – Cutting wire after bump bond, and preparing tail for ball bond





SSB Wire Bonding – Bonding of stitch bond on top of bump, and preparing tail for bump or ball bond *(depending on next wire being normal or intra-die wire)*





- Bump smoothing optimization is required to eliminate short or long tail event after bump.
- 2nd bond parameter optimization is required for SSB to eliminate non-stick and short tail events.

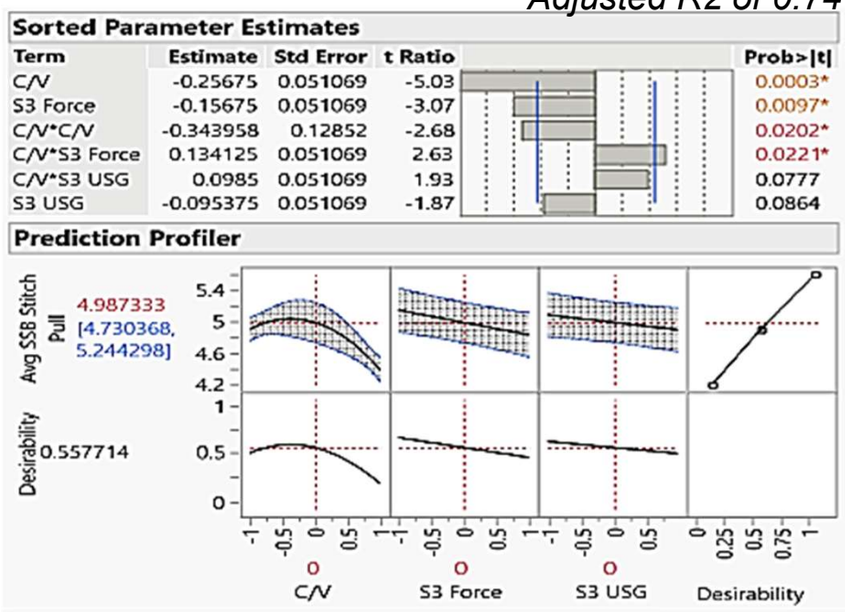
OPTIMIZING SSB BONDING PROCESS

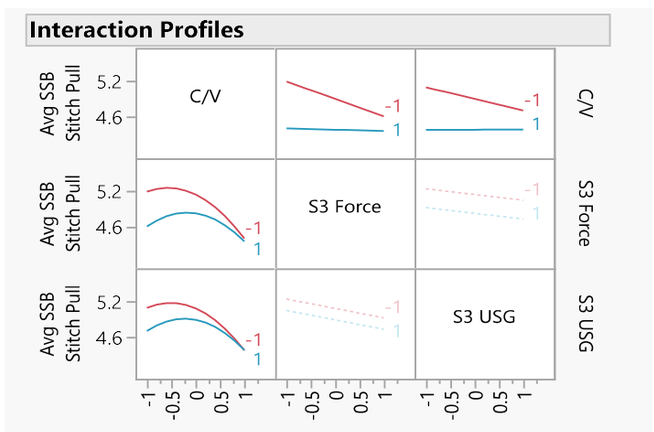
DOE 1: Identify SSB parameters that can improve SSB stitch pull strength

DOE design: 8-factor 2-level fractional factorial DOE with 3 center points (19 cells)

Pattern	C/V	Pre-bleed	S1 USG	S1 Force	S2 USG	S2 Force	S3 USG	S3 Force
00000000	0	0	0	0	0	0	0	0
+--++--+	1	-1	-1	1	1	-1	-1	1
--++--++	-1	-1	1	1	-1	-1	1	1
+-+-+-+-	1	-1	1	-1	1	-1	1	-1
---++++-	-1	-1	-1	1	1	1	1	-1
-+--+-++	-1	1	-1	-1	1	-1	1	1
--------	-1	-1	-1	-1	-1	-1	-1	-1
-++++---	-1	1	1	1	1	-1	-1	-1
++-+--+-	1	1	-1	1	-1	-1	1	-1
00000000	0	0	0	0	0	0	0	0
--+-++-+	-1	-1	1	-1	1	1	-1	1
+++----+	1	1	1	-1	-1	-1	-1	1
++++++++	1	1	1	1	1	1	1	1
++--++--	1	1	-1	-1	1	1	-1	-1
-+-+-+-+	-1	1	-1	1	-1	1	-1	1
+-++-+--	1	-1	1	1	-1	1	-1	-1
+----+++	1	-1	-1	-1	-1	1	1	1
-++--++-	-1	1	1	-1	-1	1	1	-1
00000000	0	0	0	0	0	0	0	0

R2 of 0.82
Adjusted R2 of 0.74





- 2 **significant factors** for higher SSB stitch pull strength: **C/V and S3 force**
- Lower C/V can yield higher stitch pull due to thicker stitch formation.

OPTIMIZING BUMP SMOOTHING

DOE 2: Identify bump smoothing parameters that can improve SSB stitch pull strength

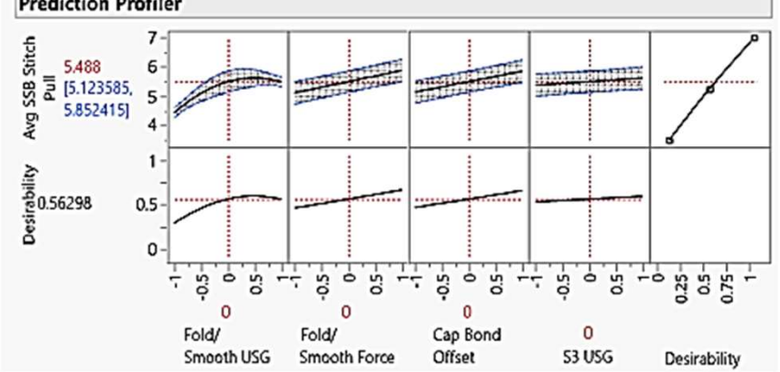
DOE design: 6-factor 2-level fractional factorial DOE with 2 center points (18 cells)

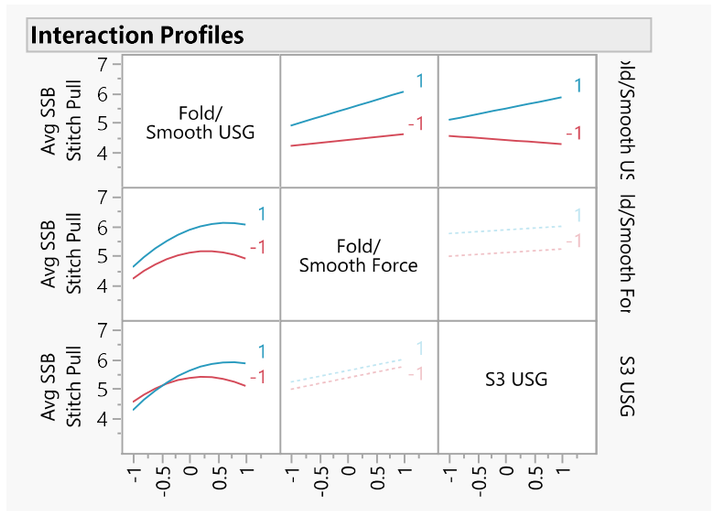
Pattern	S3 USG	S3 Force	Cap Bond Offset	Smooth Distance	Fold/ Smooth Force	Fold/ Smooth USG
000000	0	0	0	0	0	0
−+−−+−	-1	1	-1	-1	1	-1
−−−−−−	-1	-1	-1	-1	-1	-1
−++−−+	-1	1	1	-1	-1	1
−+−+−+	-1	1	-1	1	-1	1
−++++−	-1	1	1	1	1	-1
+−++−+	1	-1	1	1	-1	1
+++−−−	1	1	1	-1	-1	-1
+−−−−+	1	-1	-1	-1	-1	1
−−++−−	-1	-1	1	1	-1	-1
−−+−++	-1	-1	1	-1	1	1
++−−++	1	1	-1	-1	1	1
++++++	1	1	1	1	1	1
+−−++−	1	-1	-1	1	1	-1
+−+−+−	1	-1	1	-1	1	-1
++−+−−	1	1	-1	1	-1	-1
−−−+++	-1	-1	-1	1	1	1
000000	0	0	0	0	0	0

R2 value of 0.95
Adj R2 value of 0.92

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Fold/Smooth USG	0.529375	0.057824	9.15	<.0001*
Fold/Smooth Force	0.38375	0.057824	6.64	<.0001*
Cap Bond Offset	0.35725	0.057824	6.18	0.0001*
Fold/Smooth USG*S3 USG	0.259125	0.057824	4.48	0.0012*
Fold/Smooth USG*Fold/Smooth Force	0.188375	0.057824	3.26	0.0086*
Fold/Smooth USG*Fold/Smooth USG	-0.542	0.173472	-3.12	0.0108*
S3 USG	0.1215	0.057824	2.10	0.0620



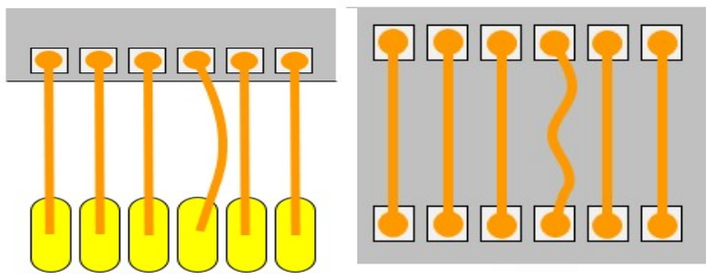


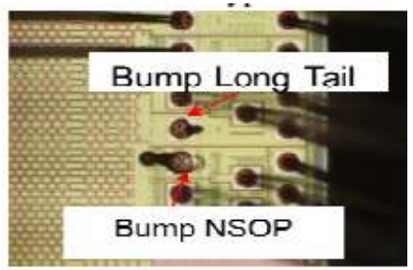
3 **significant factors** for higher SSB stitch pull strength: **Fold/Smooth USG, Fold/Smooth Force and Cap Bond Offset**

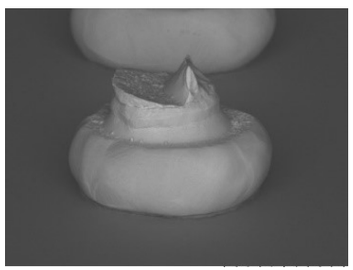
001332

INTRA-DIE WIREBOND MANUFACTURING CHALLENGES AND MITIGATIONS

Wire Looping: Wire touching exposed metal on die surface causing electrical failure	**Wire Straightness:** Wire shorting due to wire sway and S-ing due to stitch bond being formed on the same plane as 1st bond	**Bump Smoothing:** Excessive bump smoothing results in short tail errors, while insufficient smoothing results in long tail errors.
• Looping optimization to form a lowest possible loop height without wire sagging near 2nd bond region (SSB side) • Different looping parameters for different wire lengths	• Establish design rules for minimum wire pitch for intra-die wires	• SSB bump optimization DOE • Monitor bump and SSB defects: Bump NSOP, Short/long tail after bump, SSB stitch NSOB and SSB stitch short tail







INTRA-DIE WIREBOND MANUFACTURING CHALLENGES AND MITIGATIONS

Bump placement: Capillary's reverse motion hitting on other wires during intra-die ball looping trajectory

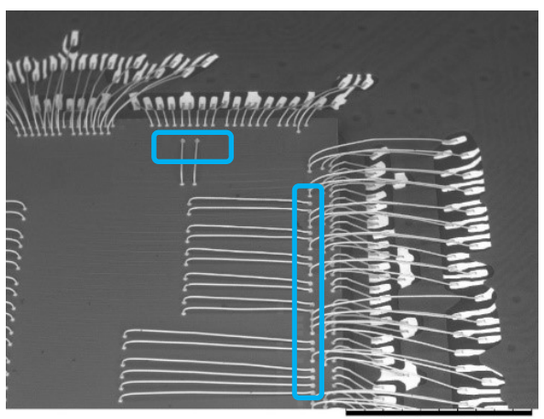
- Place SSB bumps near peripheral pads and intra-die balls in die interior

SSB Bump Oxidation: Oxidation causing NSOL and reduced interconnect reliability

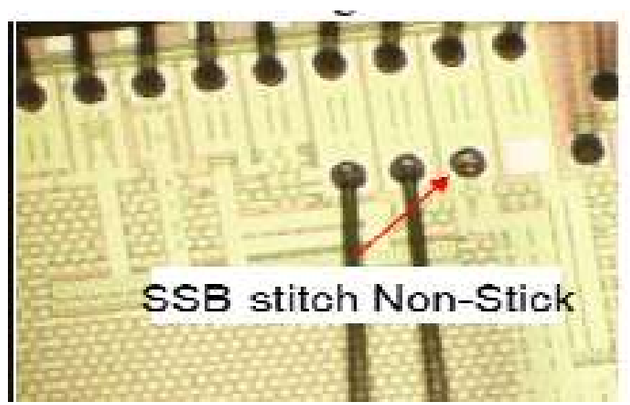
- Use Pd coated Cu wire
- Use Bump-bond-bump-bond concept for intra-die wires or control delay time before SSB

Yield Loss: SSB process doubles the failure opportunity as compared to standard bonding.

- Optimized intra-die wire bond recipe can produce low defect rate.



SSB bump at die edge

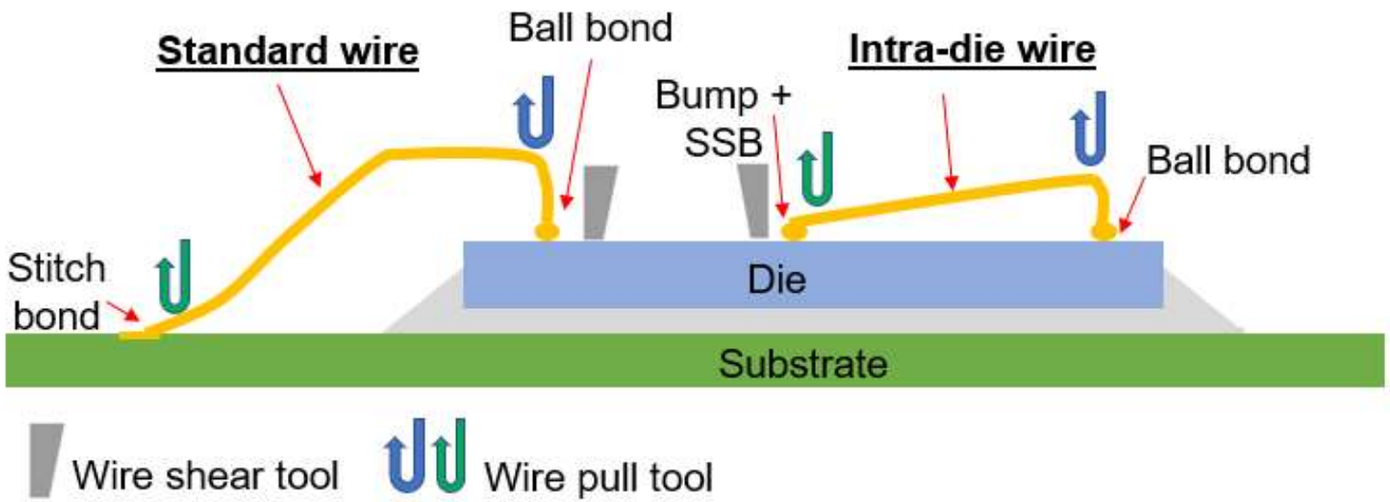


PACKAGE RELIABILITY RESULTS – ELECTRICAL TESTS

Reliability Stress	Conditions	Readpoints			Electrical Test Results
		1X	2X	3X	
uHAST	110C/85%RH	264 hrs	528 hrs	792 hrs	✓
THB	85C/85%RH	1000 hrs	2000 hrs	3000 hrs	✓
HTSL	150C	1000 hrs	2000 hrs	3000 hrs	✓
AA-TC	-55/150C	1000 cyc	2000 cyc	3000 cyc	✓

Package BOM passes electrical test up to 3X readpoints of AEC Grade 1.

PACKAGE RELIABILITY RESULTS – AEC Q006 CU WIRE BOND CONSTRUCTION ANALYSIS



Standard wire

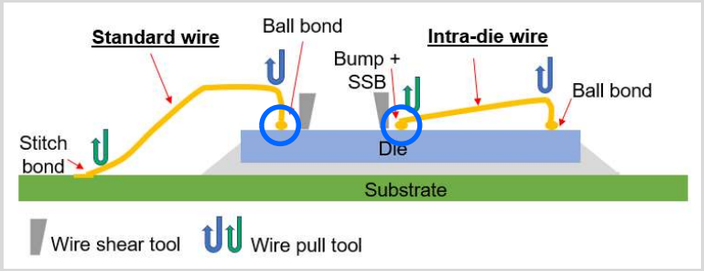
- Ball side – ball shear
- Ball side – wire pull
- Stitch side – stitch pull

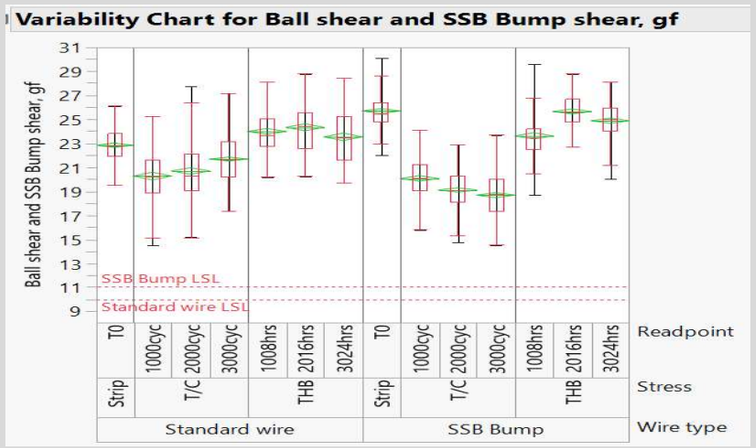
Intra-die Wire

- SSB bump – ball shear
- Ball side - wire pull
- SSB stitch – stitch pull

PACKAGE RELIABILITY RESULTS – WIRE BOND INTEGRITY

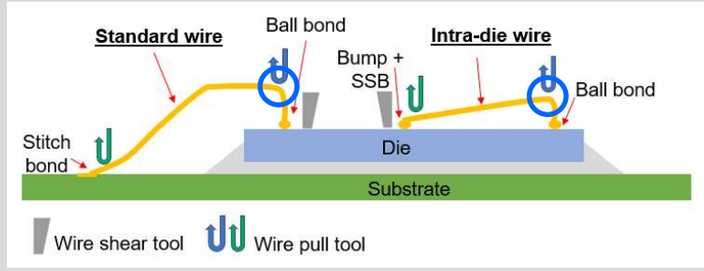
Ball Shear

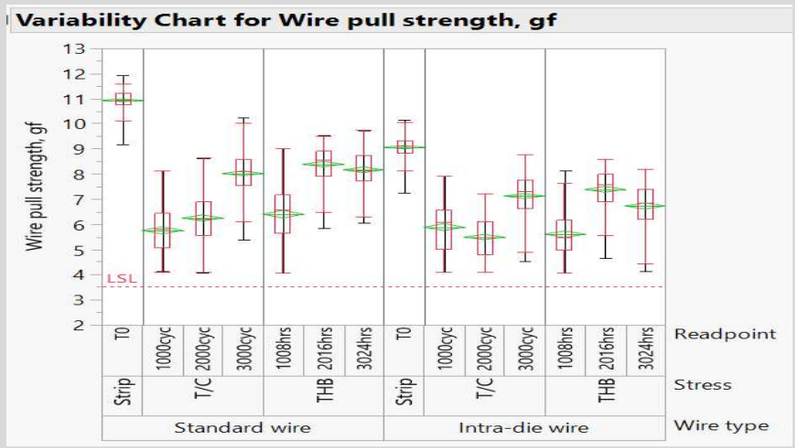




- Passed LSL with preferred failure mode of shearing through Cu ball. No significant degradation after 3X tests.
- Higher T0 ball shear in SSB bump due to larger bump size.

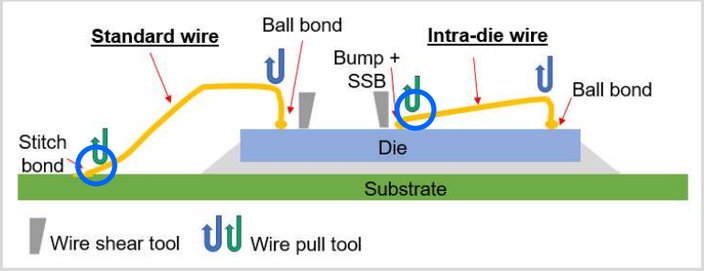
Wire Pull

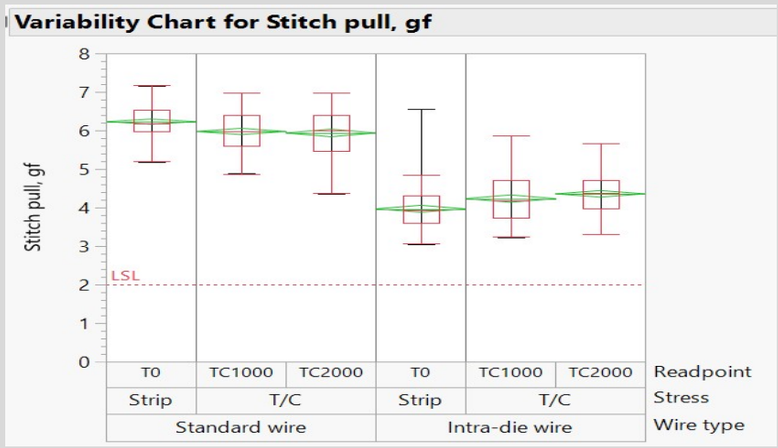




- Passed LSL with preferred failure mode of break at wire.
- Lower T0 wire pull of intra-die wire due to wire trajectory.
- Lower results with wide variation after package stresses due to chemical decapsulation.

Stitch Pull



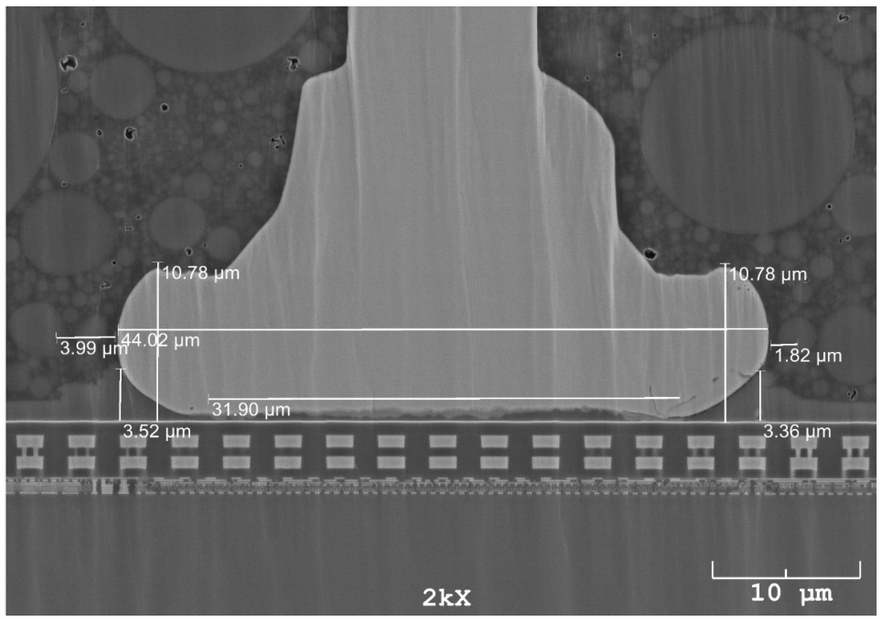


- Passed LSL with preferred failure mode of break at stitch.
- Lower T0 SSB stitch pull strength due to intra-die wire trajectory and stitch formation on bump.

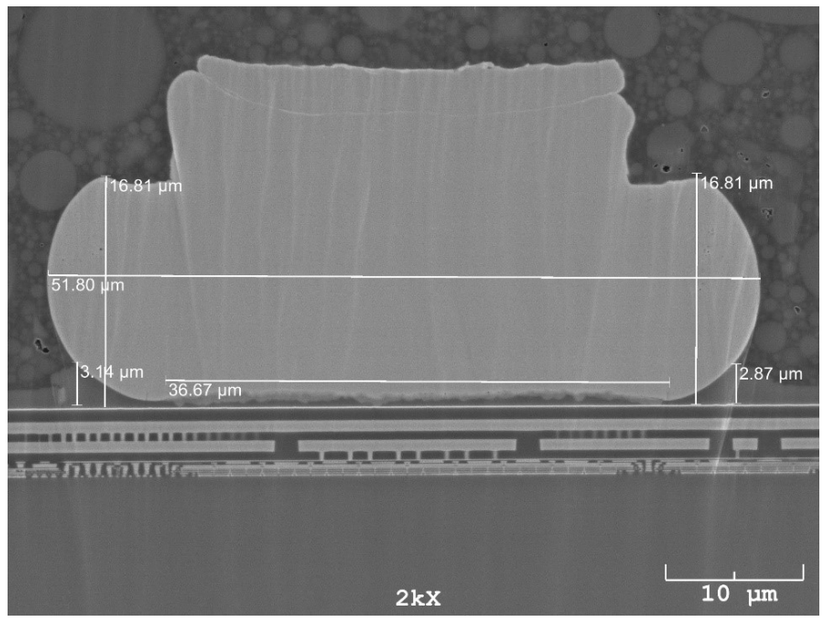
PACKAGE RELIABILITY RESULTS – IMC FORMATION

Bond Ball Cross Sections 2016 hour HTSL 150C

Standard Ball Bond

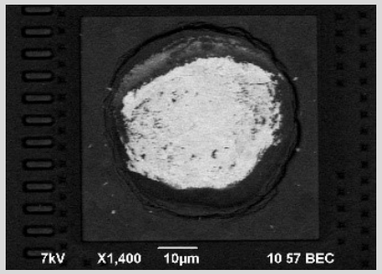
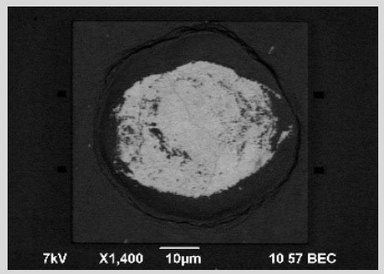
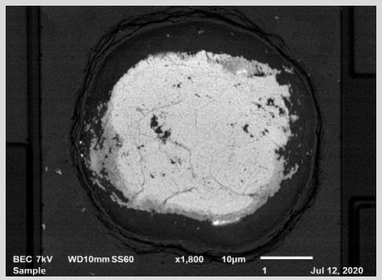
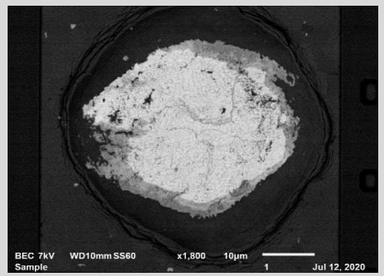


SSB Bump



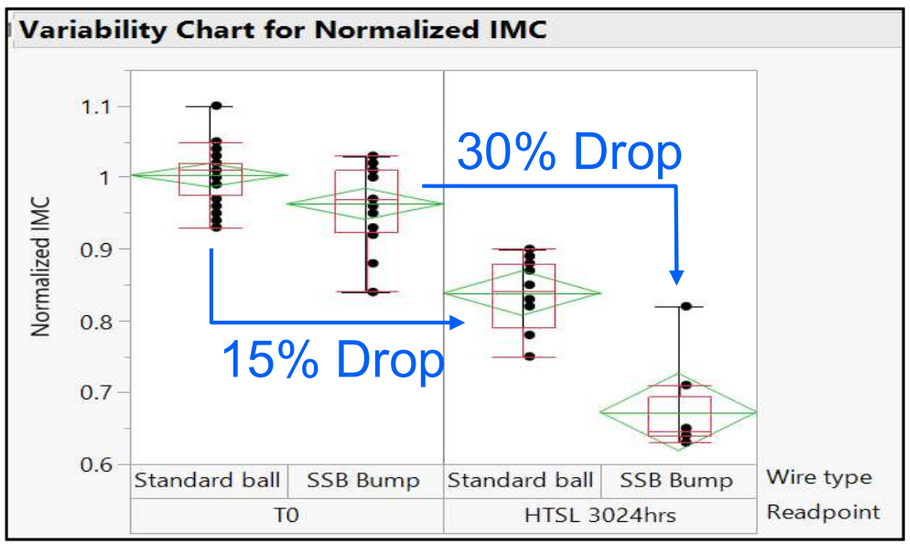
Minimal interfacial crack is observed at Cu-Al IMC region.
No BEOL damage is observed.

PACKAGE RELIABILITY RESULTS – IMC DEGRADATION

	Standard Ball	Intra-die SSB Bump
T0		
HTSL 150C 3024 hours		

- Planar analysis is used to quantify IMC coverage and degradation after package stress.
- SSB bump IMC degradation is faster than standard ball.
- Even with IMC degradation, the remaining IMC remains strong.

IMC Contact Diameter



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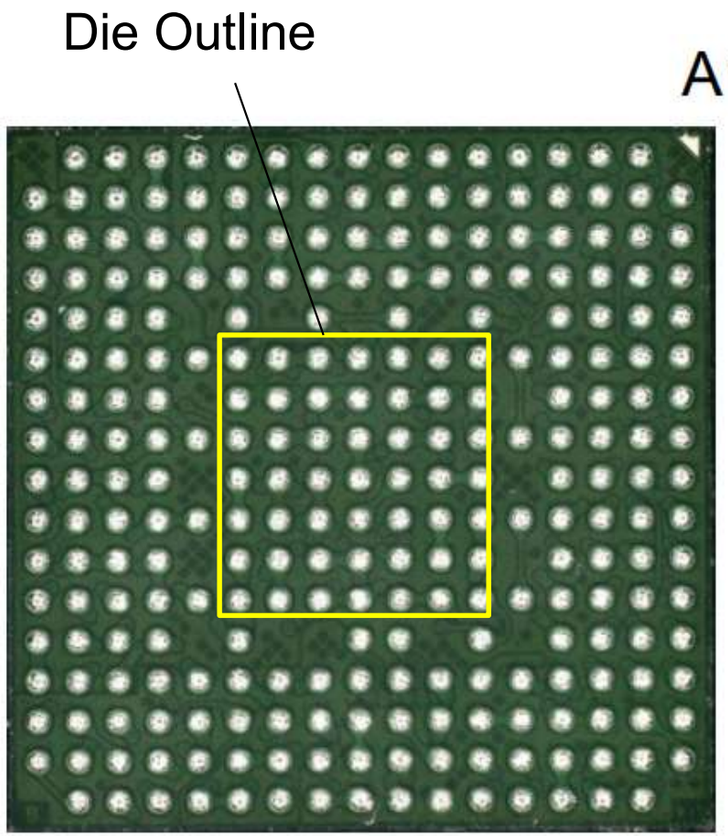
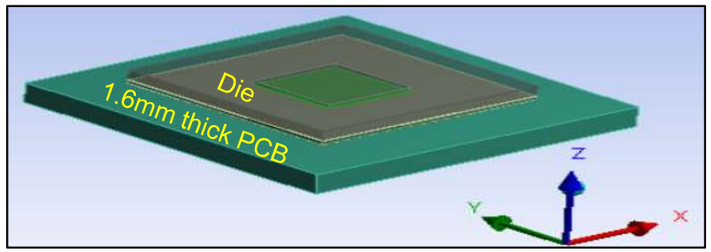
BOARD LEVEL RELIABILITY (BLR)

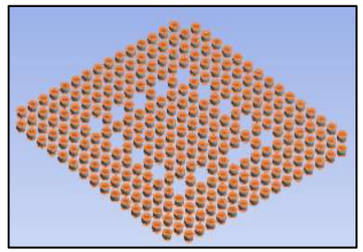


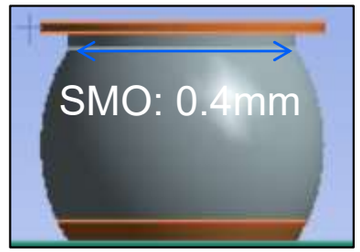
Package Bottom View

- Test Vehicle :
  - Die size: 30mm2
  - Package: 14mm x 14mm 0.8mm pitch MAPBGA
  - Die:Package: 15%
  - Substrate: 2-layer
  - Solder ball: 0.4mm SnAg
  - Depopulated 4 corner balls
- PCB: FR4, 8 Cu layers, 1.6 mm thick, 0.34mm Cu pads, NSMD
- Purpose: To continuously monitor the solder joint integrity during thermal cycling
- Concern: Depopulated 4 corner balls may increase the fatigue damage in the neighboring corner balls.

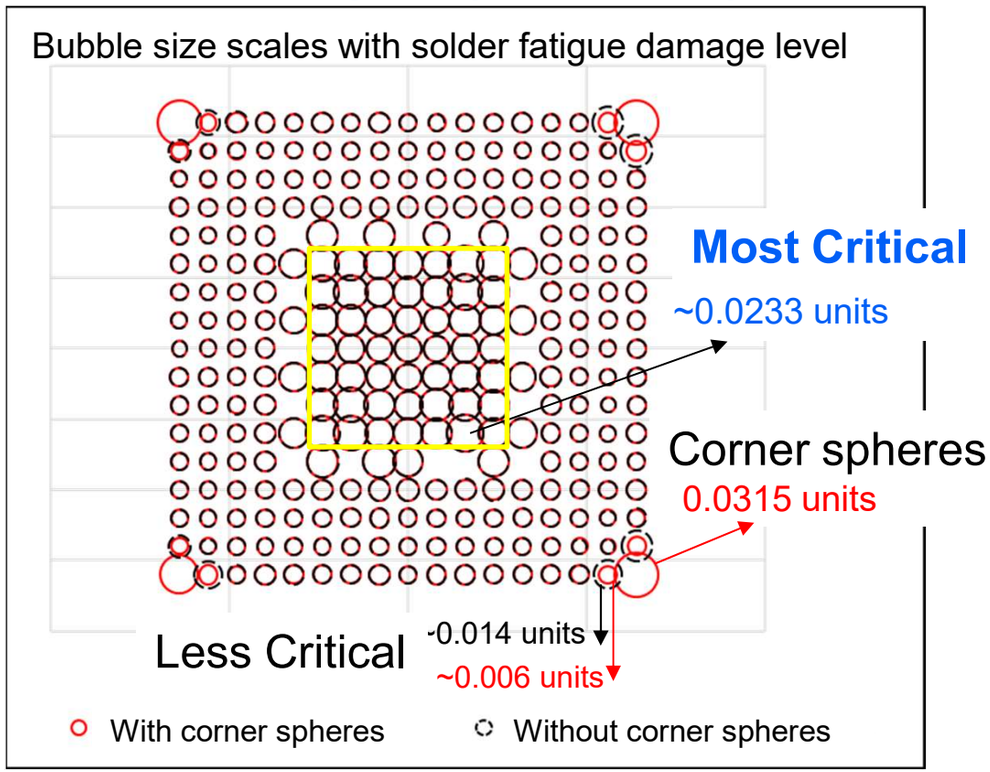
BOARD LEVEL RELIABILITY (BLR) SIMULATION







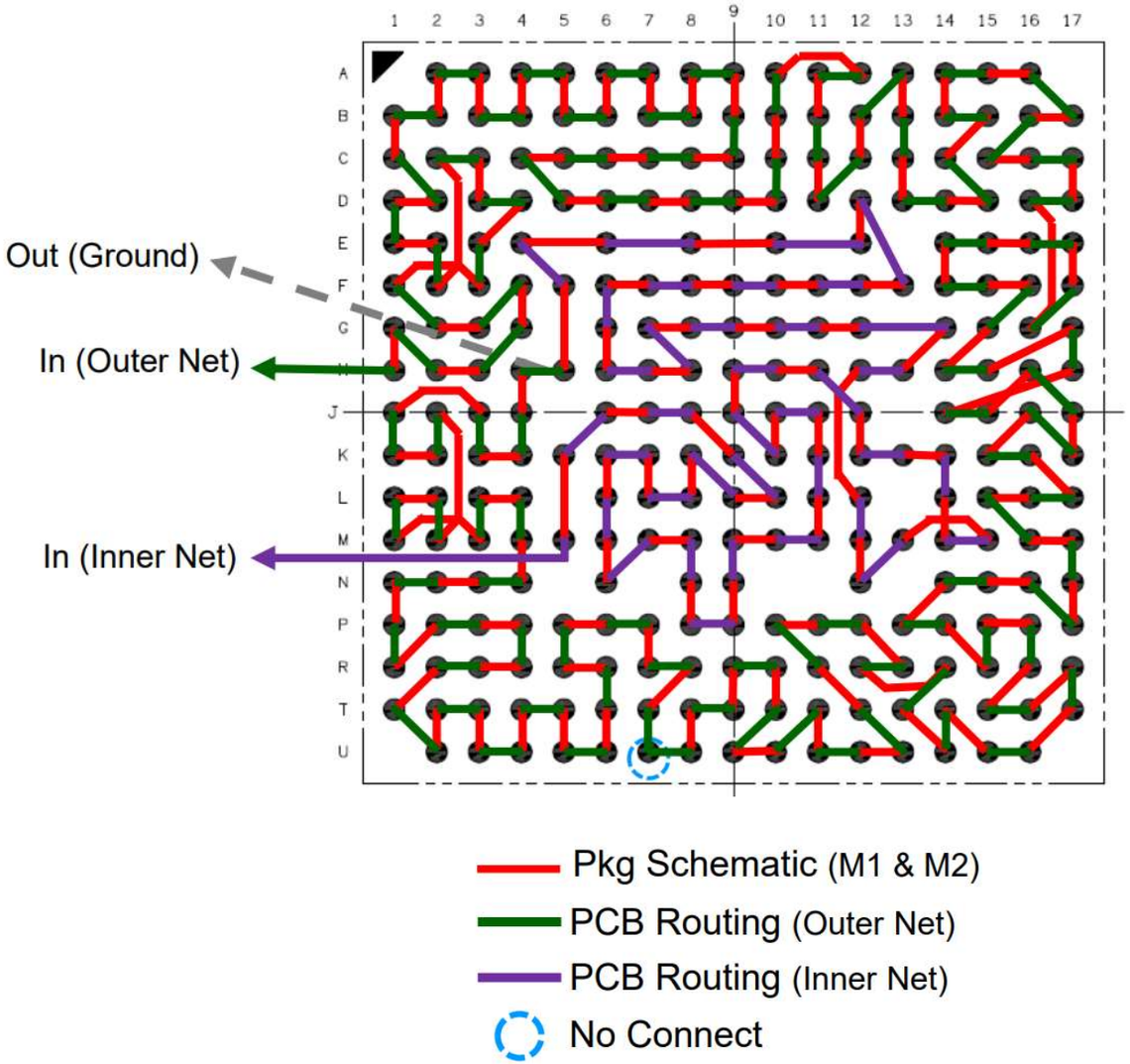
Creep Strain Energy Density per Cycle (-40C/125C)



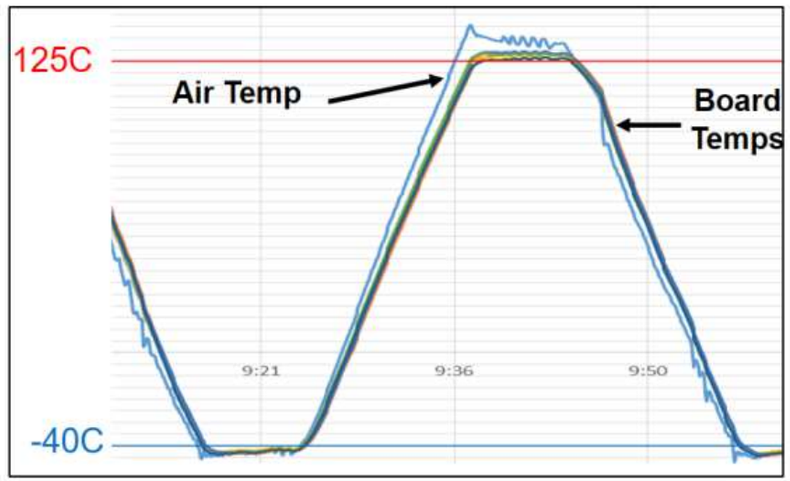
- Damage parameter: Creep strain energy density
- With corner ball depop, increased damage in neighboring corner balls is minimal.
- Solder balls near die edge and depopulated BGA area experience highest level of damage in board-level cycling.

BLR TEST METHOD

Daisy Chains through Substrate and PCB



- Single Chamber Thermal Cycling (-40/125°C, 15 minute ramp and 15 minute dwell, 1 hour cycle)



- Continuous in-situ resistance monitoring with failure when resistance ≥ 1000Ω.

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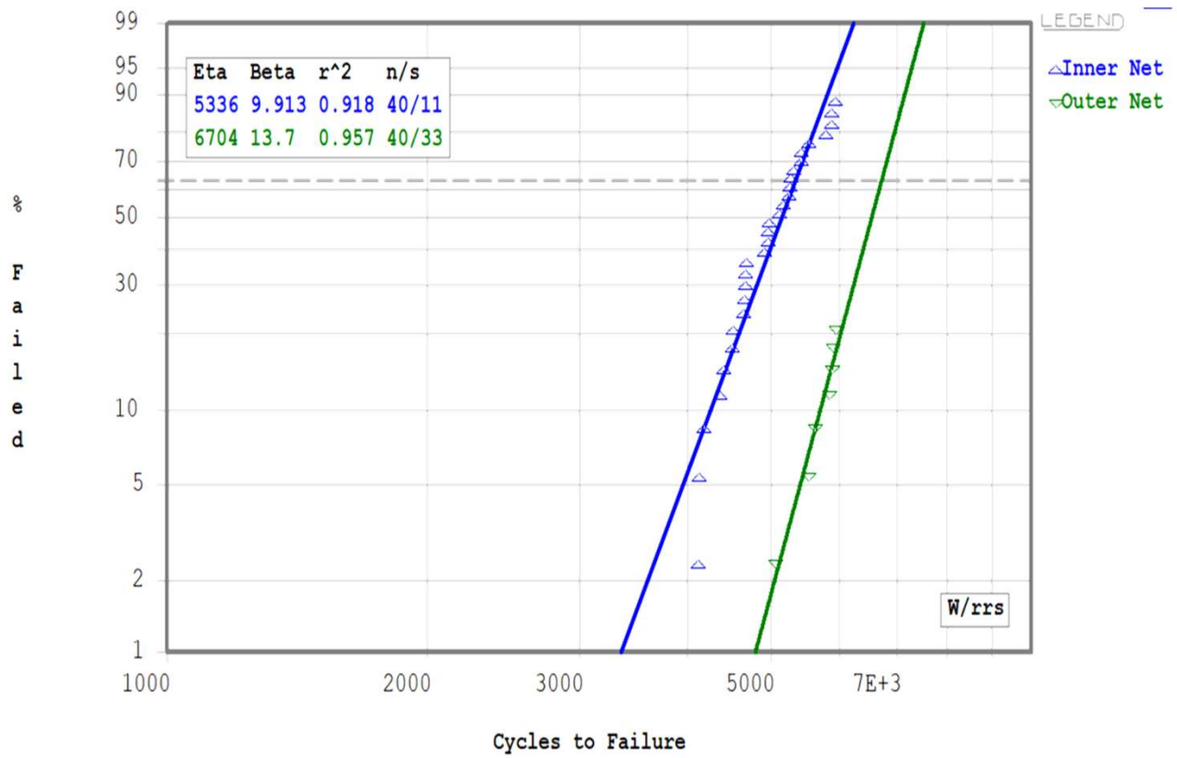
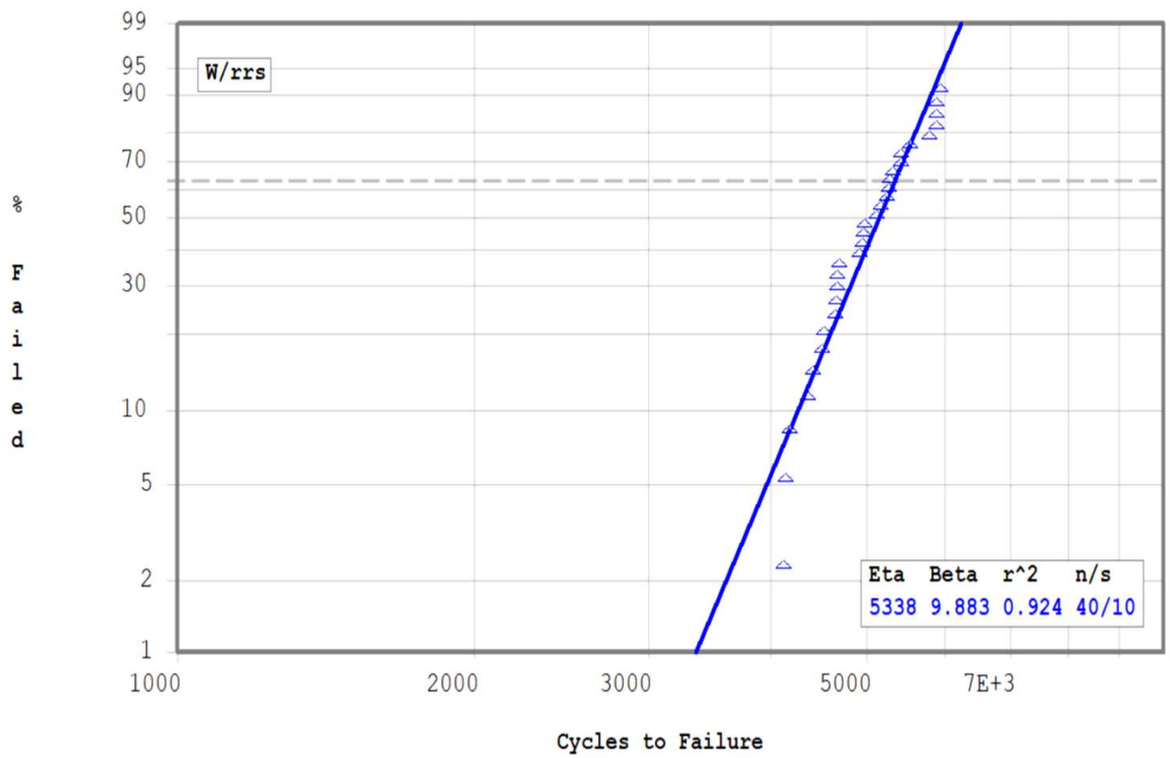
BLR WEIBULL PLOTS

Inner vs Outer Nets



Combined Nets



Net Type	First Fail (Cycles)	ETA (Cycles)
Inner Net	4124 cycles	5336 cycles
Outer Net	5055 cycles	6704 cycles
Combined	4124 cycles	5338 cycles

Exceeding internal BLR requirements for AEC G1

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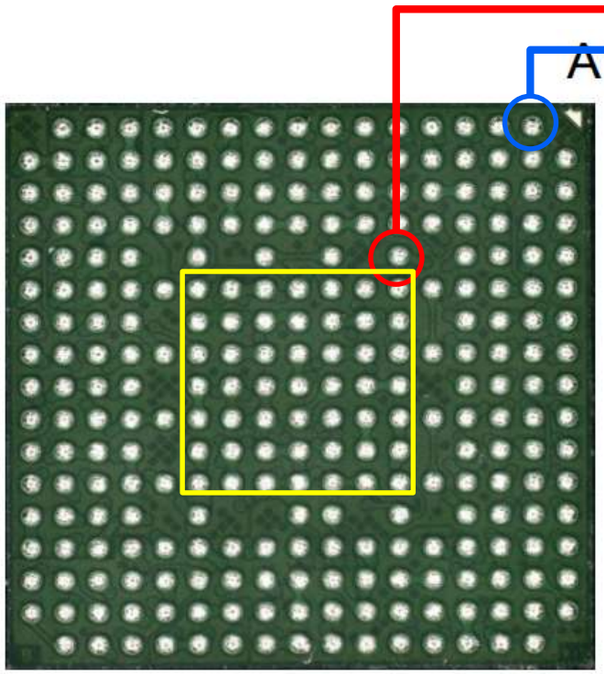
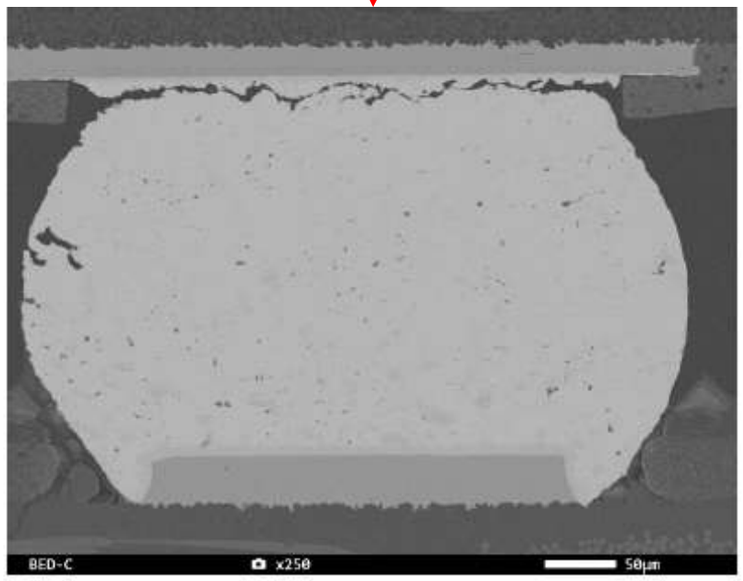
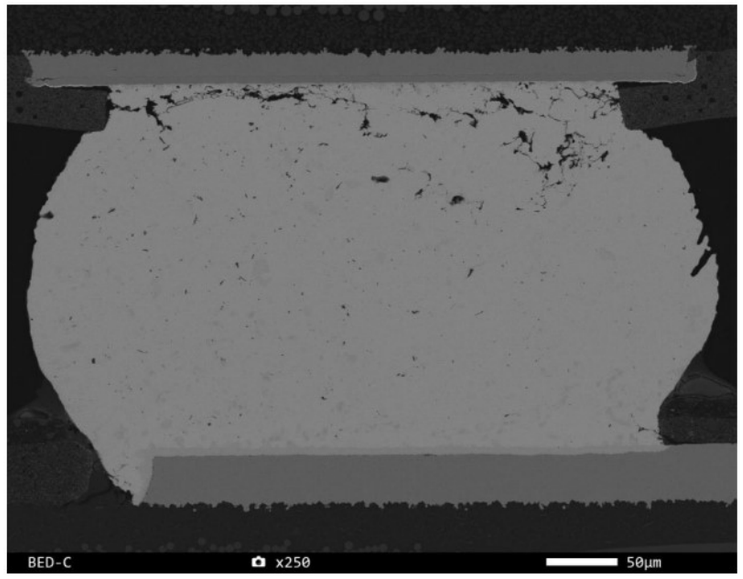
BLR BGA CROSS SECTIONS



First Fail @ 4124 Cycles



E06 - Inner Net
Complete Bulk Fracture



A02 - Outer Net
Partial Bulk Fracture

- First BGA failure occurred near die edge and near ball depopulation.
- Empirical data matches simulation.

SUMMARY

Intra-die Wire Layout Design

- Co-design between die design and assembly reduces manufacturing defects.
- IR drop simulation helps justify the implementation of high number of intra-die wires.

Intra-die Wire Process and Challenges

- Stand-off stitch bond (SSB) for intra-die wire requires two separate tail formation process, which increases the opportunity for error by a factor of 2.
- Detailed DOE's for parameter screening and optimization for bump smoothing, SSB bonding and low wire looping are required.

Package Reliability

- Package BOM exceeds AEC Grade 1 and Q006 requirements, passing 3X readpoints.
- Bump shear strength and SSB stitch pull strength observed minimal degradation at 3X package stress readpoints.

Board Level Reliability

- BLR simulation predicts the solder ball most susceptible to cyclic fatigue to be near the die edge and near the depopulated BGA area. Die:package ratio is 15%.
- Empirical study confirms simulation.

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Failure Analyses
Thammarat T. and team
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Alvin Youngblood
Roy Arldt

SECURE CONNECTIONS
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