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Warpage and Reliability Study of Large Size XDFOI™ FO-MCM fcBGA

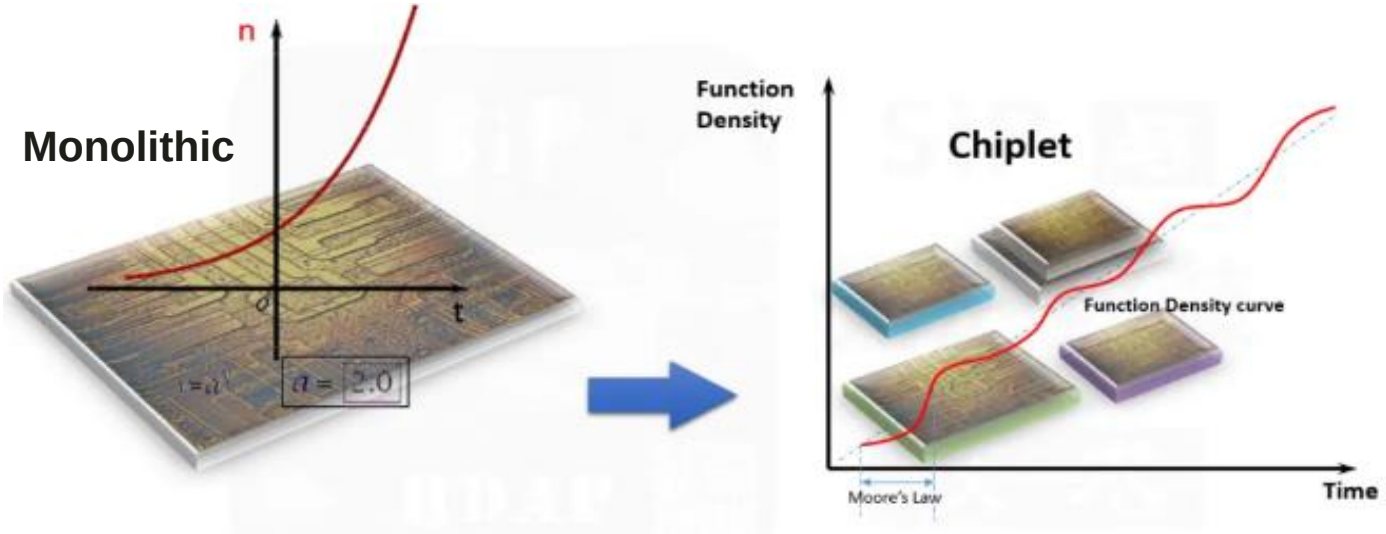
Author: Danfeng Yang, Allen Xu, Coco Xu, Yaojian Lin
Presenter: Nokibul Islam
JCET Group

Agenda

- XDFOI™ Introduction and Market
- Assembly Process
- Roadmap
- Process Level Warpage Data
- Package Level Reliability Data
- Summary

Driving Force for Packaging– “More Than Moore”

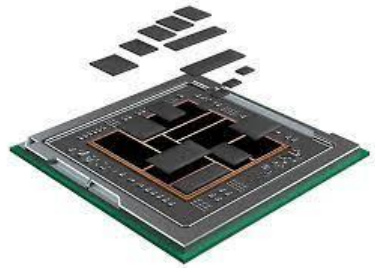
- Moore’s Law is facing problems in terms of wafer node and cost
- “More than Moore” is commonly accepted by the industry as packaging becomes more critical



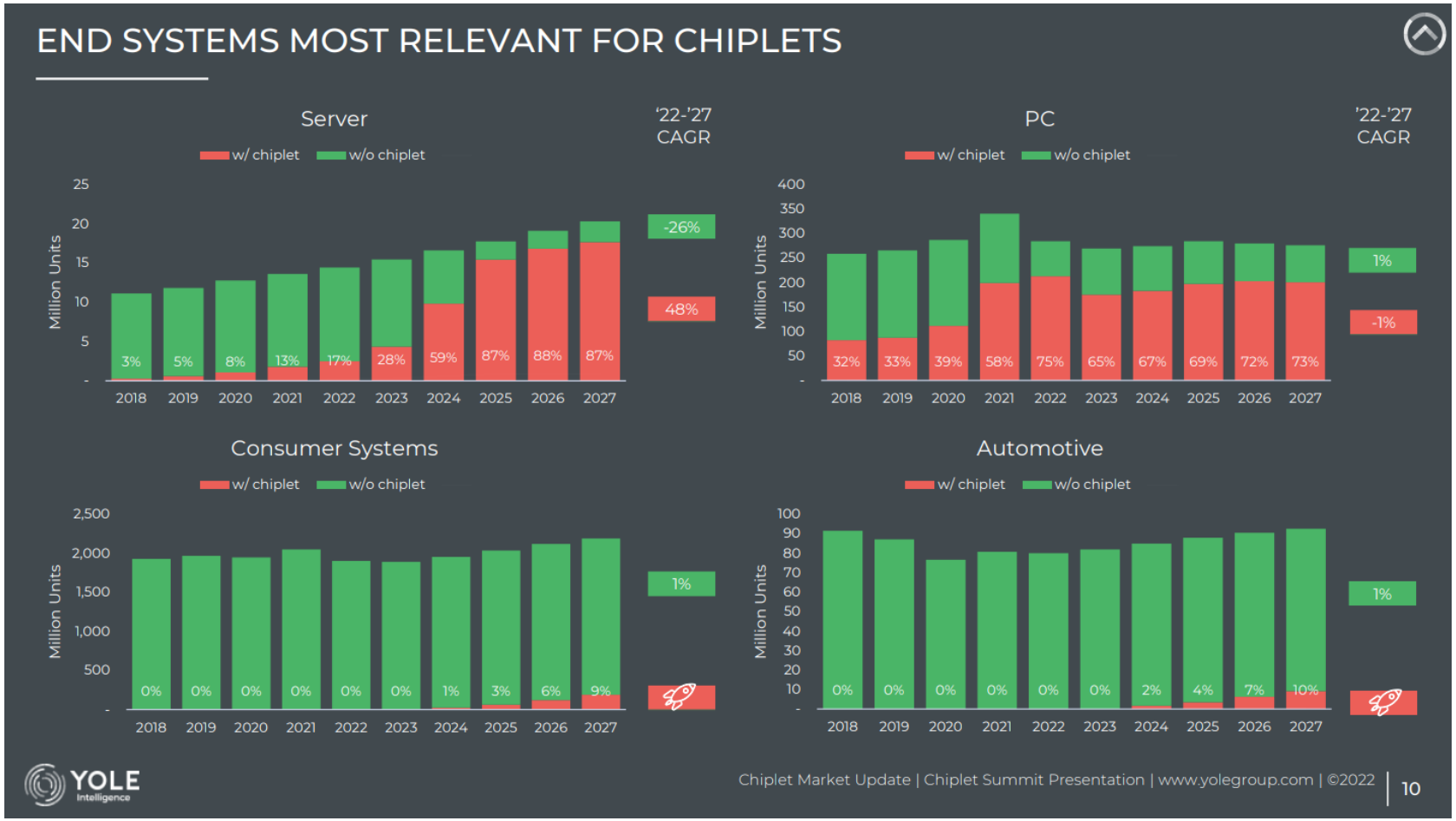
A chiplet is one part of a processing module that makes up a larger integrated circuit like a computer processor rather than manufacturing a processor on a single piece of silicon with the desired number of cores.

Chiplet advantages

Mixed process nodes (logic, analog, …)	Package reticle > 2000mm^2
Optimized cost/sqmm	Small die: High yield / Lower waste
IP-reuse, short TTM	Scalability and Flexibility



Chiplets Market Trends

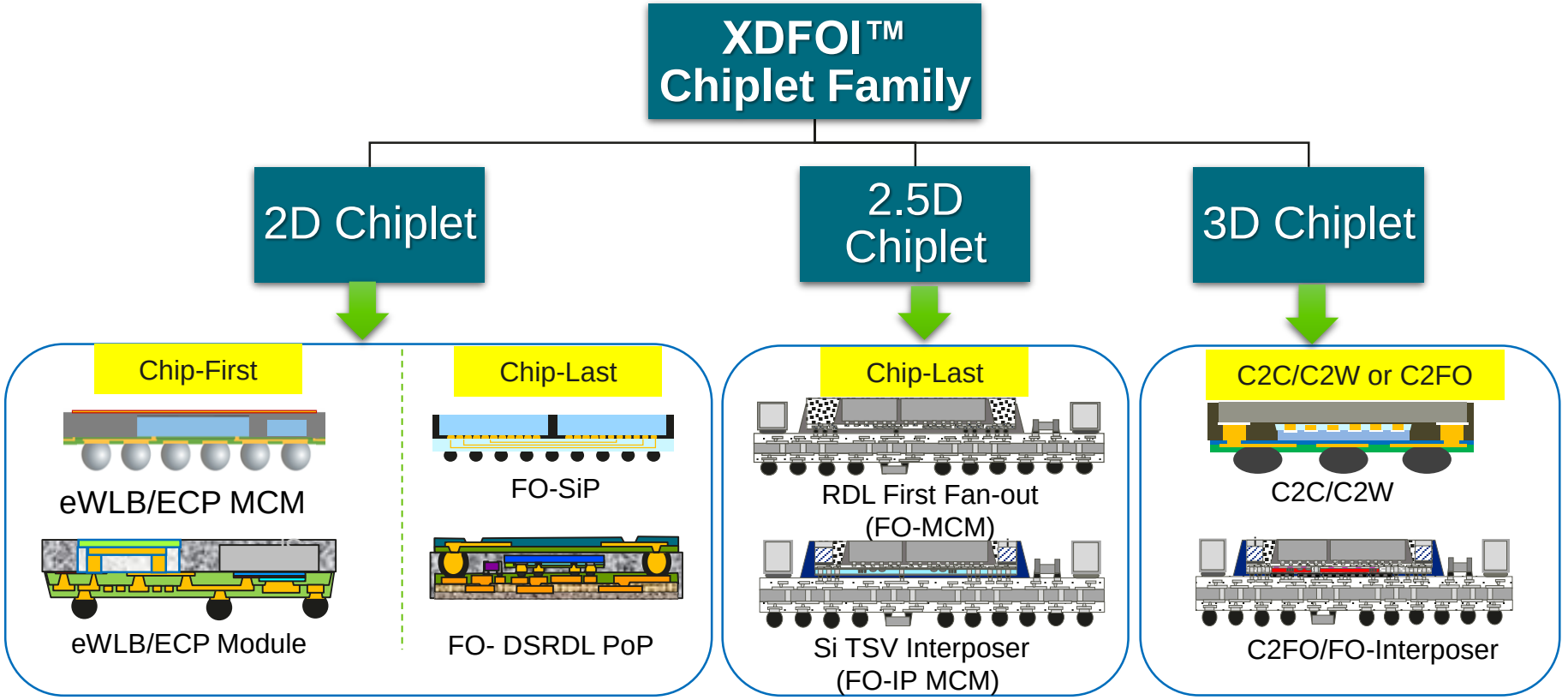


Source: Yole

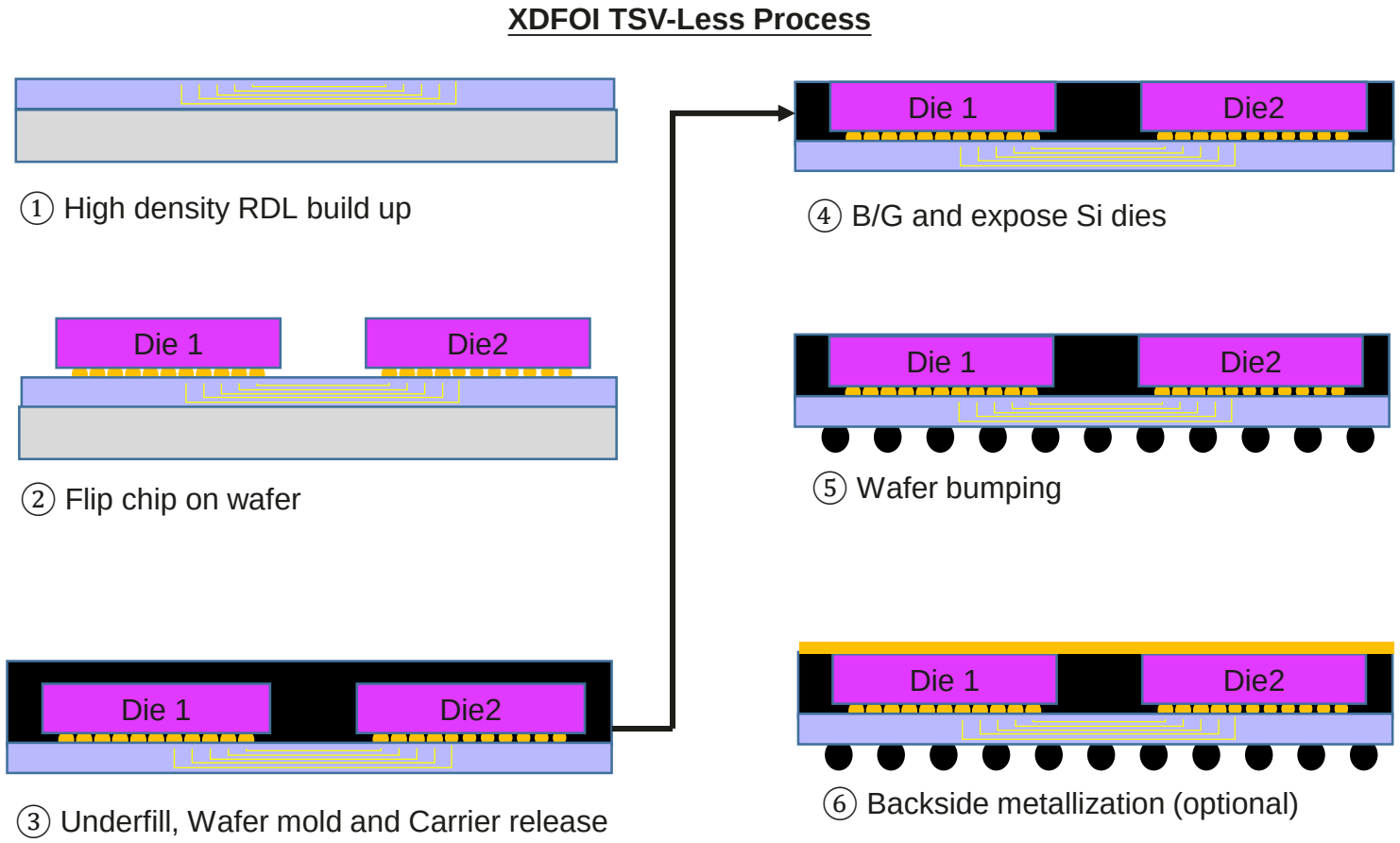
- Heterogeneous integration will play a critical role in chiplets growth
- Chiplets are expected to be one of the highest growth package categories over the next few years.
- Marketwise, the highest adoption rate is in Servers followed by PC and Automotive
- Companies like Intel, AMD, Apple, IBM, Marvell, etc. have already implemented Chiplets

What is XDFOI?

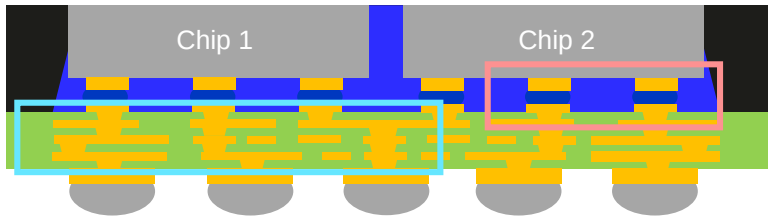
XDFOI™ (x-Dimensional Fan-Out Integration) of JCET group is a heterogeneous integration technology platform of JCET Group, which includes multiple advanced 2D/2.5D/3D chiplet MCM (multi-chip module) / SiP (System-in-Package) integration solutions.

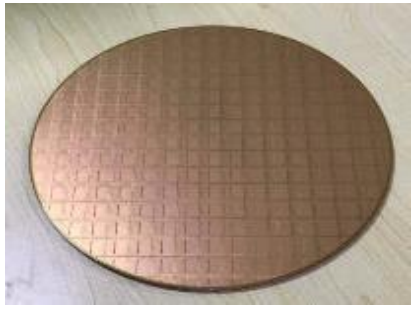


XDFOI RDL-First Assy Process Flow

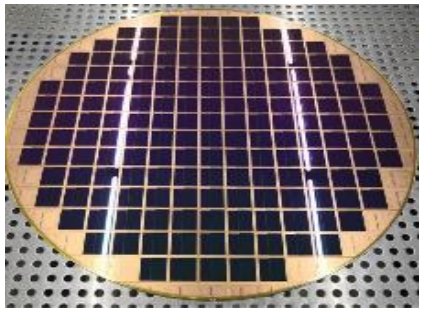


XDFOI X-Sectional Data

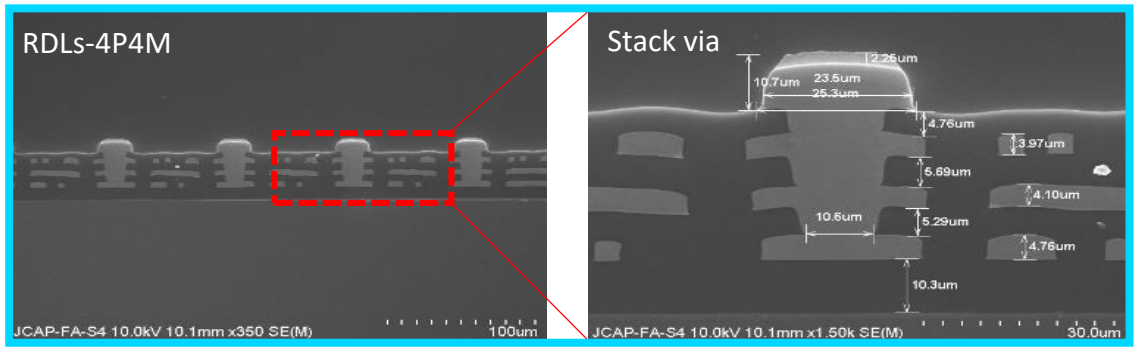


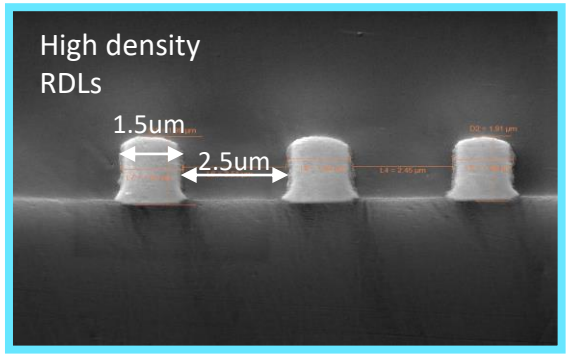


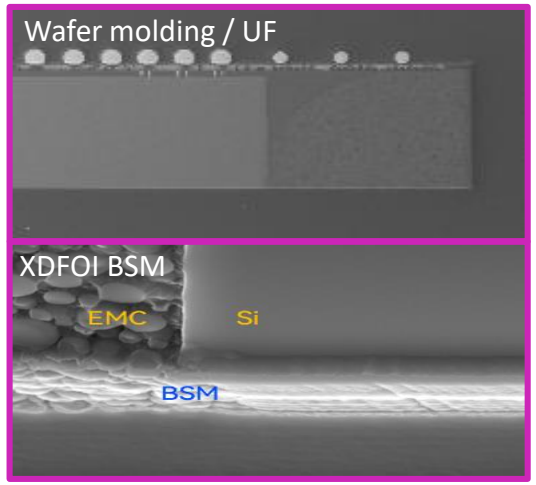
Ultra High Density RDLs

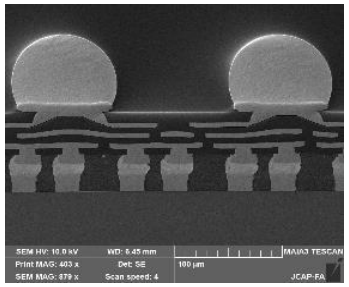


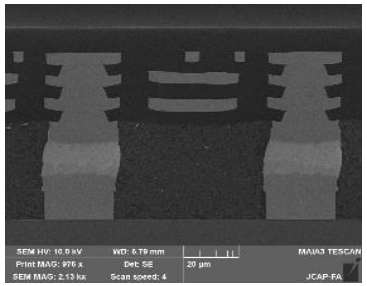
Flip Chip

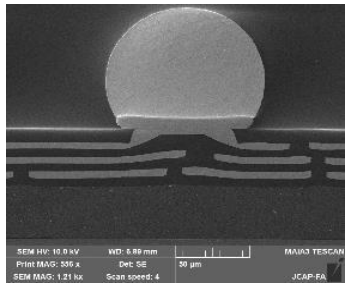




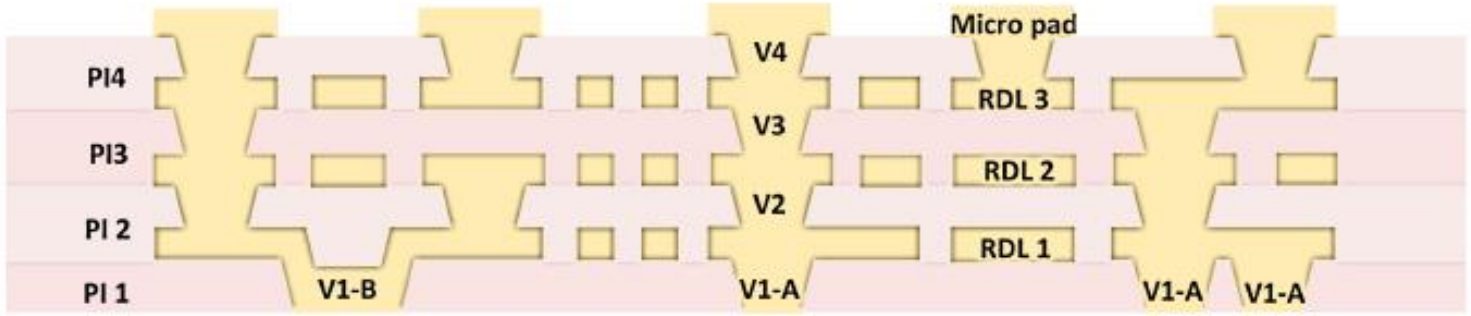


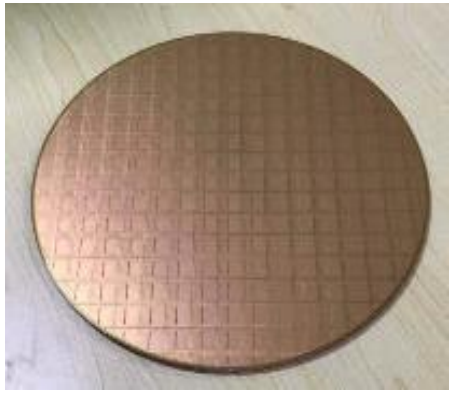






XDFOI Roadmap

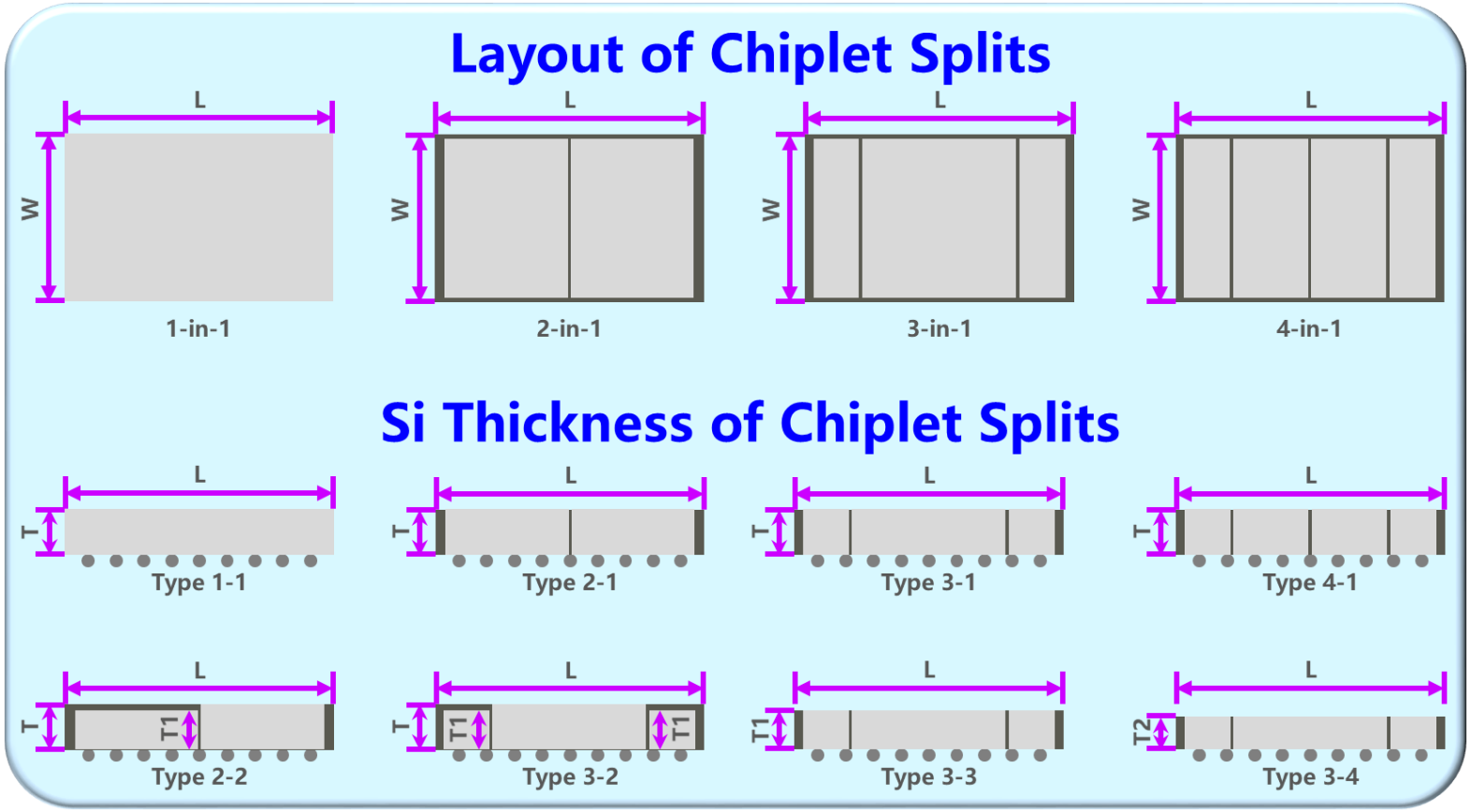


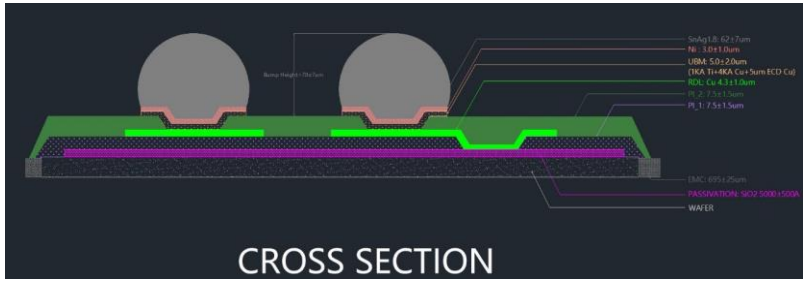


RDL Wafer

Solution	Micro bump pitch (um)	Max RDL layers	Min via size (um)	Min land size (um)	Min L/S (um)	Backside Metallization Thickness (um)	Max XDFOI size (mm)
Standard	40	5	10	20	2/2	0.75-1	44X44 (reticle size)
Advanced		6	8	17	1.5/2.5	1-10	65X65 (Y2024)

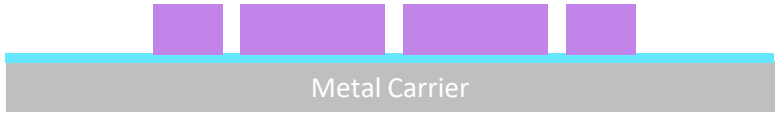
XDFOI Chiplet Structure



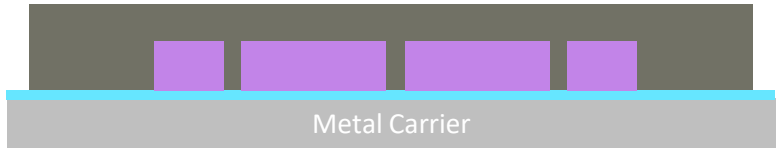


XDFOI Formation Process for 2P2M (Chip-First)

① Dicing



② Die attach

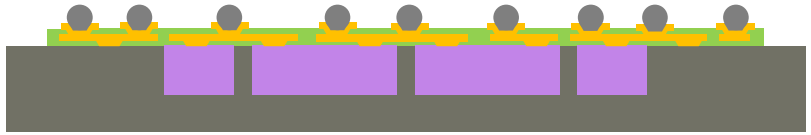


③ Molding

④ Debonding

⑤ PI 1

⑥ M 1



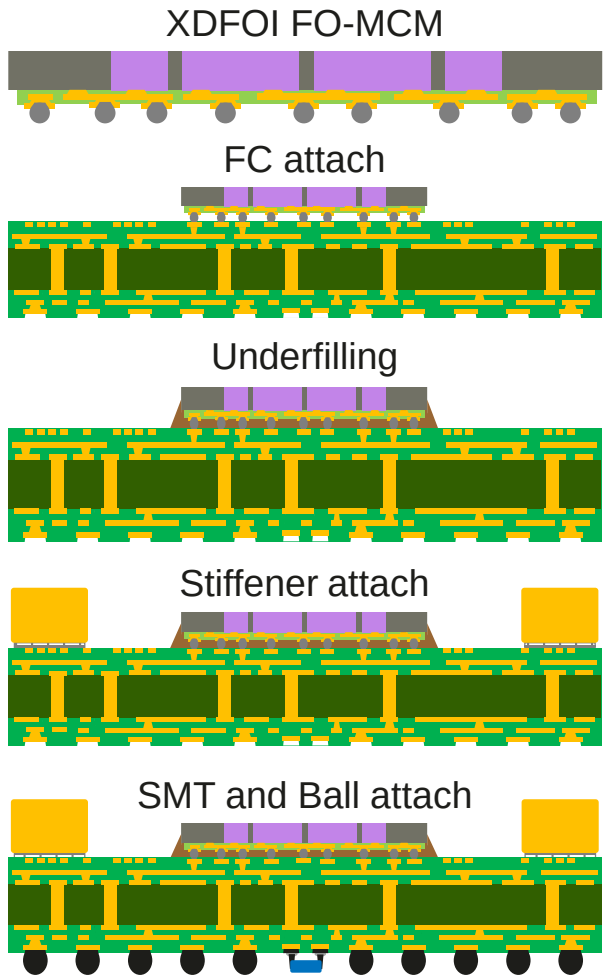
⑧ Bumping

⑨ Backgrinding

⑩ Dicing

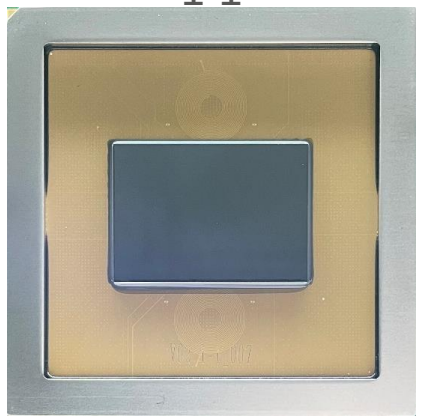
Package Attributes and FC Assy Process

Category	Item	fcBGA Parameters
Package	PKG Size	6000mm^2
	PKG Height	5.2mm
	HS type	Stiffener Ring
Die/FO	Die/FO Size	1200mm^2
	Bump Type	Solder Bump
	Min Bump Pitch	180um
	Bump Height	70um
Substrate	# of Layers	20L
	Core Thickness	1200um
	BGA Ball Pitch	0.9mm

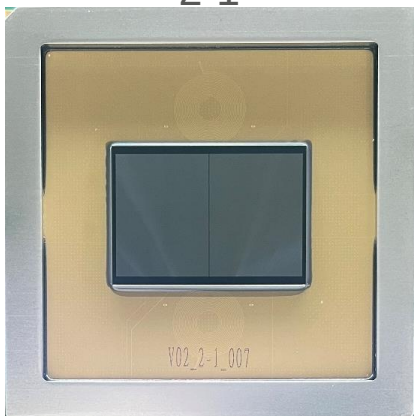


XDFOI FO-MCM fcBGA

1-1



2-1



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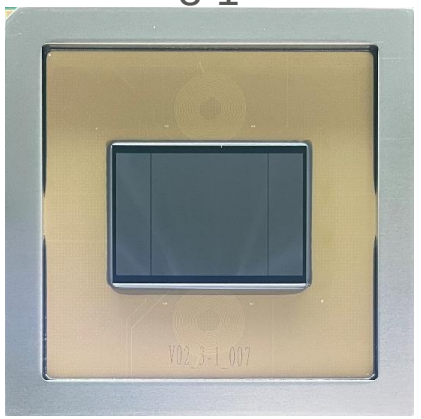

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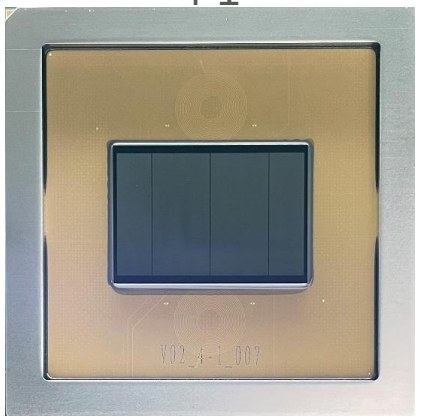
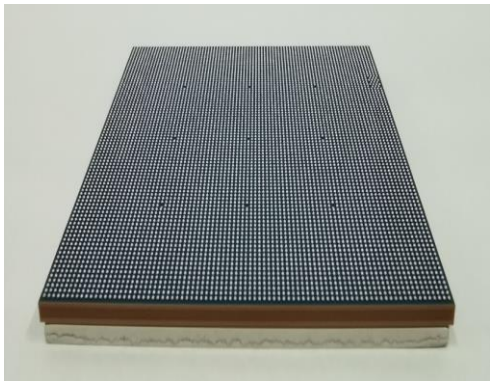
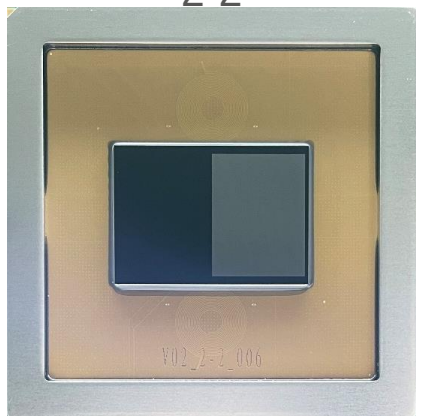




Bottom Side

2-2



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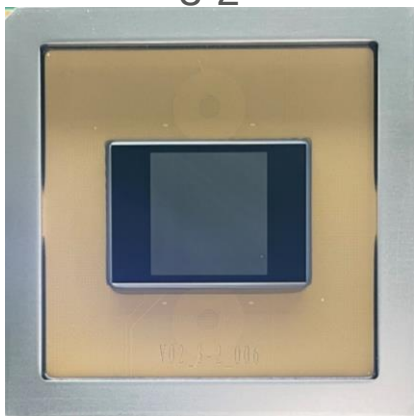

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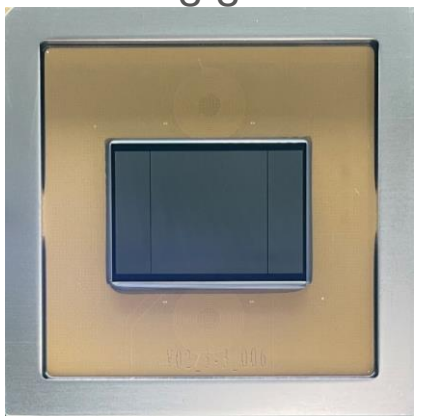

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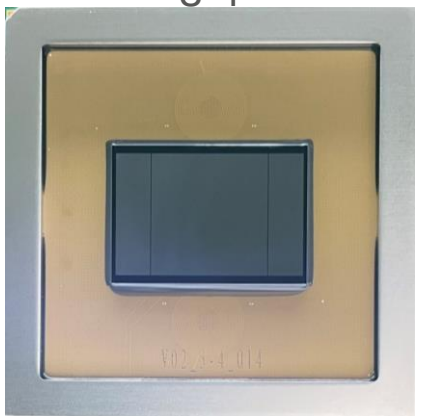
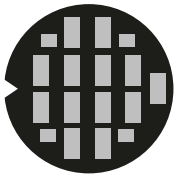
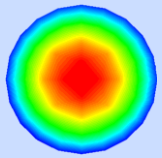
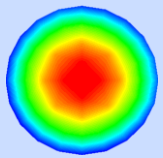
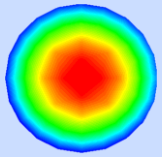
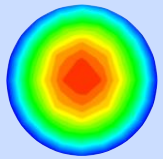
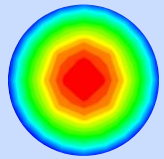
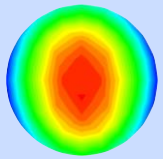
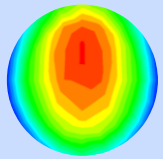


FO Process Level Warpage

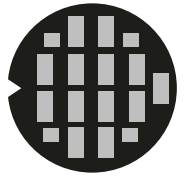


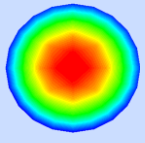
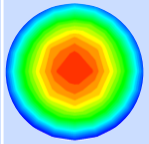
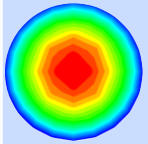
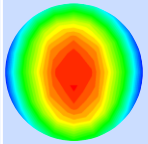
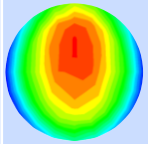
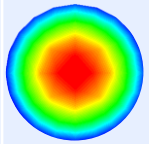
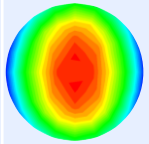
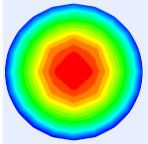
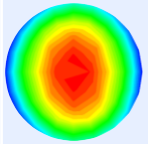
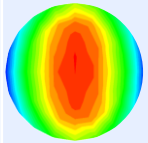
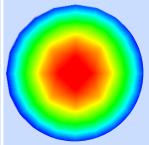
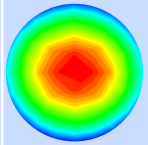
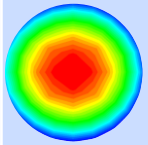
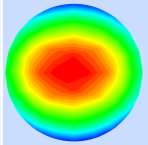
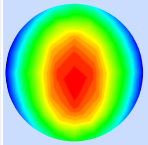
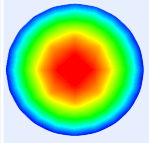
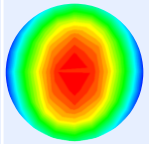
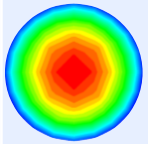
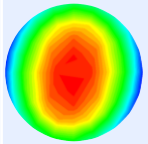
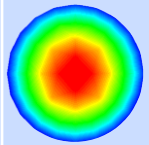
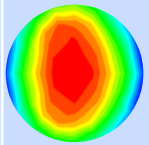
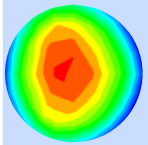
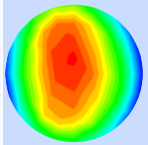
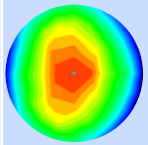
(-)Negative Warpage

Contact Plane

Warpage (mm)	Type 1-1	Type 2-1	Type 3-1	Type 4-1	Type 2-2	Type 3-2	Type 3-3	Type 3-4
Chiplet Splits	1	2	3	4	2	3	3	3
Si Thickness	T	T/T	T/T/T	T/T/T/T	T1/T	T1/T/T1	T1/T1/T1	T2/T2/T2
After Recon	NA	 -1.63	 -1.57	 -1.60	 -1.84	 -1.75	 -2.35	 -3.13

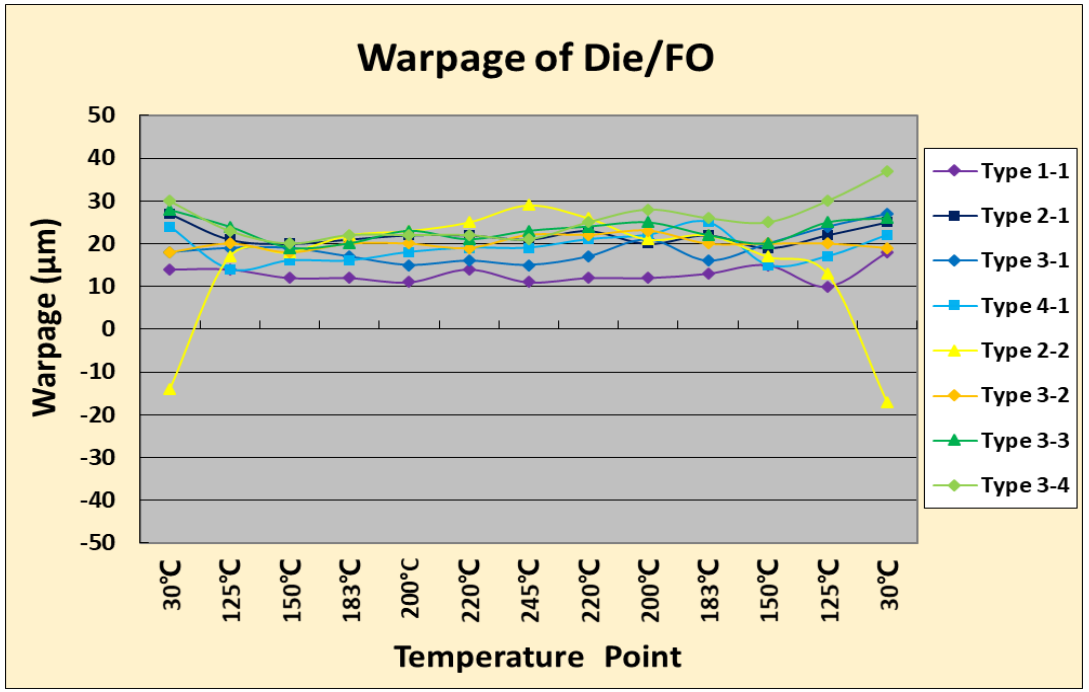
FO Process Level Warpage



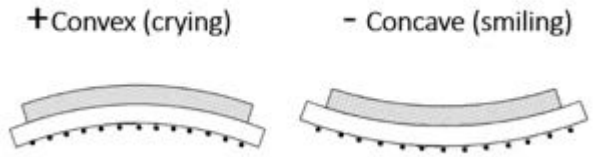
Warpage (mm)	Type 3-1	Type 2-2	Type 3-2	Type 3-3	Type 3-4
After annealing	 -1.69	 -1.84	 -1.75	 -2.35	 -3.13
After PI1	 -1.52	 -2.47	 -1.87	 -2.37	 -4.06 *
After M1	 -1.90	 -2.52	 -2.27	 -2.93	 -2.55
After PI2	 -1.50	 -2.31	 -1.79	 -2.58	missed
After M2	 -2.02	 -1.58	 -1.23	 -1.89	 -1.75

*Thickness mismatch, warpage adjustment and backgrind.

Shadow Moire Data (FO)

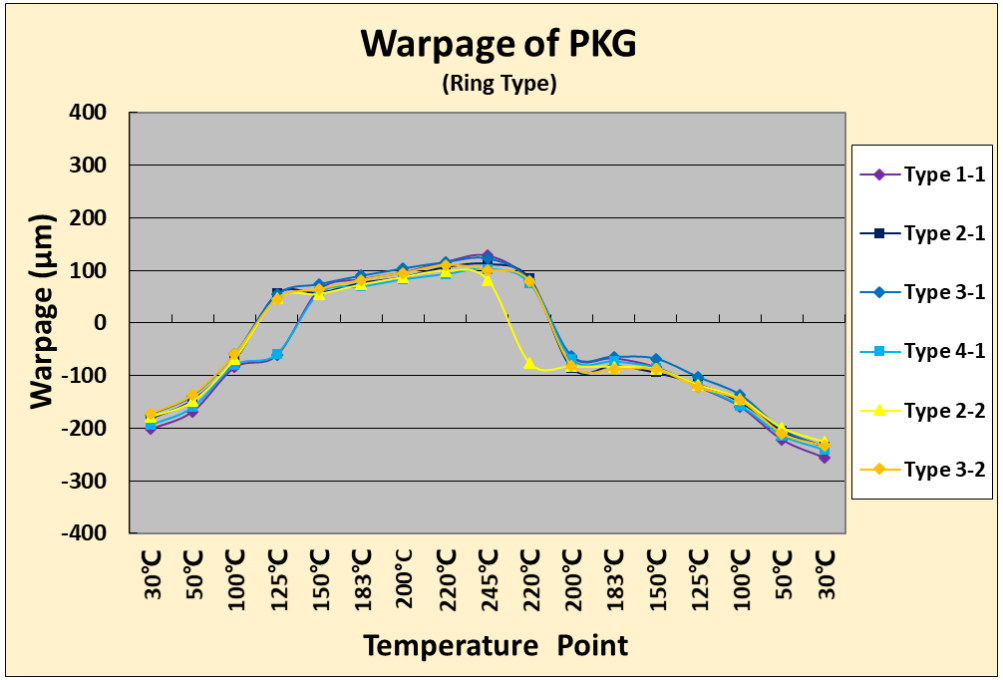


TEMP No.	30℃	125℃	150℃	183℃	200℃	220℃	245℃	220℃	200℃	183℃	150℃	125℃	30℃
Type 1-1	14	14	12	12	11	14	11	12	12	13	15	10	18
Type 2-1	27	21	20	21	22	22	21	23	20	22	19	22	25
Type 3-1	18	19	19	17	15	16	15	17	21	16	20	24	27
Type 4-1	24	14	16	16	18	19	19	21	22	25	15	17	22
Type 2-2	-14	17	18	22	23	25	29	26	21	22	17	13	-17
Type 3-2	18	20	18	20	20	19	22	22	23	20	20	20	19
Type 3-3	28	24	19	20	23	21	23	24	25	22	20	25	26
Type 3-4	30	23	20	22	22	22	21	25	28	26	25	30	37

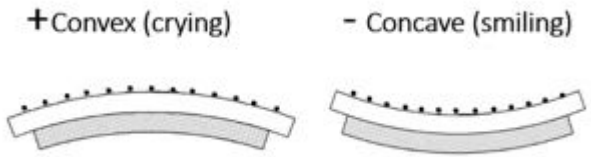


Remark:
1)Sample size, 3ea/type;
2)Backside up (bump side down);
3)Die/FO area.

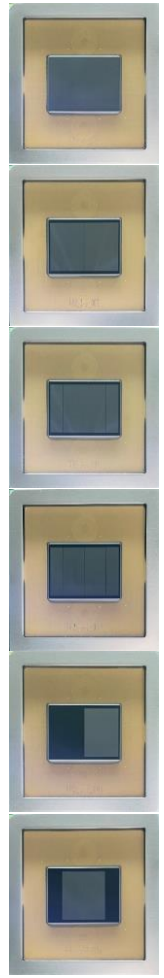
Shadow Moire Data after FC Assy



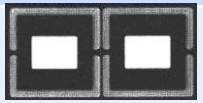
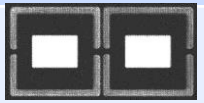
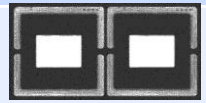
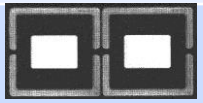
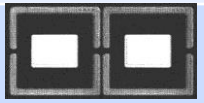
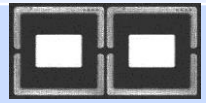
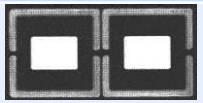
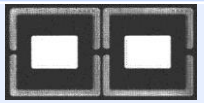
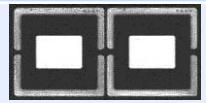
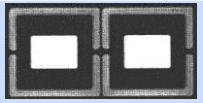
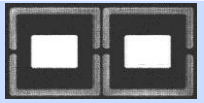
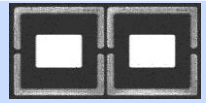
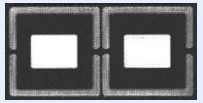
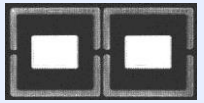
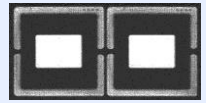
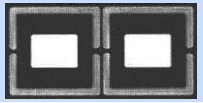
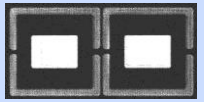
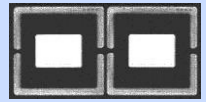
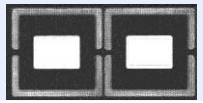
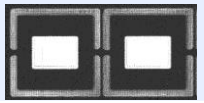
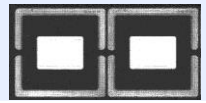
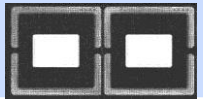
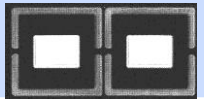
TEMP No.	30℃	50℃	100℃	125℃	150℃	183℃	200℃	220℃	245℃	220℃	200℃	183℃	150℃	125℃	100℃	50℃	30℃
Type 1-1	-202	-168	-84	-61	63	83	96	116	128	79	-64	-67	-84	-121	-159	-222	-256
Type 2-1	-181	-146	-70	56	58	77	88	107	113	85	-85	-81	-94	-116	-150	-205	-235
Type 3-1	-174	-138	-59	54	74	90	104	116	123	81	-63	-64	-68	-103	-137	-203	-236
Type 4-1	-194	-160	-80	-59	57	69	83	93	103	76	-69	-73	-85	-120	-157	-214	-241
Type 2-2	-178	-148	-68	47	55	73	87	99	82	-76	-82	-83	-87	-117	-144	-199	-225
Type 3-2	-172	-136	-59	46	64	82	95	110	101	79	-81	-88	-88	-122	-147	-210	-233



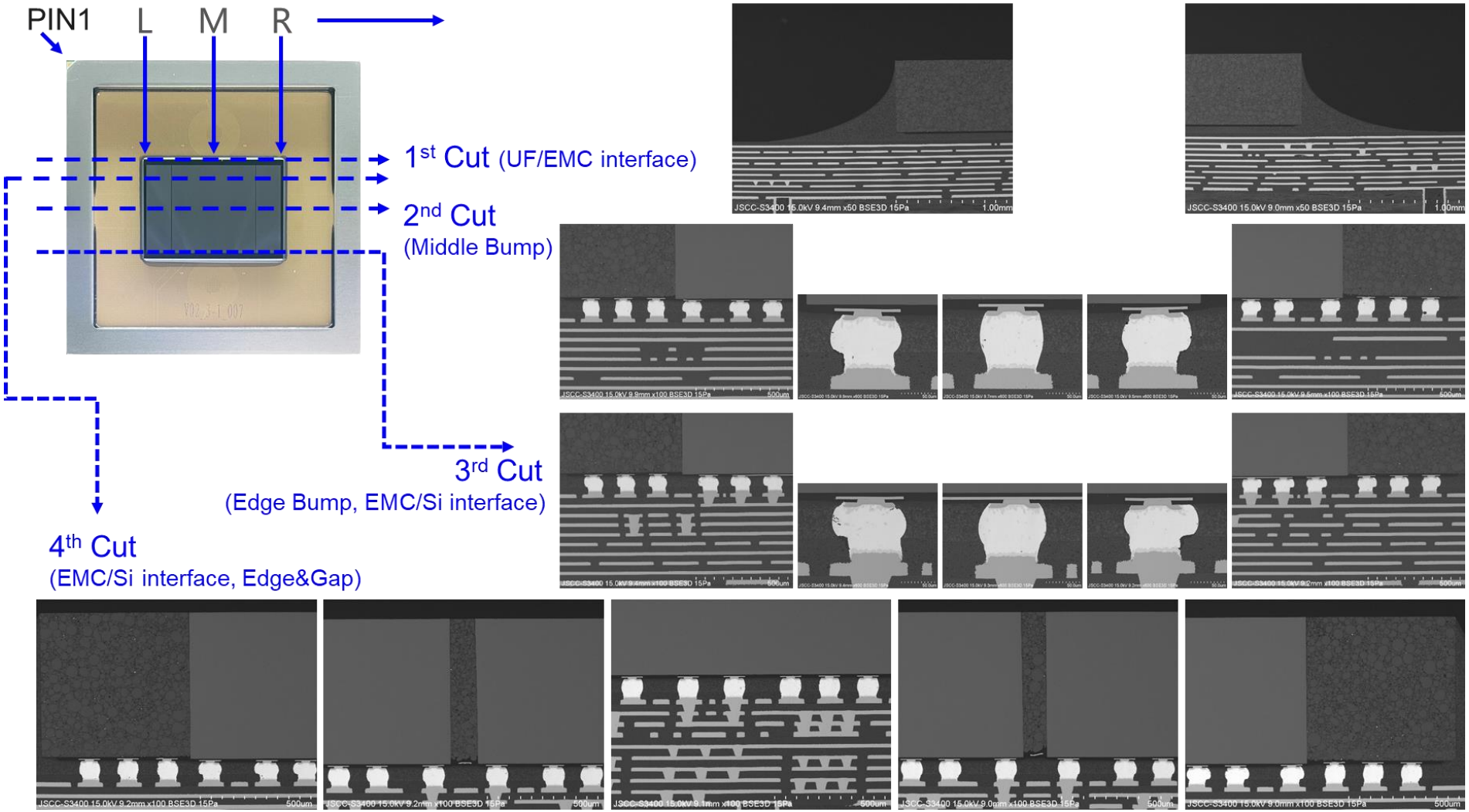
Remark:
1)Sample size, 1ea/type;
2)BOT side up;
3)Substrate area.



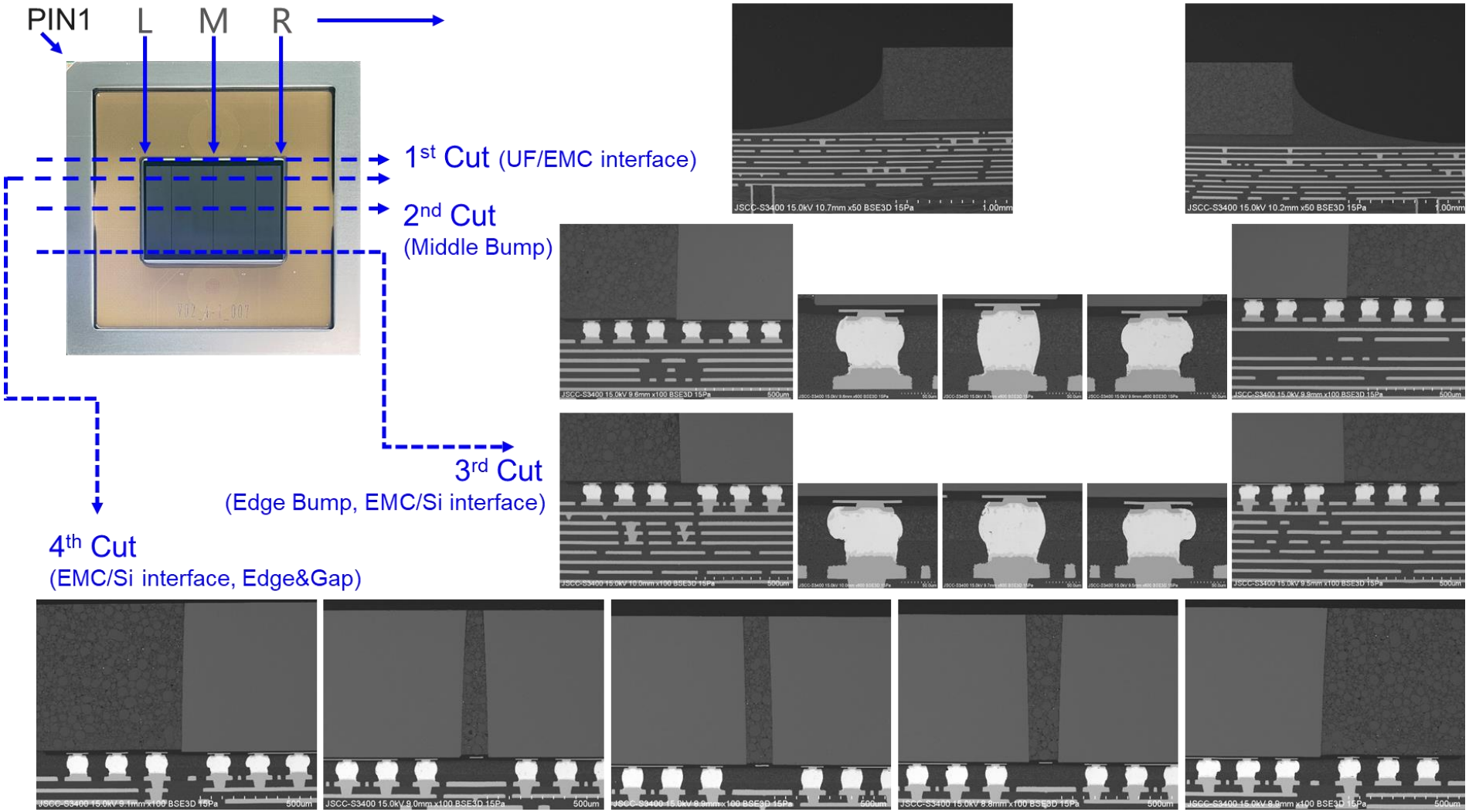
Accelerated Reliability Results

XDFOI™ Type	T0		After MSL4		After TC1000cycles	
	OS	SAT	OS	SAT	OS	SAT
Type 1-1	Pass		Pass		Pass	
Type 2-1	Pass		Pass		Pass	
Type 3-1	Pass		Pass		Pass	
Type 4-1	Pass		Pass		Pass	
Type 2-2	Pass		Pass		Pass	
Type 3-2	Pass		Pass		Pass	
Type 3-3	Pass		Pass		Pass	
Type 3-4	Pass		Pass		Pass	

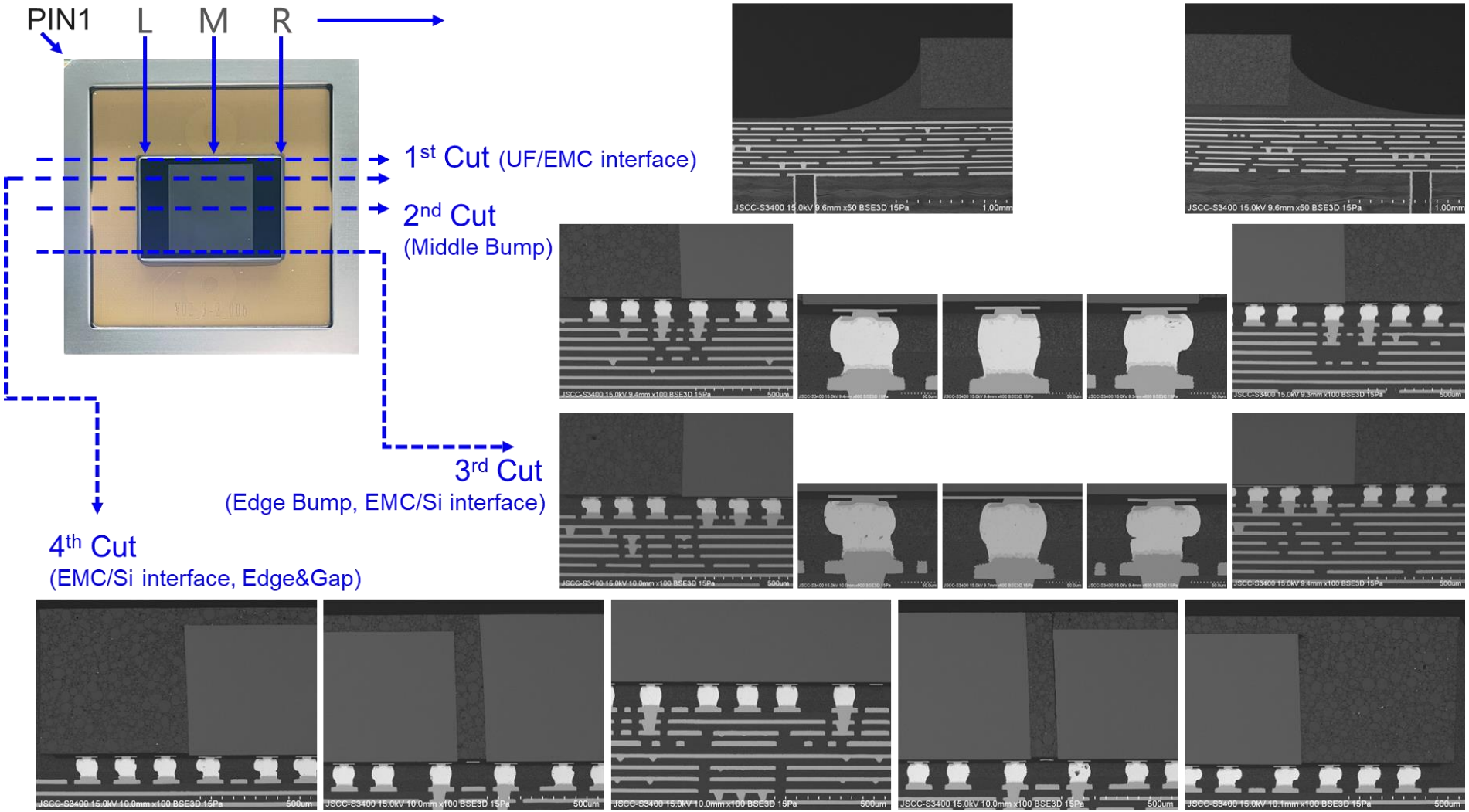
Failure Analysis after TC1000cycles (Type 3-1)



Failure Analysis after TC1000cycles (Type 4-1)



Failure Analysis after TC1000cycles (Type 3-2)



Summary

- Heterogeneous integration is an attractive and widely accepted technology for high performance packaging.
- Chip-first XDFOI FO-MCM are designed to address all the above requirements for high performance chiplet package solutions.
- As part of the XDFOI process flow, warpage data and package level reliability data are collected and analyzed for this high performance package.
- Design flexibility, time to market, expense, and supply-chain bottleneck can be significantly reduced with XDFOI technology.
- Further development is ongoing to expand the capability window of the technology.

19TH INTERNATIONAL CONFERENCE & EXHIBITION ON
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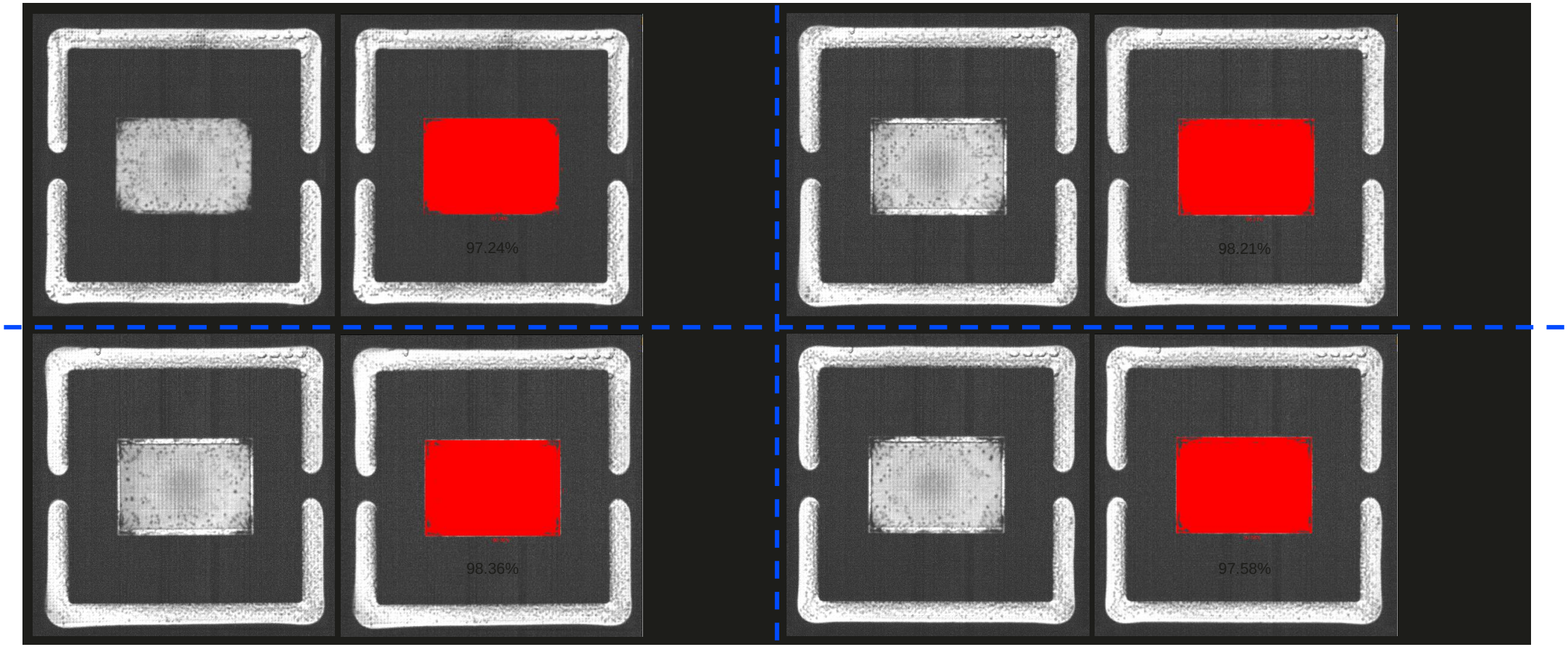
Thank You!

Lid Attach Process

TIM coverage: >90% Die Area

Type 1-1

Type 2-1



Type 3-1

Type 4-1