Advanced Glass Carriers for Buildup Structure Warp Control and Wafer Ultra-thinning

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Corning Incorporated

Outline

- Introduction
- Warp control for buildup structures
  - Fundamentals
  - Simulation examples
- Wafter ultra-thinning
  - ALoT – advanced lift-off technology
  - Ultra-low-TTV glass carrier
  - Results
- Conclusions

Founded:
1851

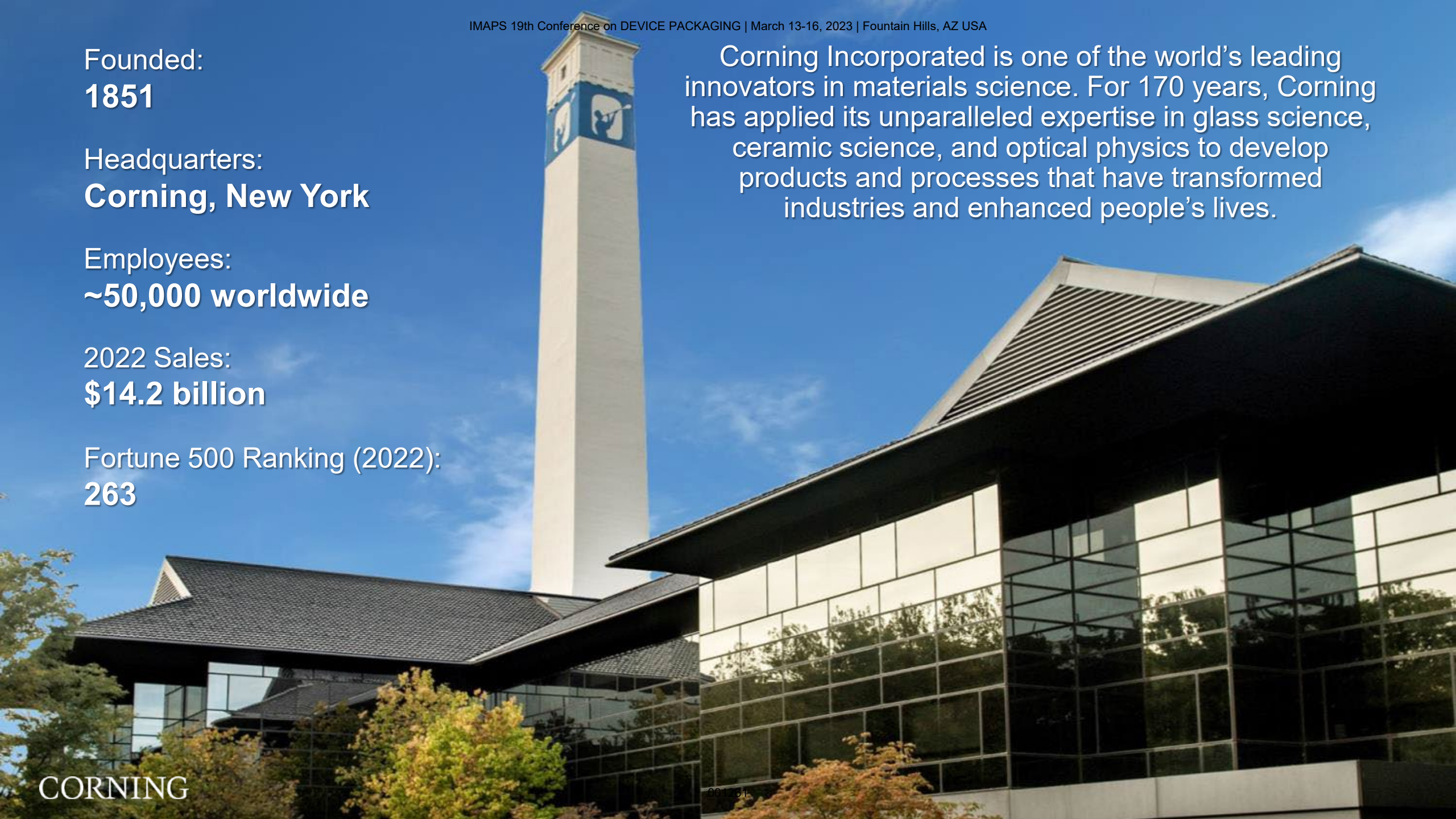
Headquarters:
Corning, New York

Employees:
~50,000 worldwide

2022 Sales:
$14.2 billion

Fortune 500 Ranking (2022):
263

Corning Incorporated is one of the world's leading innovators in materials science. For 170 years, Corning has applied its unparalleled expertise in glass science, ceramic science, and optical physics to develop products and processes that have transformed industries and enhanced people's lives.



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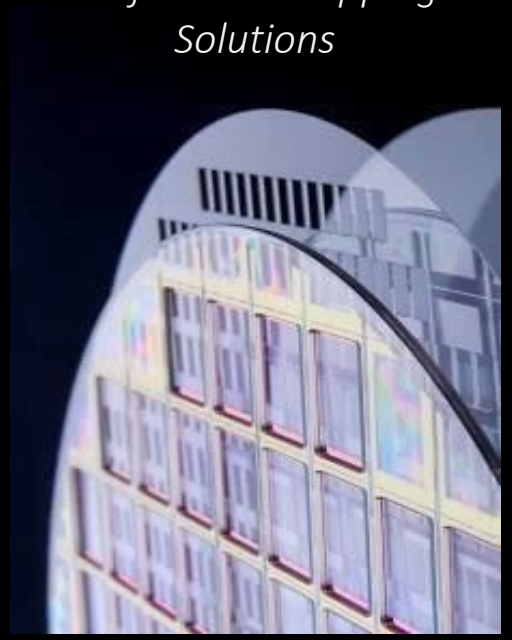
Precision Glass Solutions

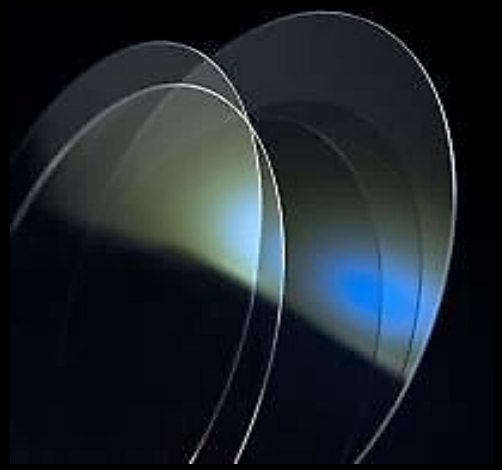
Corning Precision Glass Solutions offers industry-leading wafer and panel format glass-based solutions.

Our products help customers deliver increasingly demanding functionality and form factor requirements in consumer devices and Internet of Things (IoT) applications.

Wafer-Level Capping Solutions



Wafer-Level Optic Solutions



Augmented Reality Solutions

Carrier Solutions

Custom Glass Solutions

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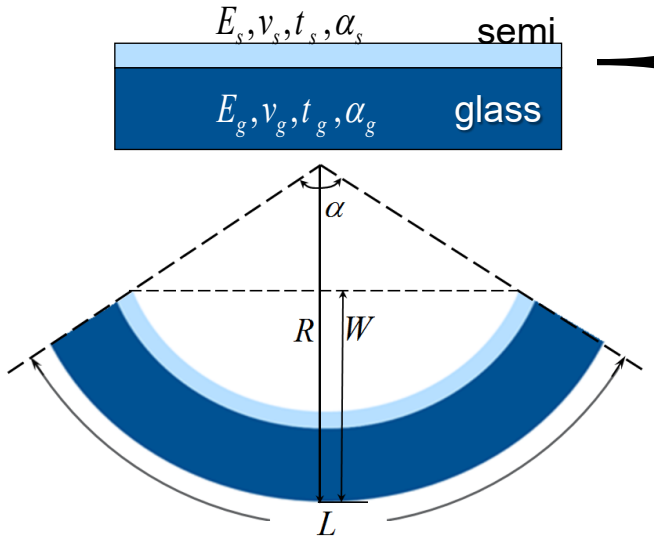
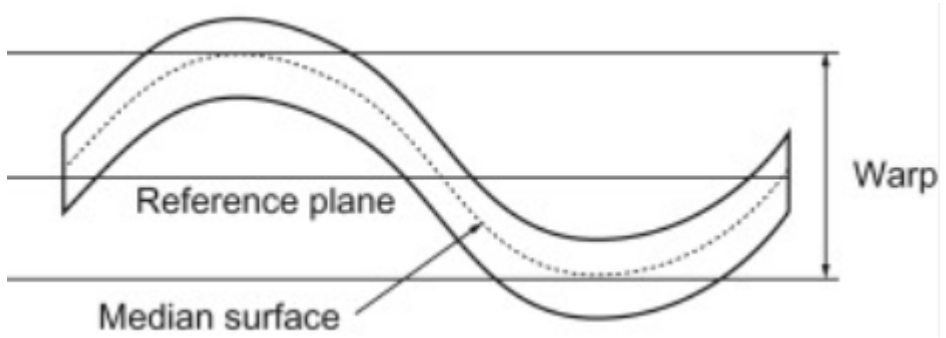
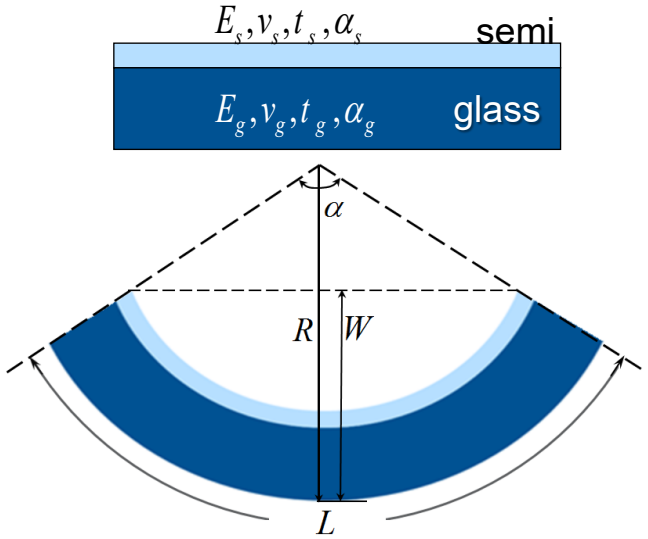
Definition of a buildup structure and warp



- Buildup structure on glass
  - Laminate of metal and dielectric
  - Epoxy molding compound w/ Si
  - Adhesive layer
  - Any combination of the above



CTE mismatch causes in-process warp



Under typical buildup conditions, in-process warp follows a simplified formula showing its dependence on:

1. CTE mismatch between glass & the composite semi material
2. Inverse of glass Young's modulus
3. Inverse of square of glass thickness

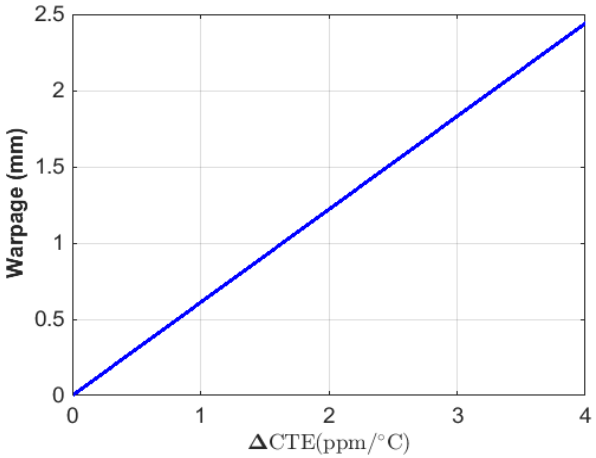
} *Both deliver "Stiffness"*

$$\approx 0.75 L^2 \Delta\alpha \Delta T \frac{E_s(1-v_g)}{E_g(1-v_s)} \frac{t_s}{t_g^2}$$

E : Young's modulus; ν : Poisson's ratio; t: Glass thickness;
α : Coefficient of thermal expansion; T : Temperature.
g: glass; s: semiconductor layers (MC + redistribution layers + die)

Three glass-based levers to minimize in-process warp

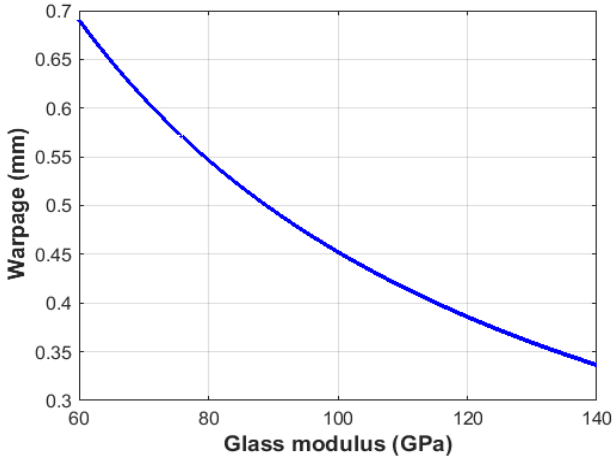
1. Decrease Δ CTE



$E_g = 70\text{GPa}$; $E_s = 20\text{GPa}$;
$\nu_g = 0.22$; $\nu_s = 0.35$;
$t_g = 1.1\text{mm}$; $t_s = 0.15\text{mm}$;
$T_{room} = 20°\text{C}$; $T_{process} = 250°\text{C}$;

Challenge: Package CTE changes throughout processing

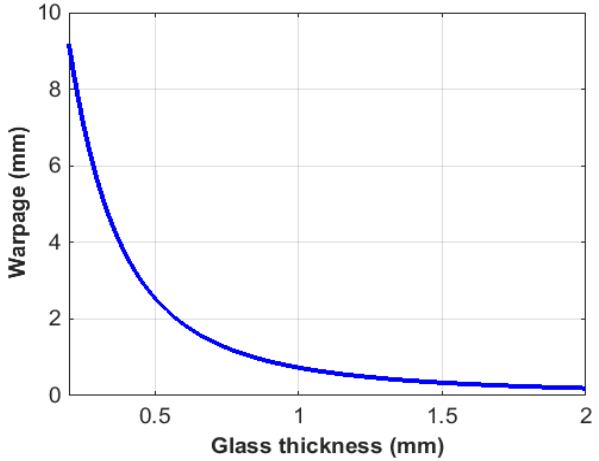
2. Increase modulus



$E_s = 20\text{GPa}$;
$\nu_g = 0.22$; $\nu_s = 0.35$;
$t_g = 1.1\text{mm}$; $t_s = 0.15\text{mm}$;
$\Delta\text{CTE} = 1.0\text{ppm}/°\text{C}$;
$T_{room} = 20°\text{C}$; $T_{process} = 250°\text{C}$;

Challenge: Thermal shock risk if Young's modulus is too high, especially for high CTE

3. Increase thickness



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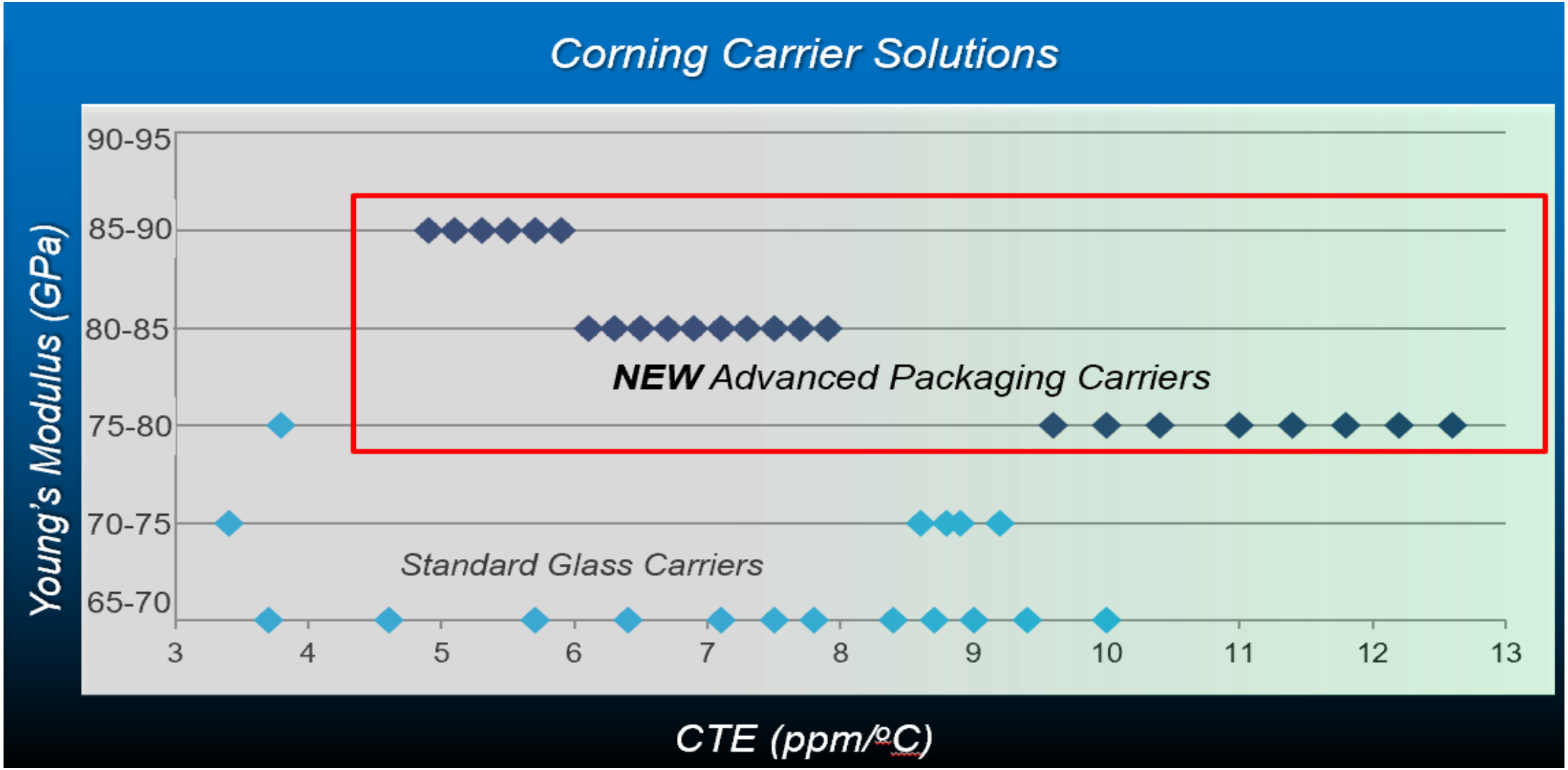
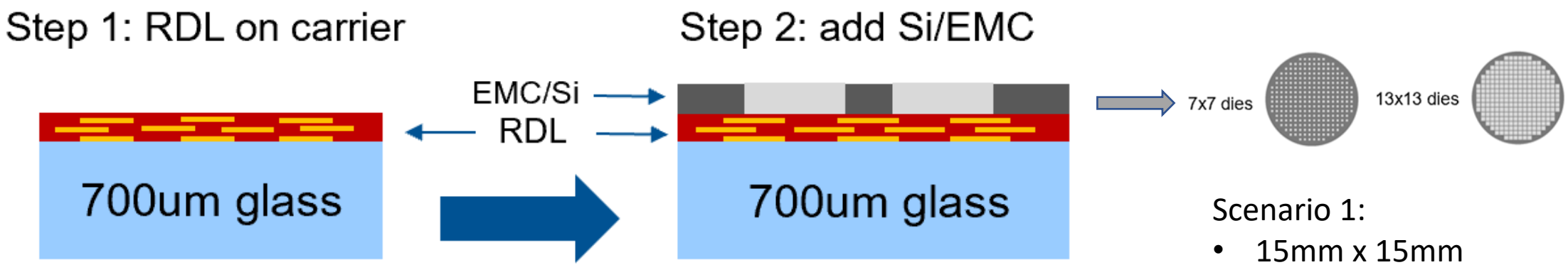
Challenge: Equipment can only accommodate certain maximum thickness

Corning glass covers broad CTE range and fine granularity



Simulation case 1: RDL-first fanout in two FO ratio scenarios



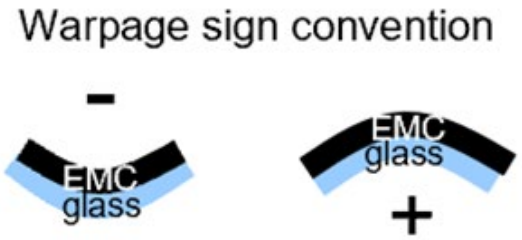
	Glass	Dielectric	Copper	EMC	Si
Young's modulus (GPa)	80.0	0.9	117.0	18.5	Anisotropic
CTE (ppm/K)	4.0/8.0/12.6	80.0	17.0	9.0	2.6
Poisson's ratio	0.22	0.30	0.34	0.30	Anisotropic
Density (g/cc)	2.4	1.0	9.0	1.0	2.3

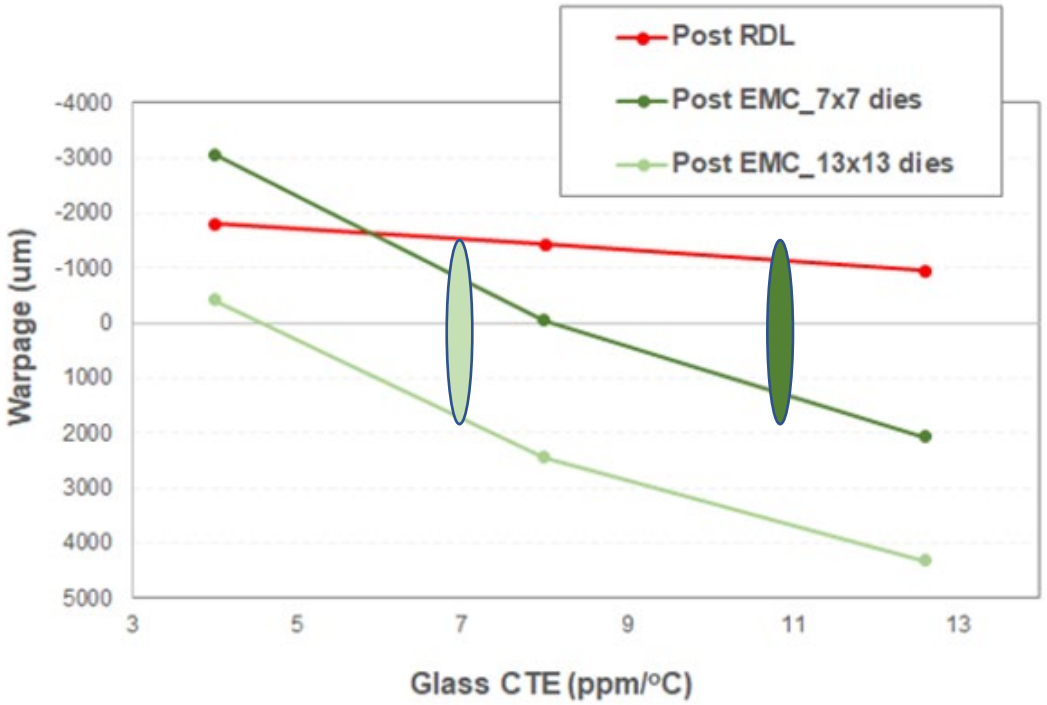
Scenario 1:
- 15mm x 15mm package size
- 7mm x7mm die size

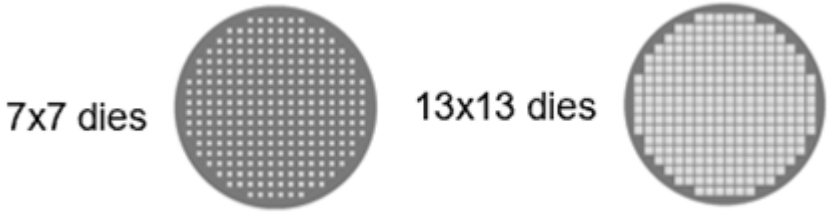
Scenario 2:
- 15mm x 15mm package size
- 13mm x 13mm die size

Reference: Z. Chen et al, "Package Level Warpage Simulation of Fan-out Wafer Level Package (FOWLP) Considering Viscoelastic Material Properties", EPTC, 2018

Simulation case 1: RDL-first fanout in two FO ratio scenarios







- Post RDL shows smiley face bow due to higher Cu and PI CTE than carrier
- Adding Si and EMC flips bow direction due to lower CTE of Si and EMC
- Single carrier CTE choice should keep maximum bow within equipment tolerance: ~11 ppm/C for high FO ratio and ~7 ppm/C for low FO ratio

Simulation case 2: multilayer organic (MLO)

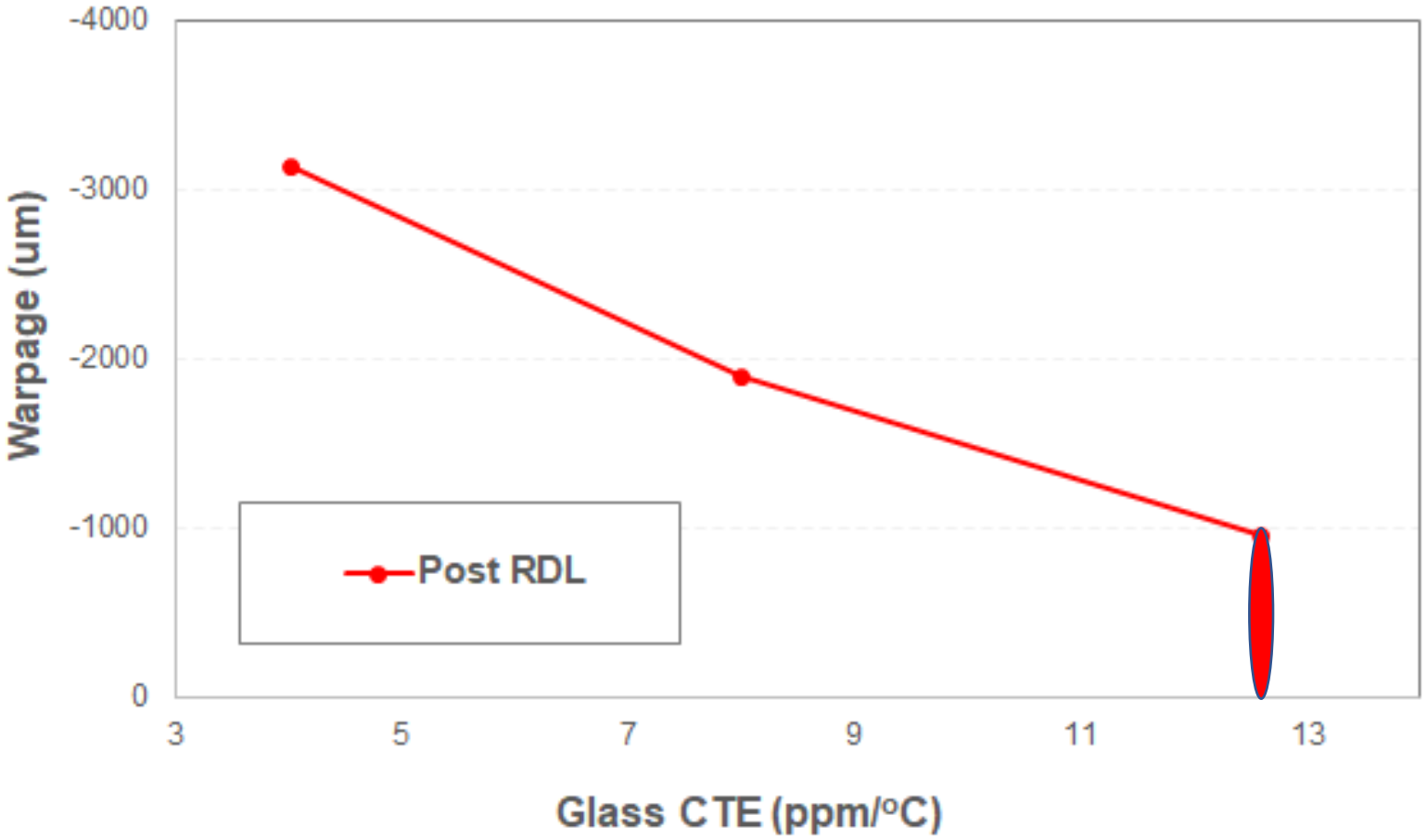
MLO built on carrier

6-layer Cu/PI MLO →

	Glass	Dielectric	Copper
Young's modulus (GPa)	80.0	8.5	117
CTE (ppm/K)	4.0/8.0/12.6	3.0	17.0
Poisson's ratio	0.22	0.30	0.34
Density (g/cc)	2.4	1.4	9.0

Source: HD MicroSystems PI-2600 product bulletin

Simulation case 2: multilayer organic (MLO)



- Bow is smiley face because Cu has high CTE and high Young's modulus
- Low CTE PI plays a minor role due to low Young's modulus
- CTE @12.6 ppm/C brings bow < 1mm

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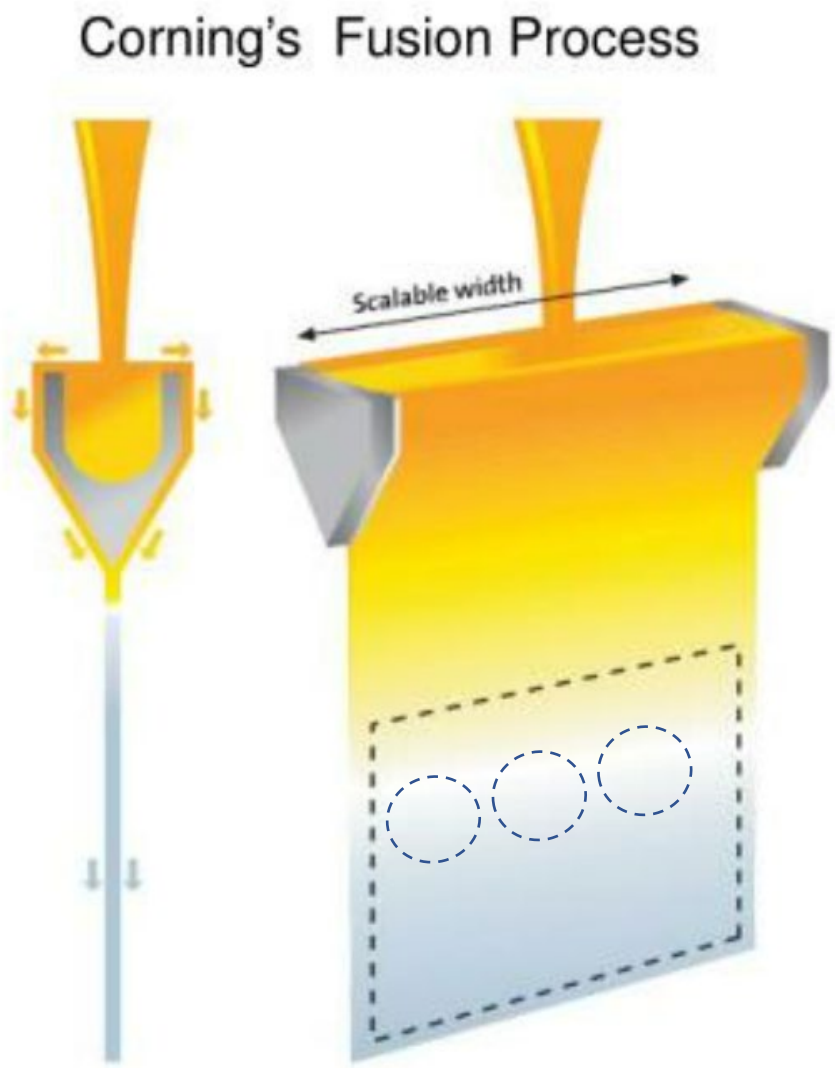
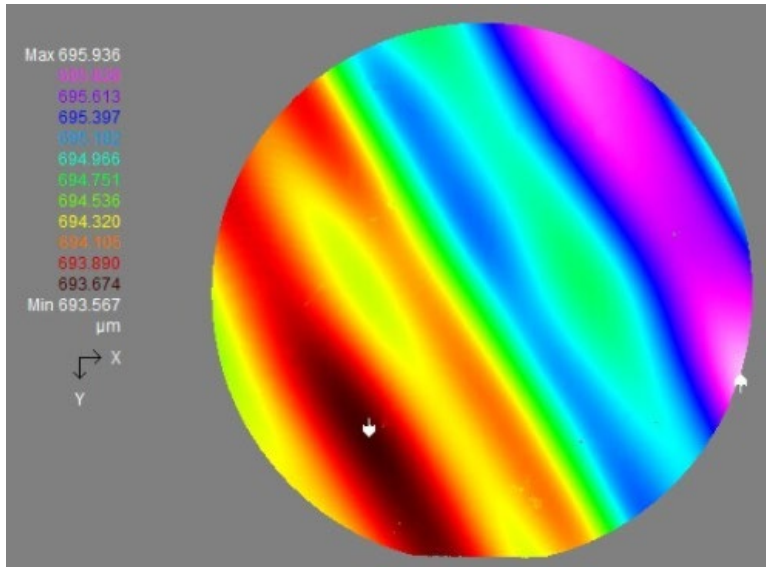
Fusion is a highly capable sheet forming technology

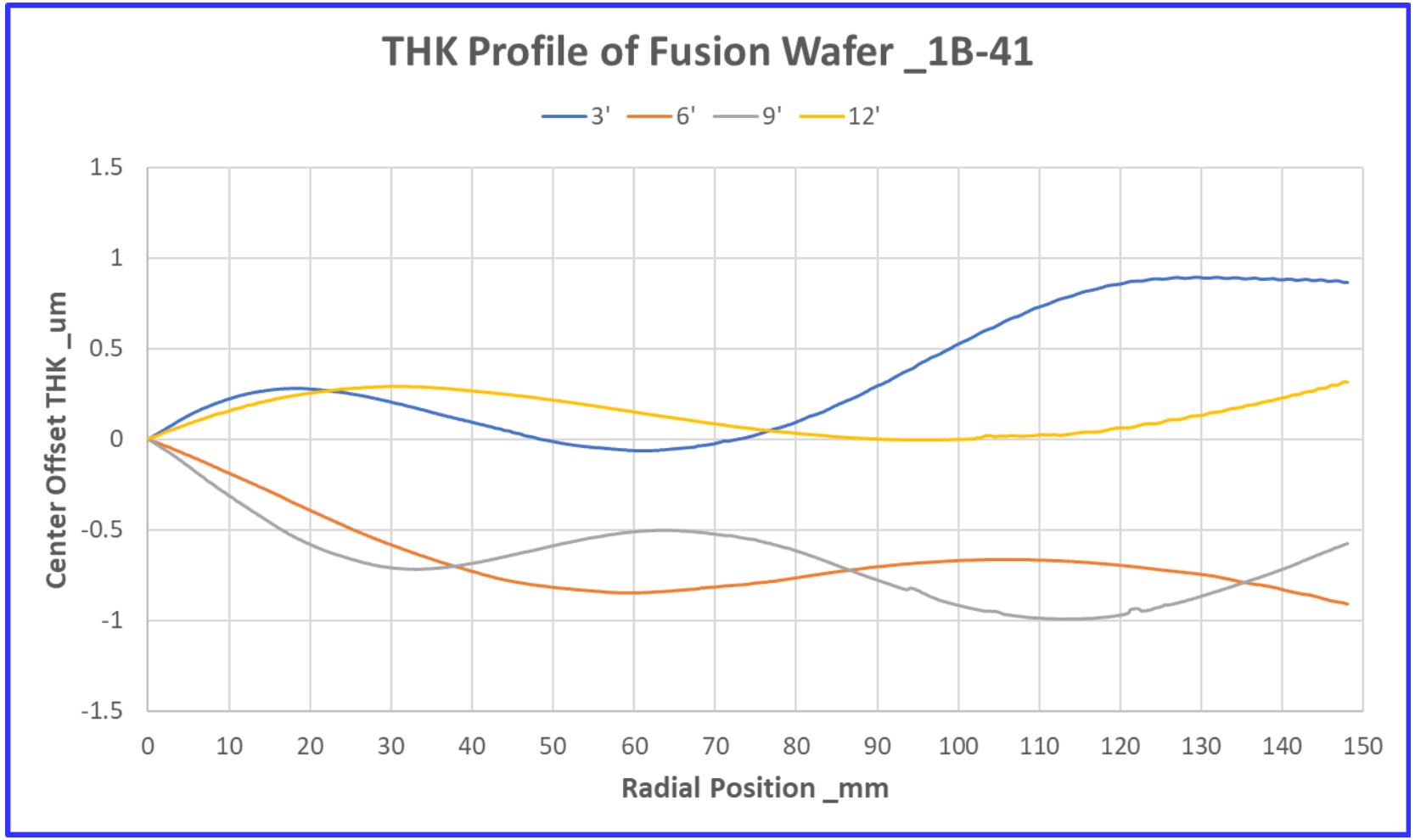


- Many different compositions
- Typical thickness 0.1-3.0mm
- Width as large as 3M
- Flat: low warp as-made
- Uniform thickness: low TTV

Fusion surface profile

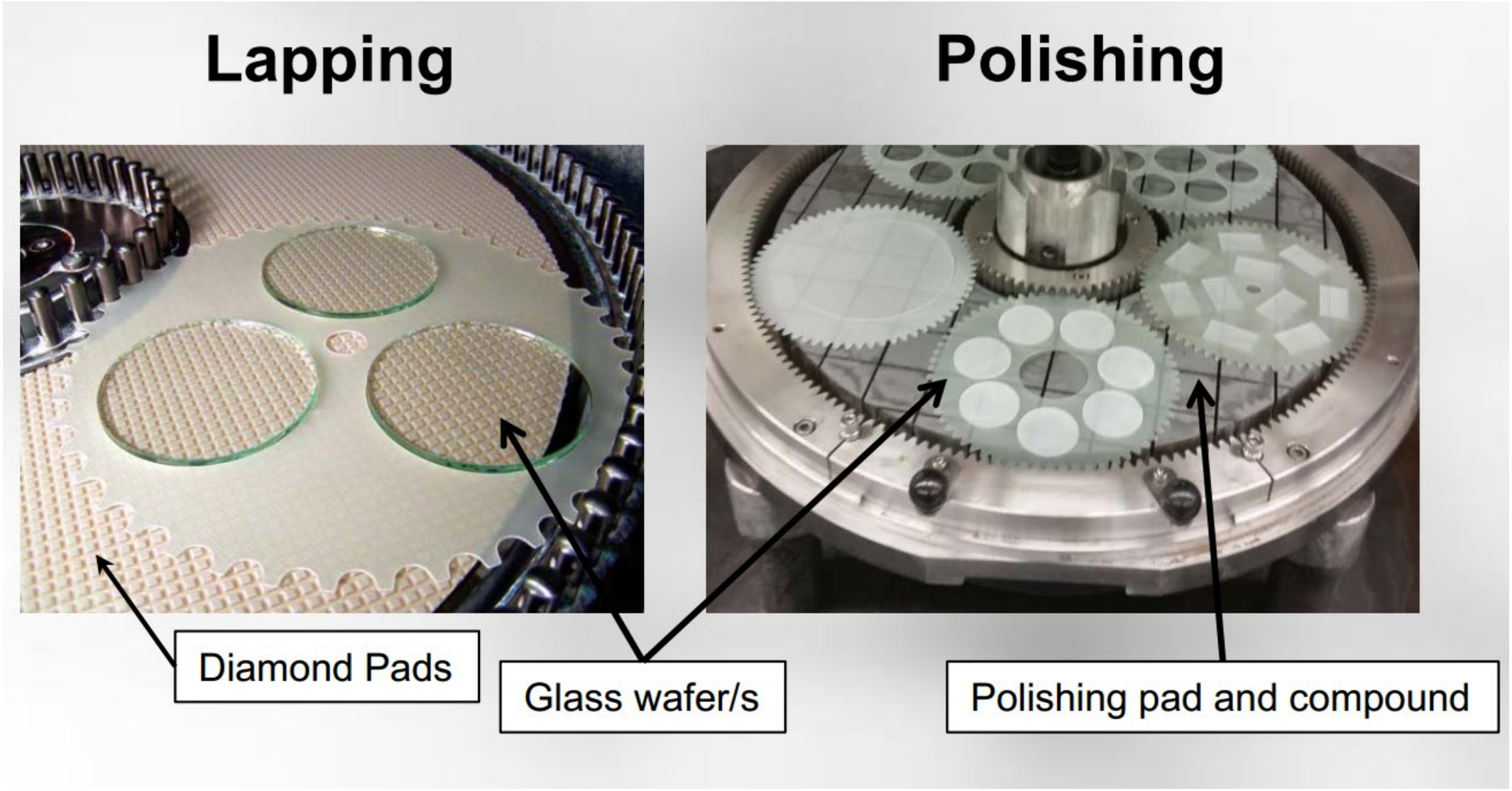
draw direction



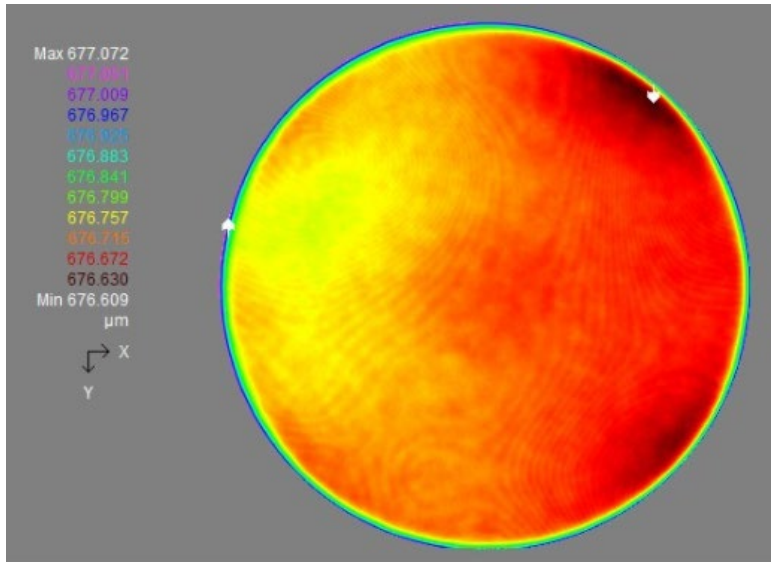


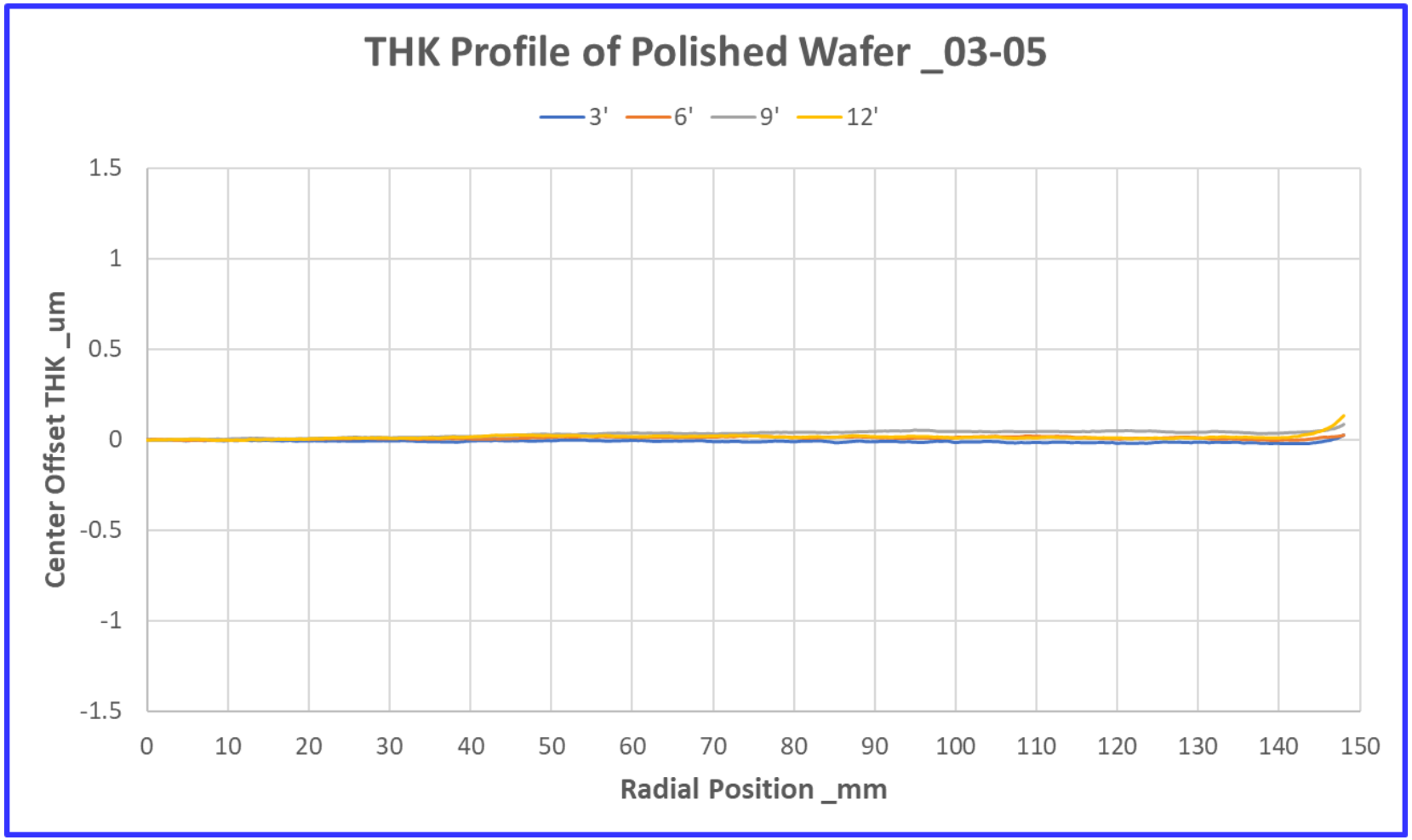
Data based on results of internal Corning studies

Glass finishing makes even flatter wafers



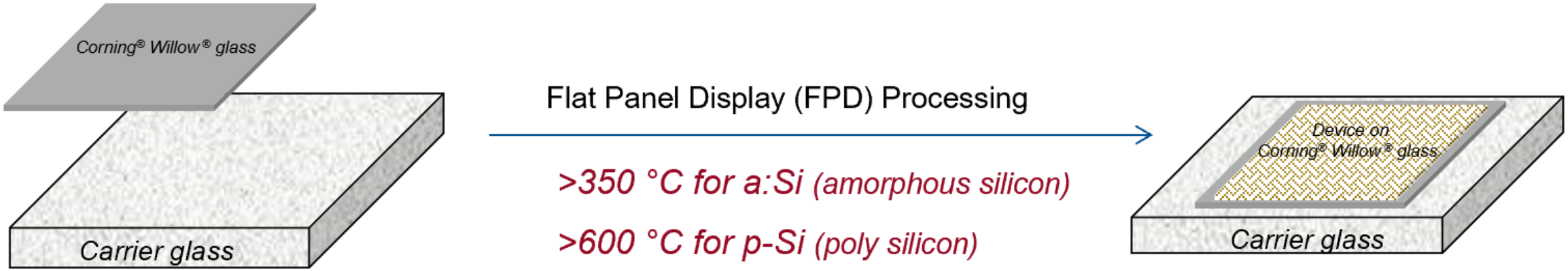
Polished surface profile





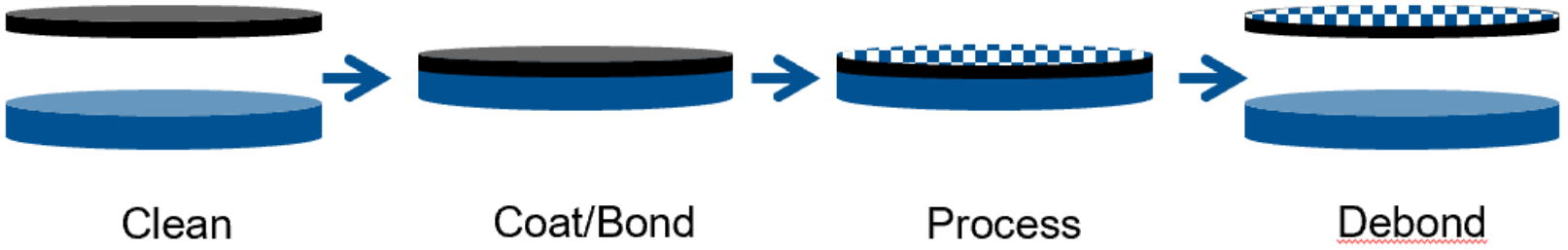
Data based on results of internal Corning studies

ALoT (Advanced Liftoff Technology) Introduction



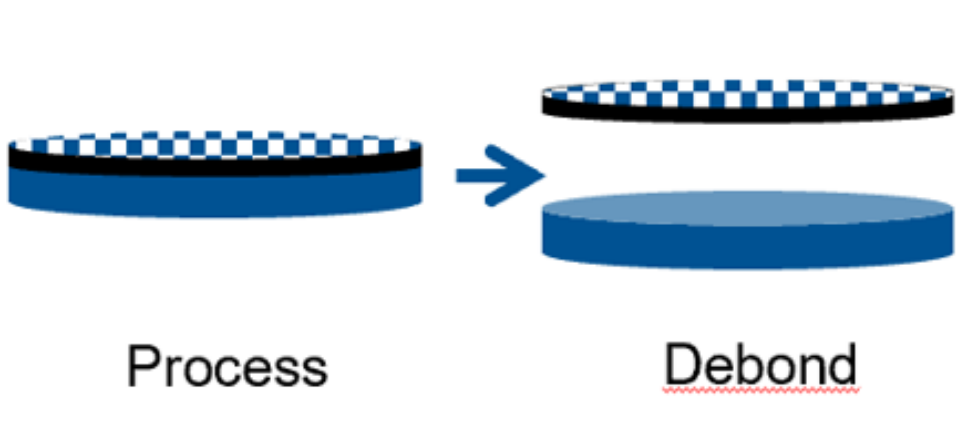
From display panels

To semiconductor wafers



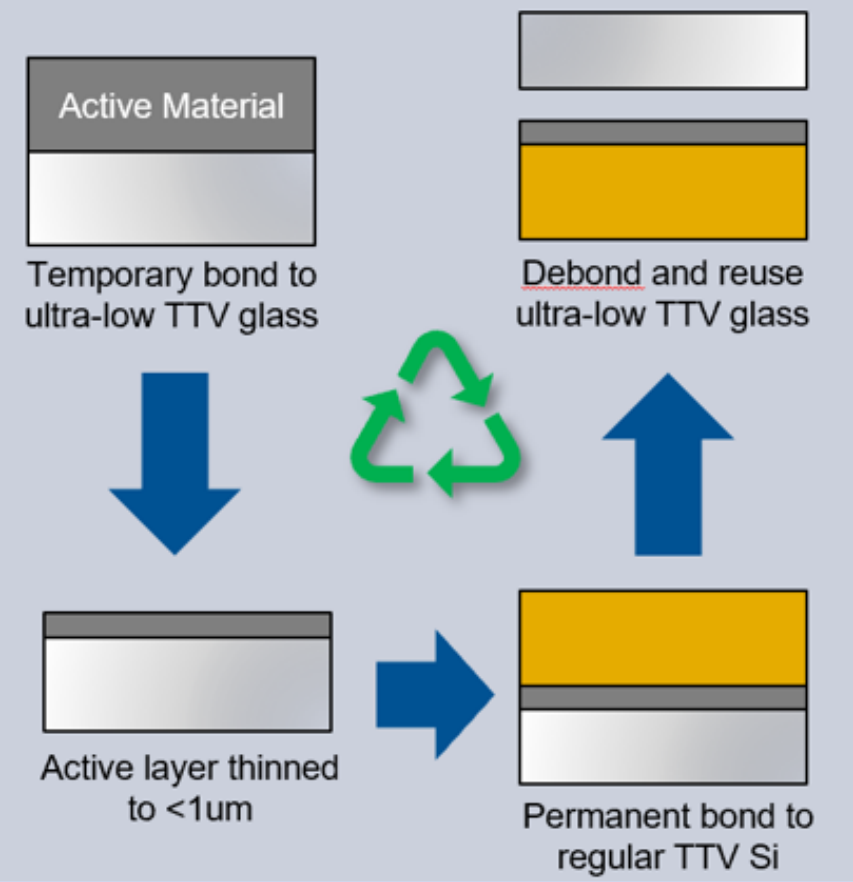
Key benefits: high temperature and near-zero-TTV

High Temperature



- Commercial adhesives < 350C
- Many semicon processes need >400C

Near-zero-TTV



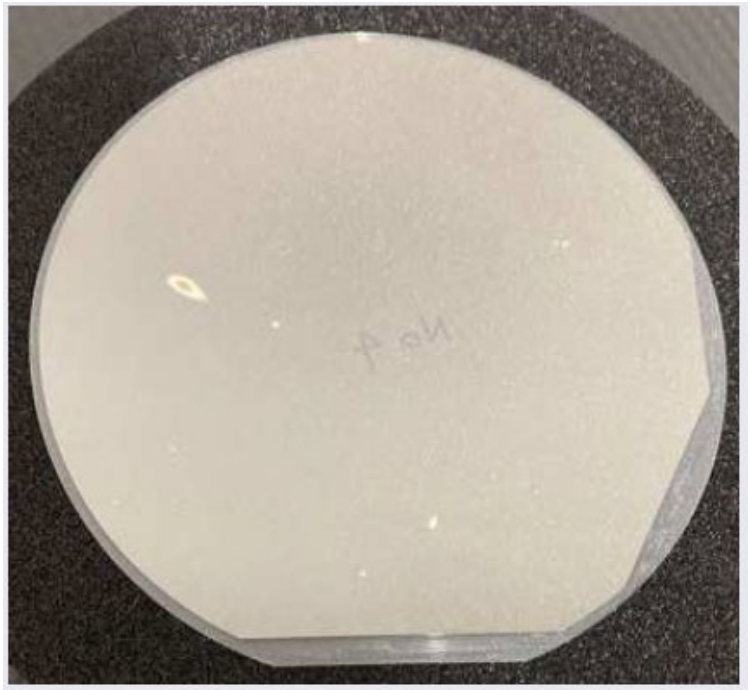
Near-zero TTV supports wafer grinding

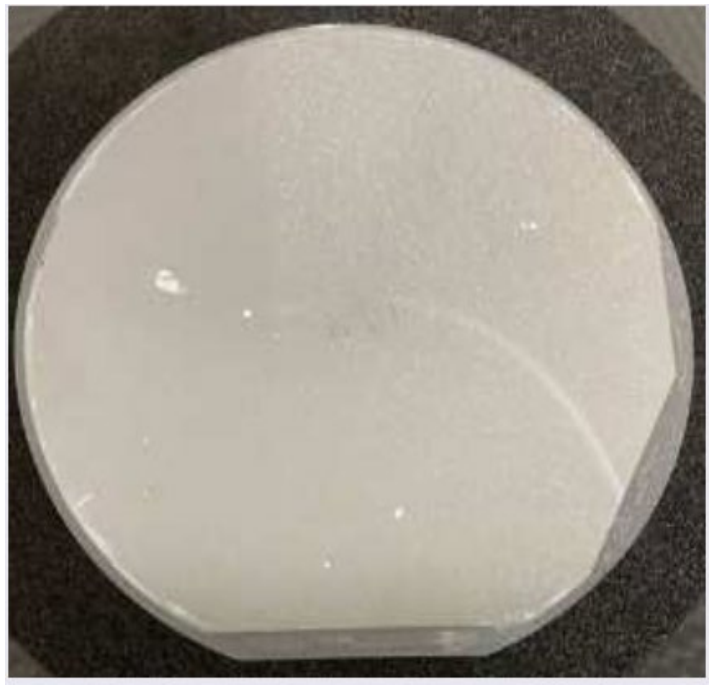
Thinning steps

Run time: 0 min	Run time: 2 min	Run time: 1 min	Run time: 1 min	Run time: 0.5 min
Removal: 0um	Removal: 200um	Removal: 100um	Removal: 100um	Removal: 50um
Si layer: 500um	Si layer: 300um	Si layer: 200um	Si layer: 100um	Si layer: 50um

Data based on results of internal Corning studies

Thinning down to 5um has been demonstrated





LT @350um

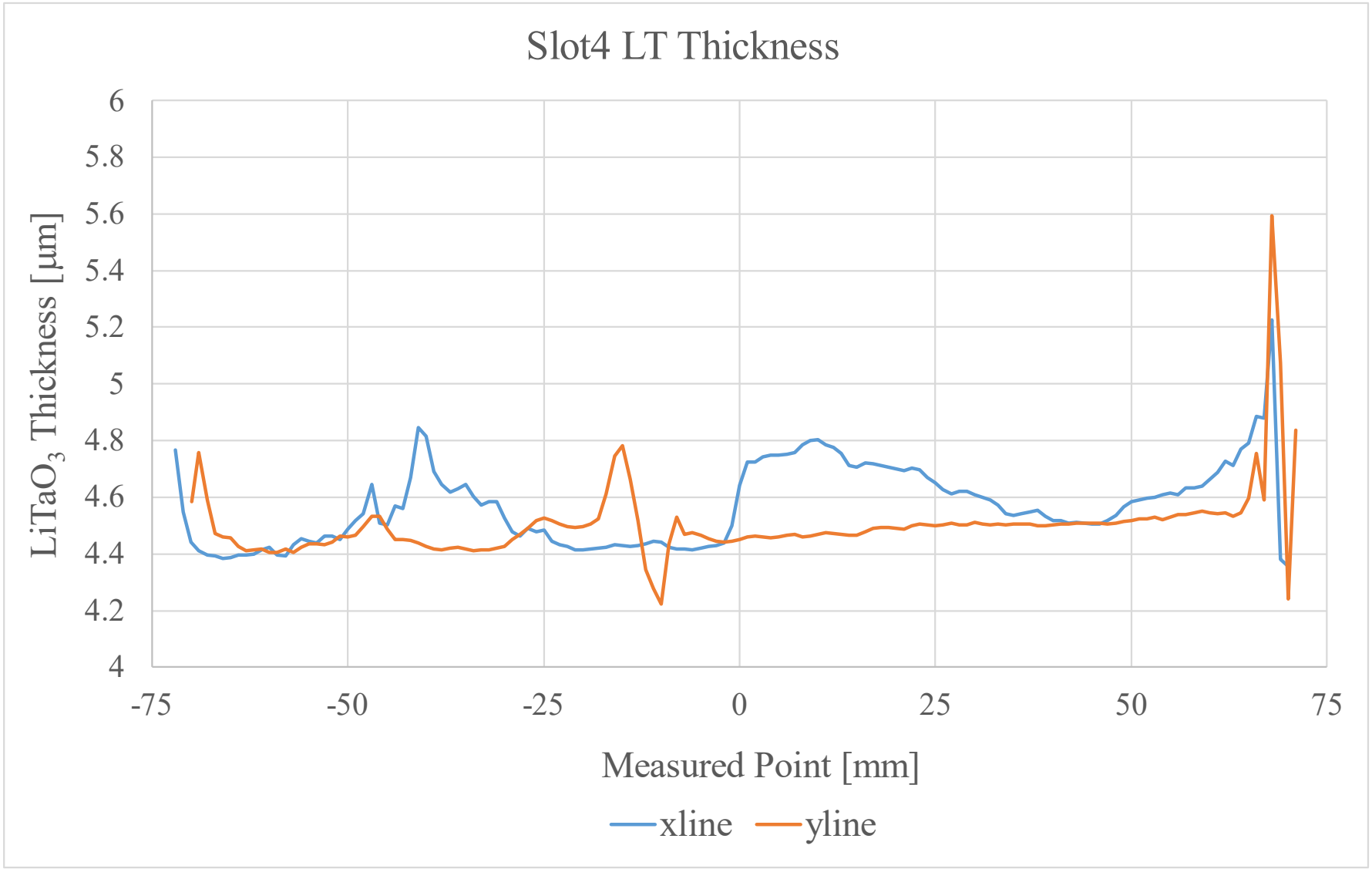
LT @15um

LT @<5um

Credit: DISCO

001280

TTV of thinned LT ~2X carrier TTV



Credit: DISCO

001281

Successful mechanical debonding at EVG

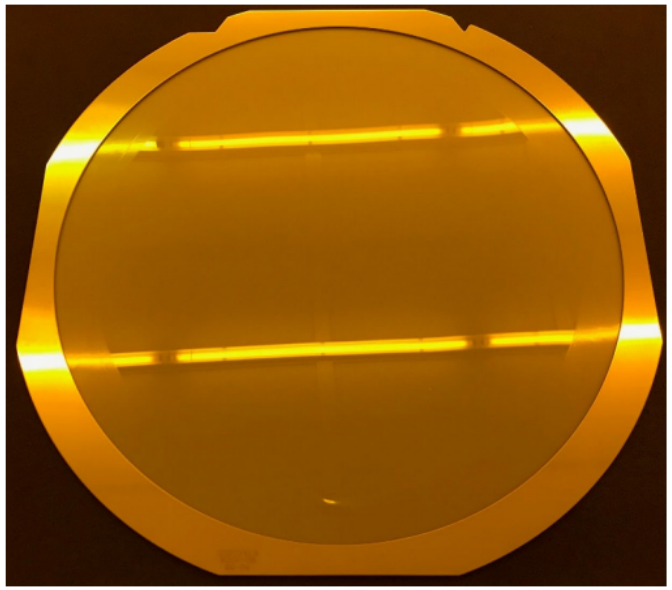
Substrate 1 Thickness	Substrate 2 Thickness
100 µm	700 µm

No separation could be succeeded without a blade initiation
→ Vacuum loss

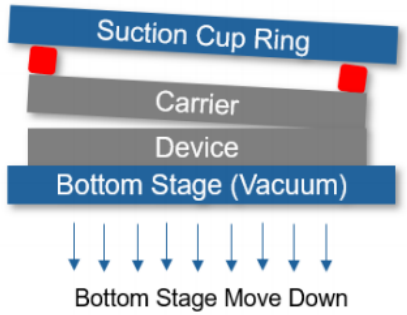
A proper initiation could be achieved with a stainless steel and a low abrasion plastic initator

The wafer stack could be successfully separated (carrier peel off) after initiation
→ Pull force (~10N)

300 mm thin wafer on FilmFrame
Post debond inspection



Method A



Credit: EVG

Conclusions

- Glass carrier wafers can effectively help control warp in many buildup processes through CTE engineering, Young's modulus enhancement, and thickness customization
- Corning's advanced packaging carrier (APC) product line now covers wide range of CTE with fine granularity, high Young's modulus and thickness flexibility to deliver on this promise
- Corning's ultra-low-TTV carrier and "near-zero-TTV" temporary bonding solutions (ALoT) deliver <<1um stack TTV, enabling extreme wafer thinning
- Corning welcomes applications inquiries and joint development opportunities with customers

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Dr. Han Xu: xuh20@corning.com

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- DISCO Corporation in Japan for wafer thinning down to 5um thickness as well as insightful discussions with Dr. Frank Wei of DISCO Hi-Tec America
- EVG in Austria for mechanical debonding