Low Loss/Low CTE Semiconductor Carrier Packaging Thin Core Material

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AGC Multi-Material America

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19TH INTERNATIONAL CONFERENCE & EXHIBITION ON

DEVICE PACKAGING

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AGC Overview

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Company name	AGC Inc.
Established	September 8, 1907
Representative director	Yoshinori Hirai
Paid-in capital	¥90.9 billion*
Consolidated net sales	¥1,412.3 billion*
Consolidated no. of employees	55,999*
No. of consolidated subsidiaries	206 companies

AGC Group

Glass (50%)

Flat Glass

-Float flat glass
-Figured glass
-Polished wired glass
-Low-E glass
-Decorative glass
-Fabricated glass for architectural use
（Heat Insulating/shielding glass, Disaster-resistant/Security glass, Fire-resistant glass, etc.）

Automotive Glass

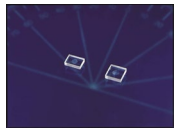
-Tempered glass
-Laminated glass

Electronics (18%)

Display

-LCD glass substrates
-Specialty glass for display applications
-Cover glass for car-mounted displays
-Display related materials
-Glass for solar power system
-Fabricated glass for industrial use

Electronic Materials



-Semiconductor process materials
-Optoelectronics materials
-Lighting glass products
-Laboratory glass, etc.

- PCB Materials

-High-speed Digital
-RF

Chemicals (30%)

Fluor chemicals & specialty chemicals

-Fluorinated resins
-Water and oil repellents
-Gases
-Solvents
-Pharmaceutical and agrochemical intermediates and active ingredients
-Iodine-related products

Chlor-alkali & urethane

-Vinyl chloride
-Vinyl chloride monomer
-Caustic soda
-Urethane

Ceramics/Other (2%)

-Ceramic products
-Logistics and financial services, etc.

AGC PCB Materials

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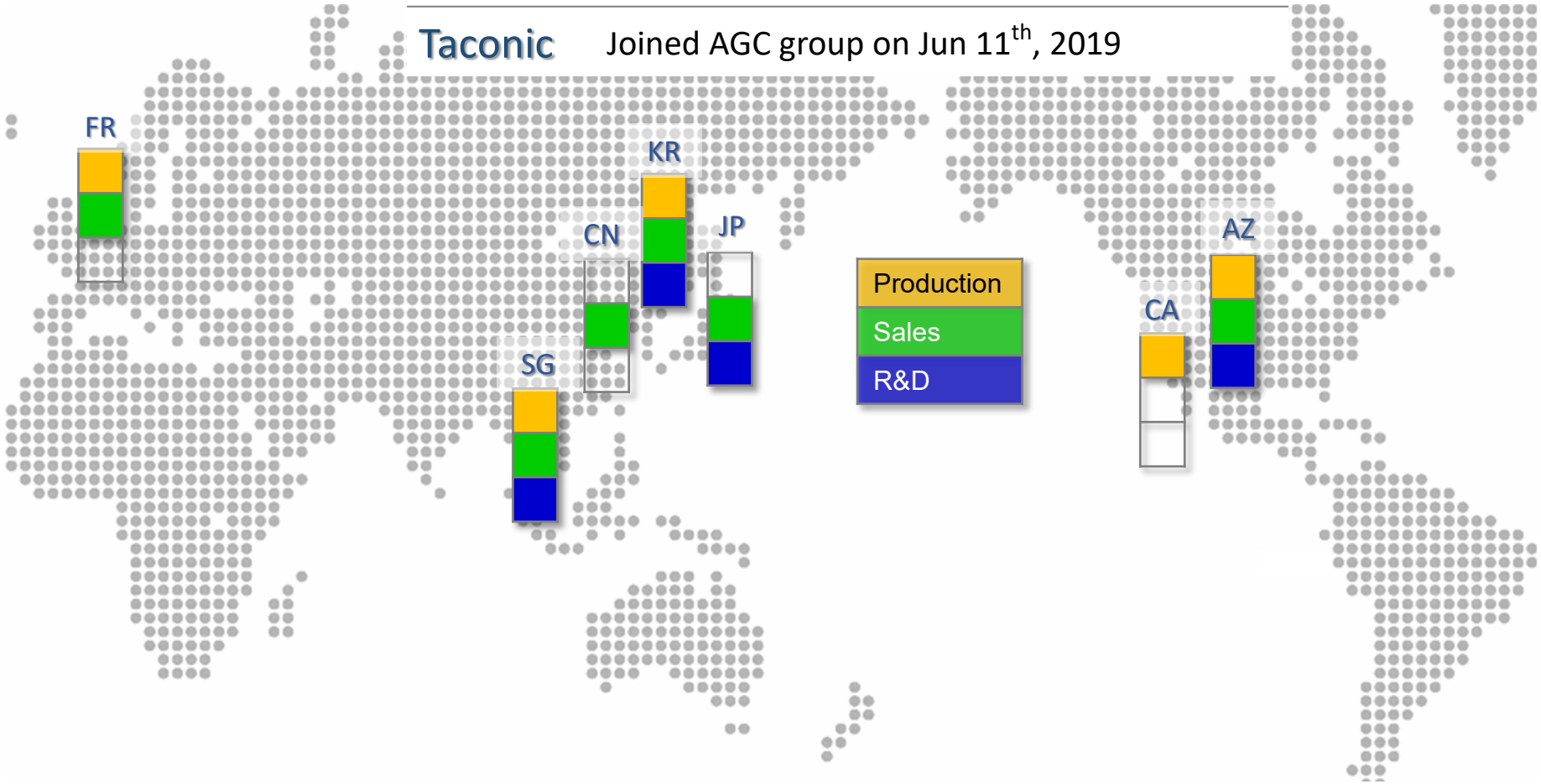
Nelco Joined AGC group on Dec 4th, 2018

Taconic Joined AGC group on Jun 11th, 2019



Introduction (Personal)

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- ✓ B.S. – Chemistry, Shippensburg University
  - Graduated 2019
- ✓ 2+ years at AGC Nelco, now AGC Multi-Material America.
- ✓ Research Chemist with focus on build-up film materials, technology and their application.

SHIPPENSBURG UNIVERSITY

Introduction and Goal of Material

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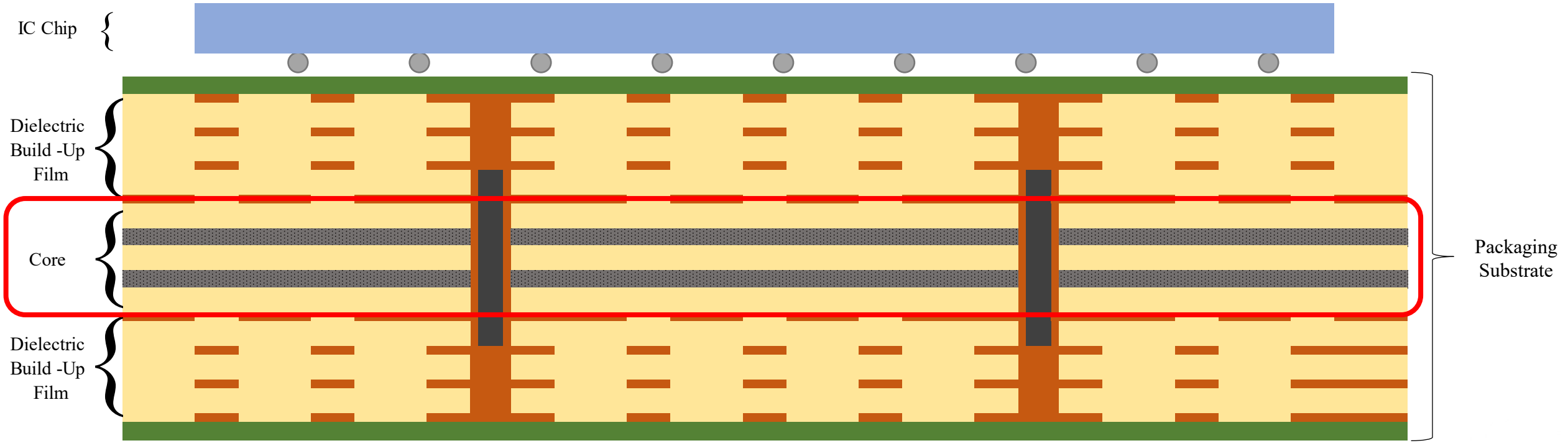
Need low loss, low CTE chip carrier substrate core material suitable for HDI applications that create robust, reliable and efficient boards.



Existing Strategy

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Traditional dielectric reinforced prepreg manufacturing techniques that have been in process for years have some drawbacks:

- Very difficult to impregnate fiber glass weave with high filler contents.
- Struggles to control resin contents and thickness.
- Prone to cracking issues in cured laminates; polyimides for example.

Existing Strategy

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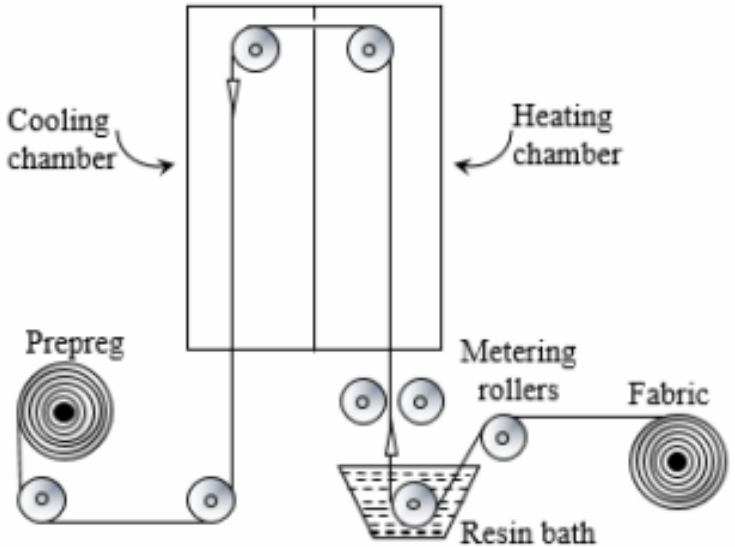
Raw Materials → Resin Varnish → Raw Fiber Glass → Prepreg → Foil Clad Laminates



Credit: Dimeski and Srebenkoska, OTEH 2014

Existing Strategy

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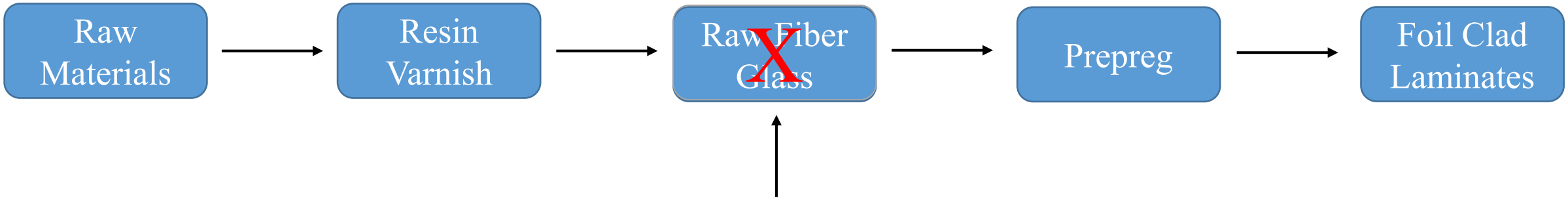

- Has potential to impregnate fiber glass weave with high filler content resin.
- Can easily control thickness based on press parameters.

Existing Strategy

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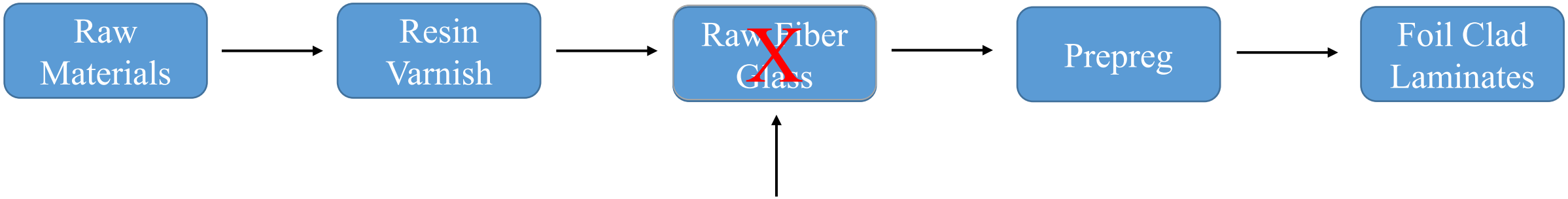

Coat resin varnish directly on release substrate

Our Strategy

TACONIC

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- Incorporate existing AGC-Taconic fastRise™ Build-Up films that have high filler content with fiberglass weave.

A. Laminate Form
B. Prepreg Form

- A combination of high heat and/or pressure can force resin into glass bundle fibers creating a coherent and consistent “prepreg-like” material.

Strategy A- Laminate Form

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High Pressure and Temperature

↓

Copper Foil
Resin Build-Up Film
Raw Fiberglass Weave
Resin Build-Up Film
Raw Fiberglass Weave
Resin Build-Up Film
Raw Fiberglass Weave
Resin Build-Up Film
Copper Foil

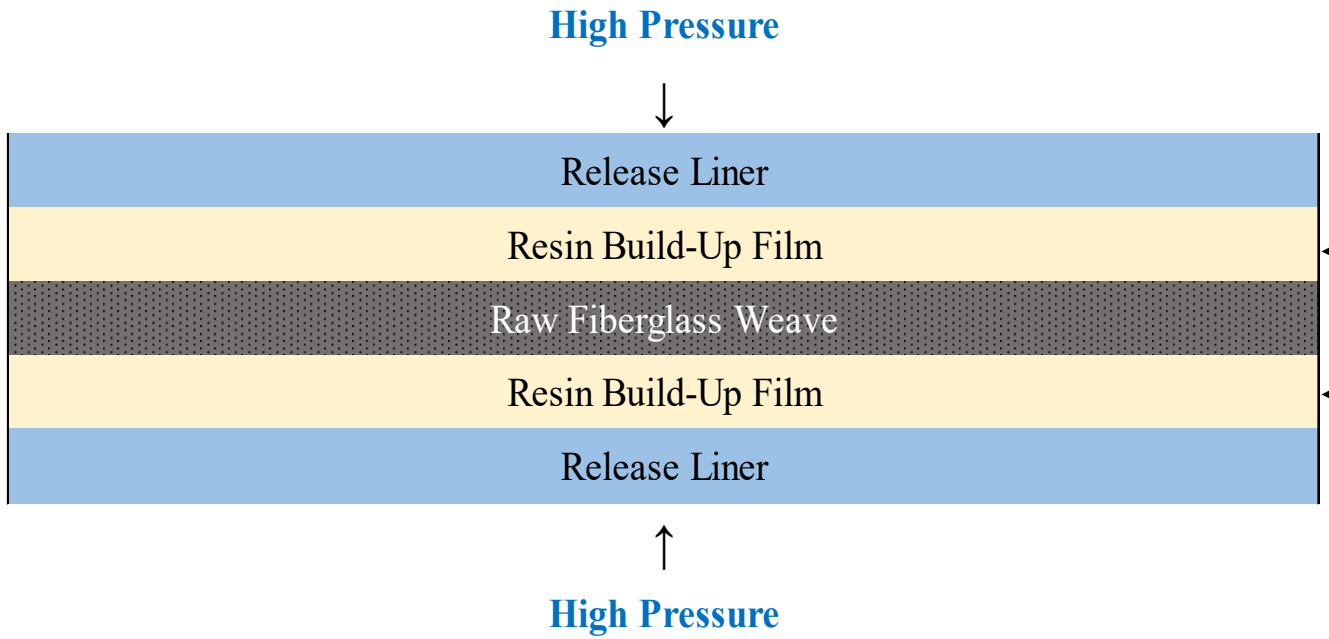
↑

High Pressure and Temperature

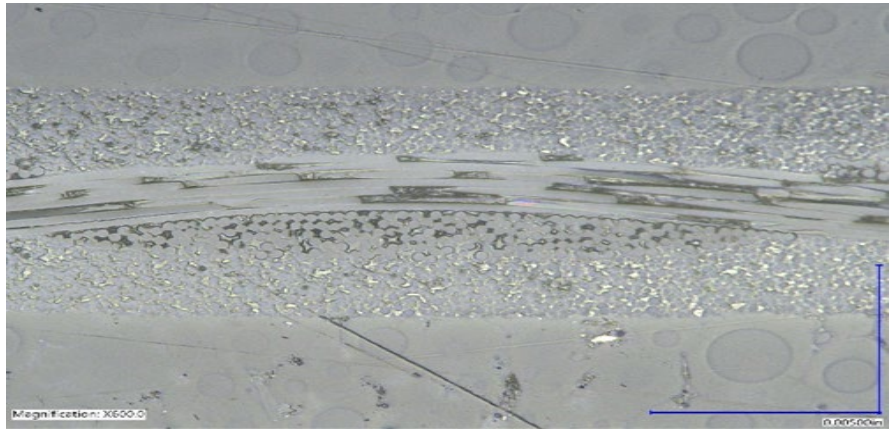
Able to be directly used as substrate core.

Can manipulate glass style and finish enough to dial in desired CTE values!

Strategy B – Prepreg Form



Thickness can very easily be controlled by amount of BUF pressed on either side of glass weave.



Goal is to have low degree of “cure” so prepreg is still in state of flow and fill.

Desired and Expected Properties

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Properties	Unit	Value
Df	N/A	<0.002
Dk	N/A	3.0 - 4.0
X/Y-CTE (40-260 °C)	PPM/°C	5 - 10
TMA Glass Transition (Tg)	°C	>260
Copper Peel Strength	lb/in	>2.5
Thermal Conductivity	W/M*K	0.94

← Low Loss

← Ultra Reliability

How is ultra reliability achieved?

↓

Matching and consistent CTE values

X/Y-Axis Coefficient of Thermal Expansion

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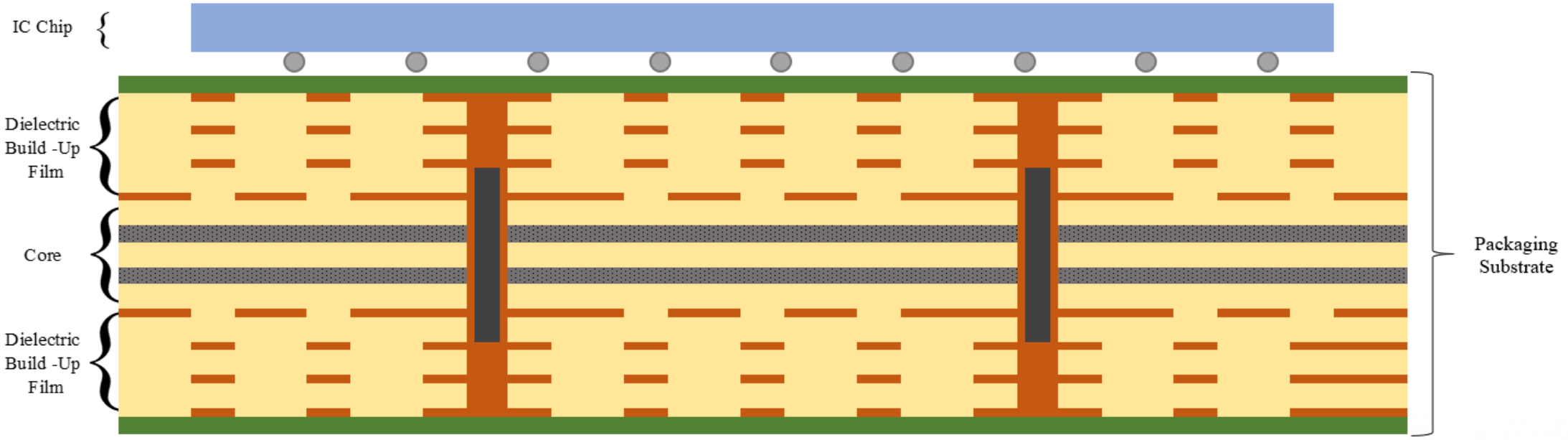
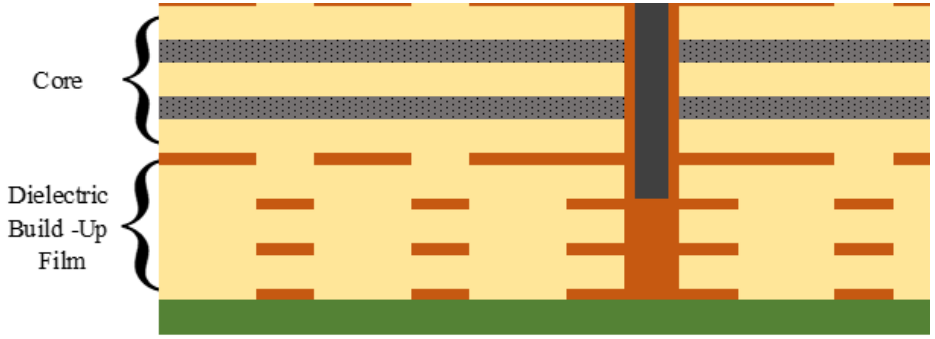


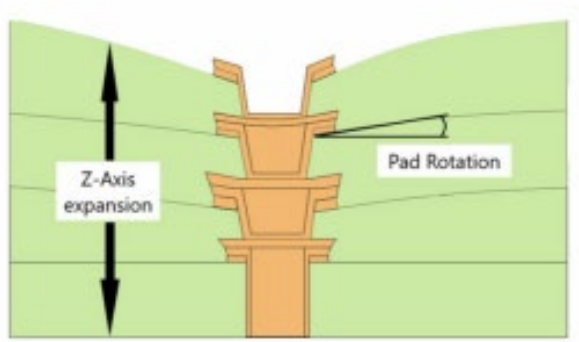
Substrate Core X/Y-CTE Target = 5-10 PPM/ °C

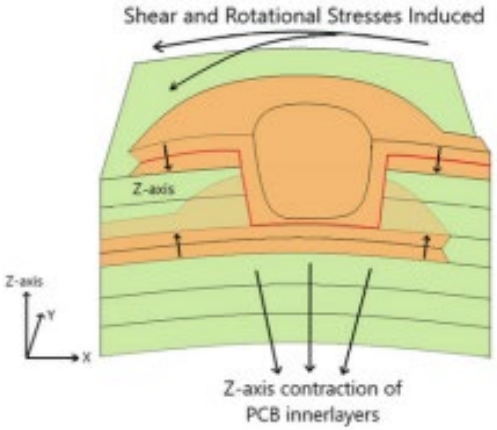
*Overall 40C – 260C

Low CTE: **IC Chip < Substrate Core < Solder Connection**: Higher CTE

Z-Axis Coefficient of Thermal Expansion



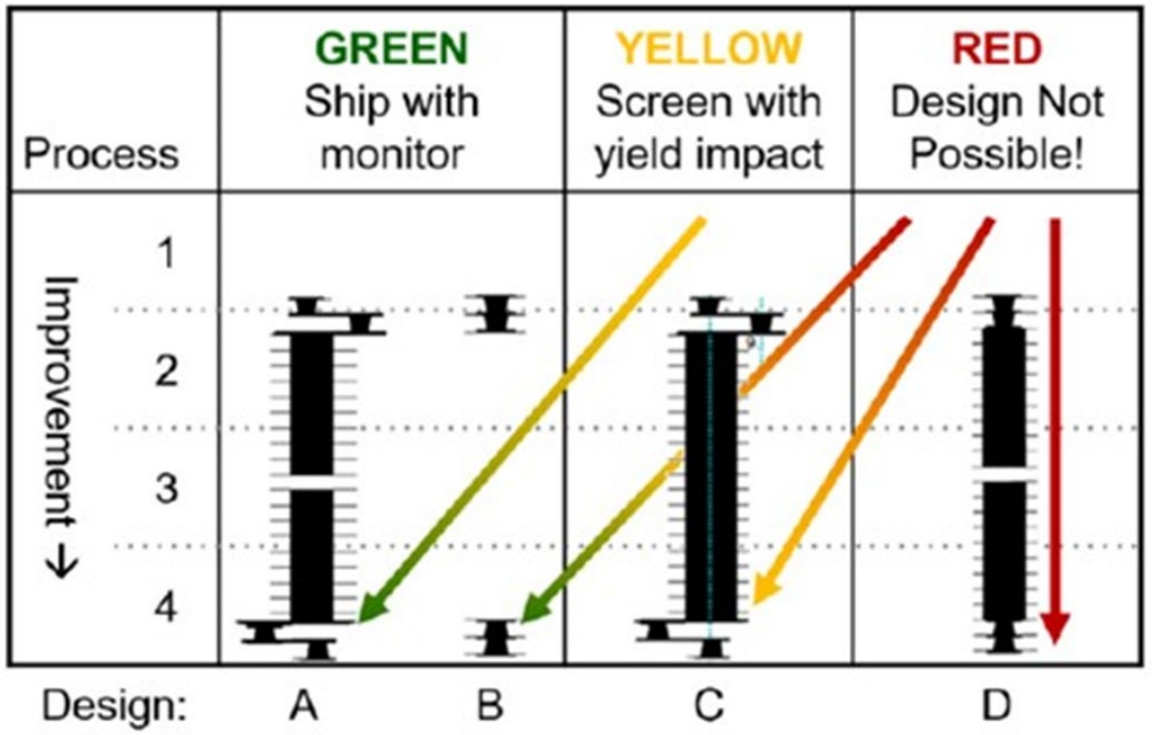




Microvia structure reliability is achieved with a dielectric build-up film that has a closely matched CTE to copper.

Copper = 17 ppm/C
Build-Up Film ~ 20 ppm/C
*Overall 40C – 260C

CTE Study with Stacked Microvias (Subassembly Design)



Design, material selection and fabrication quality matter!

- Bad design can shift green to red.
- High quality material can shift red to green.
- Bad fabrication quality can shift green to red.

Kevin Knadle, "The Keys to 100% Effective Reliability Testing and Failure Analysis of HDI/Microvias", IPC APEX EXPO™ 2020.

CTE Study with Stacked Microvias

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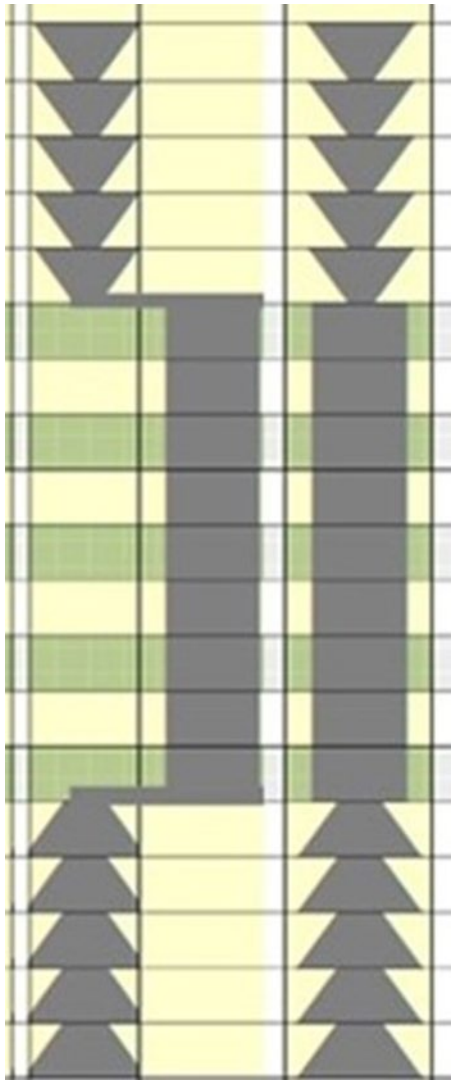
Study conducted of dielectric build-up material:

A. D-coupon
B. Current Induced Thermal Cycle (CITC)

Both tests reach a solder reflow temperature of 260 °C!



Can be direct attach with no offset or staggered with ~10 mil offset.

→ Buried Subassembly (55-60 mils)

fastRise™ Build-Up Film

CTE Study with Stacked Microvias (Staggered)

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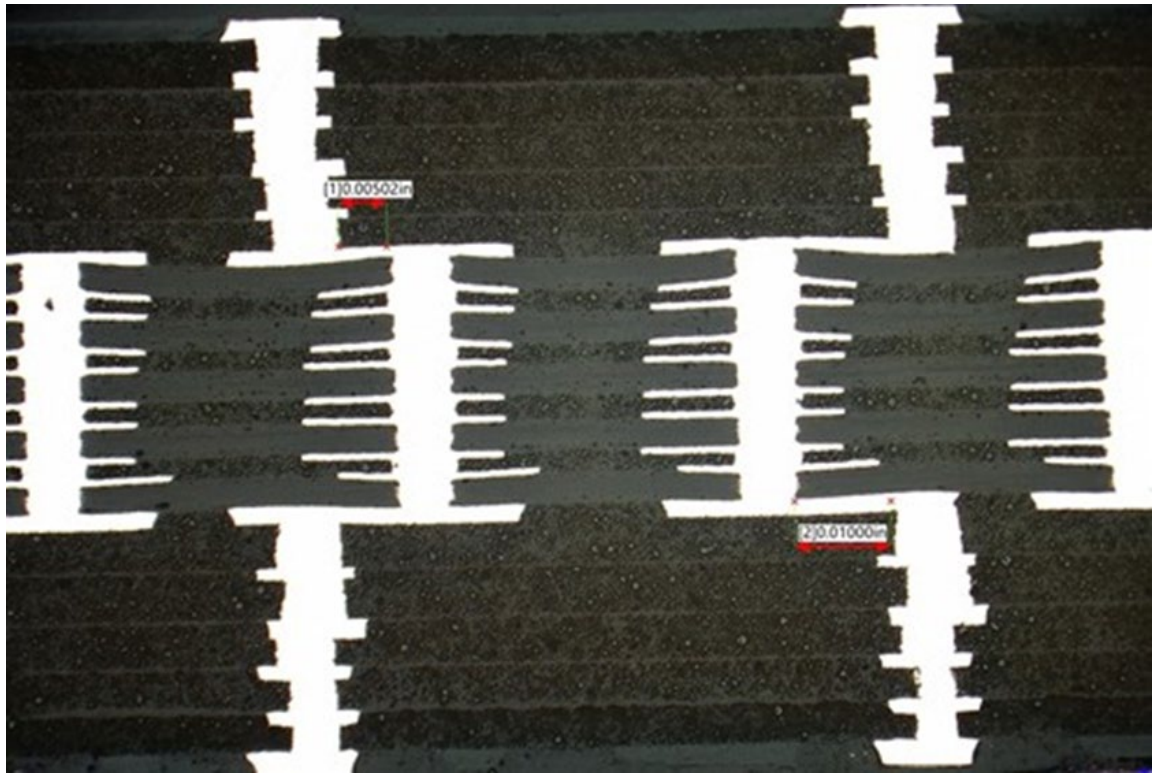

RLISerial	ReqNo	ReqGroup	Req	MeasuredValue	LTL	UTL	ConformityCalc
1	1	IPC-TM-650 2.6.27	Resistance Change	-0.006	-0.010	0.050	PASS
2	1	IPC-TM-650 2.6.27	Resistance Change	-0.001	-0.010	0.050	PASS
3	1	IPC-TM-650 2.6.27	Resistance Change	-0.007	-0.010	0.050	PASS
4	1	IPC-TM-650 2.6.27	Resistance Change	-0.006	-0.010	0.050	PASS
5	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
6	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
7	1	IPC-TM-650 2.6.27	Resistance Change	-0.004	-0.010	0.050	PASS
8	1	IPC-TM-650 2.6.27	Resistance Change	-0.006	-0.010	0.050	PASS
9	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
10	1	IPC-TM-650 2.6.27	Resistance Change	0.006	-0.010	0.050	PASS
11	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
12	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
13	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
14	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
15	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
16	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
17	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
18	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
19	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
20	1	IPC-TM-650 2.6.27	Resistance Change	-0.004	-0.010	0.050	PASS
21	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
22	1	IPC-TM-650 2.6.27	Resistance Change	-0.005	-0.010	0.050	PASS
23	1	IPC-TM-650 2.6.27	Resistance Change	-0.003	-0.010	0.050	PASS
24	1	IPC-TM-650 2.6.27	Resistance Change	-0.004	-0.010	0.050	PASS

PASSED 24 REFLOWS OF 35 °C – 260 °C.

CTE Study with Stacked Microvias (Direct Attach)

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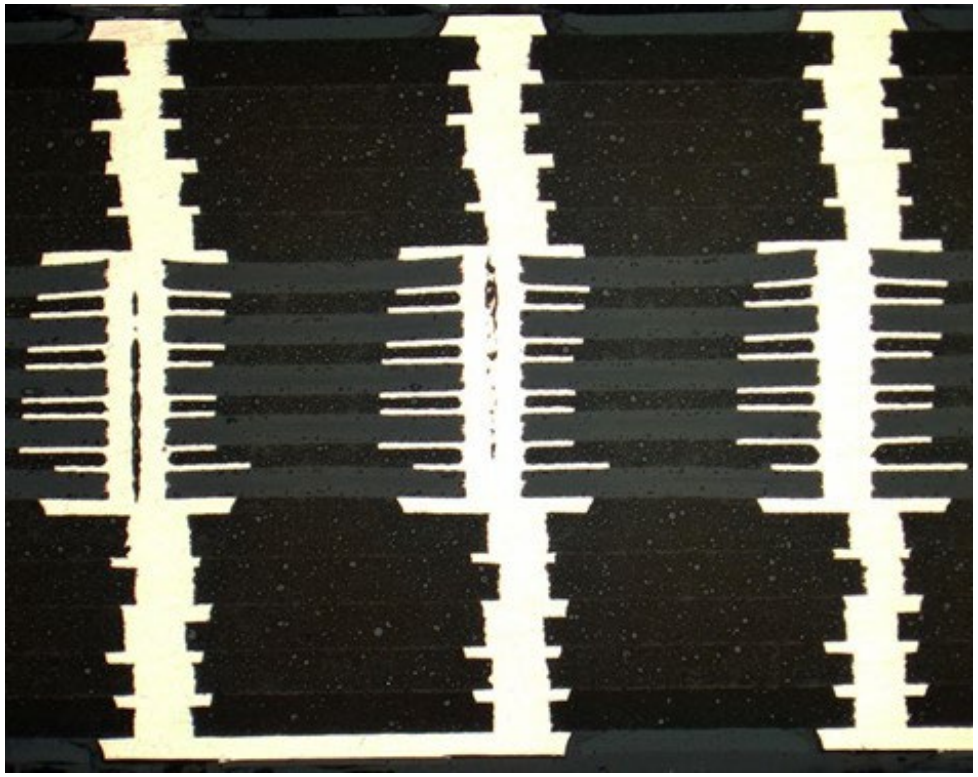

24 reflow cycles, 35 °C – 260 °C

↓

NO MICROVIA FAILURES

5 stack microvia structure successfully survived the following stress cycle:
24x @ 45 to 260C, 100x @ -55 to 155C, 24x @ 45 to 260C

Resin Flow and Fill

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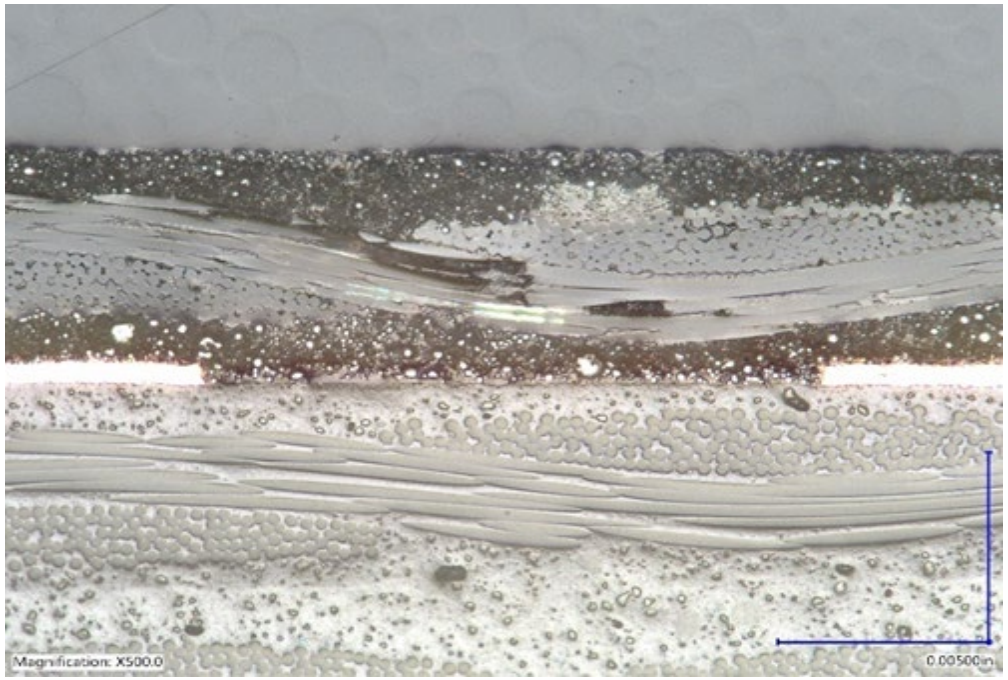
Flow needs to be high enough for material to act as a leveling agent to reduce thickness variations in a subassembly.



Advantage of prepreg approach because of flow and fill characteristics.

- Low material viscosity allows highly filled ceramic to penetrate fiber glass weave.

Material with high ceramic needs to completely fill line/space gapping and vias in assembly process.

Dielectric Constant and Dissipation Factor

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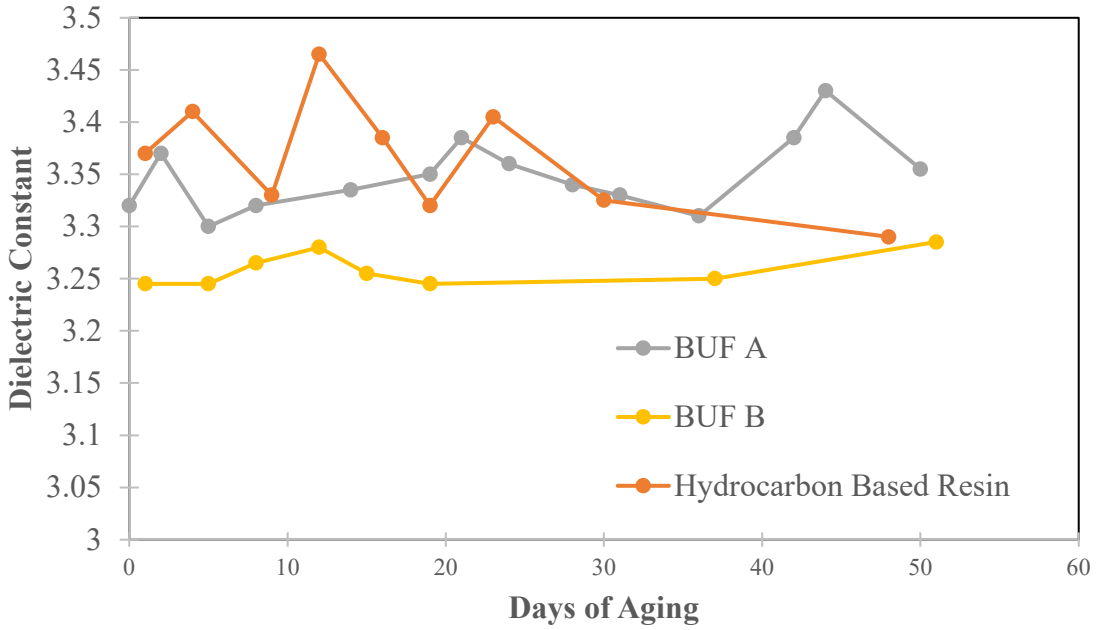
Dielectric Build-Up has extreme thermal aging resistance to Dielectric Constant.



	Dk @ Day 0	Dk @ Day 45+	Change
BUF A	3.32	3.355	0.035
BUF B	3.245	3.285	0.04
Hydrocarbon Based Resin	3.37	3.29	-0.08

Aged 45+ days @ 155 °C

Dielectric Constant and Dissipation Factor

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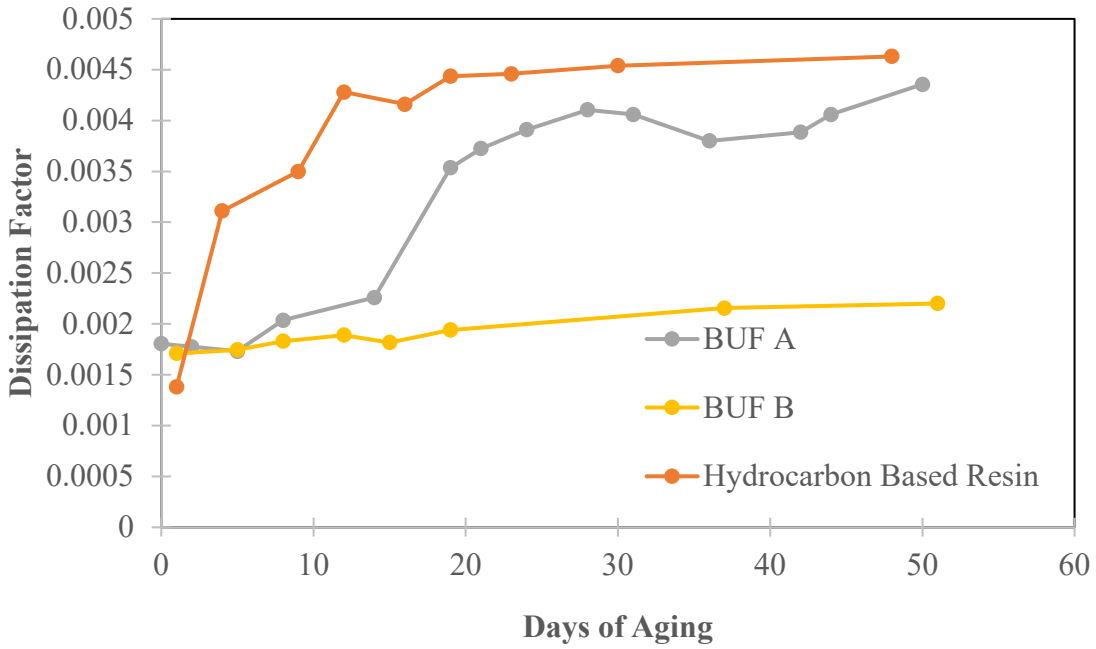
Dielectric Build-Up has extreme thermal aging resistance to Dissipation Factor.



Aged 45+ days @ 155 °C

	Df @ Day 0	Df @ Day 45+	Change
BUF A	0.001805	0.004355	0.00255
BUF B	0.00171	0.002201	0.000491
Hydrocarbon-Based Resin	0.00138	0.00463	0.00325

Low Df over time means transmission can remain low over time with aging!

Summary

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- Successfully provide a solution for a low loss, low CTE ultra reliable IC package substrate core material.
  - X/Y-CTE = 5-10 ppm/C and Df < 0.002 with heat resistant properties
- Two approaches include a prepreg and laminate for fabrication.
- Dielectric build-up film material was proven to survive multiple reflow simulations with staggered or stacked vias, directly attached to a subassembly with no offset.

Summary

- This method is not only suitable for high-volume manufacturing, but for high-mix, low-volume manufacturing for the US advanced chip packaging supply chain.

- AGC-Multi Material America is developing and manufacturing here in the “Silicon Desert” of Greater Phoenix, Arizona!

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Q & A

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Thank you

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