High Speed Copper Plating Process for IC Substrate

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Outline

- What is an IC substrate?
- Industry trends – miniaturization
- Technical challenges – typical feature sizes
- Plating tools and equipment
- Solution concentrations – plating parameters
- Experimental results
- Conclusion

What is an IC Substrate

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- IC substrate is the connecting point between integrated circuit chip and the printed circuit board.
- Image Key:
  - A : Processor die
  - B : 80-90µm bump pitch
  - E : Heat spreader
  - **F : IC substrate**
  - G : Embedded capacitor
  - I : Solder balls
  - K : Printed circuit board

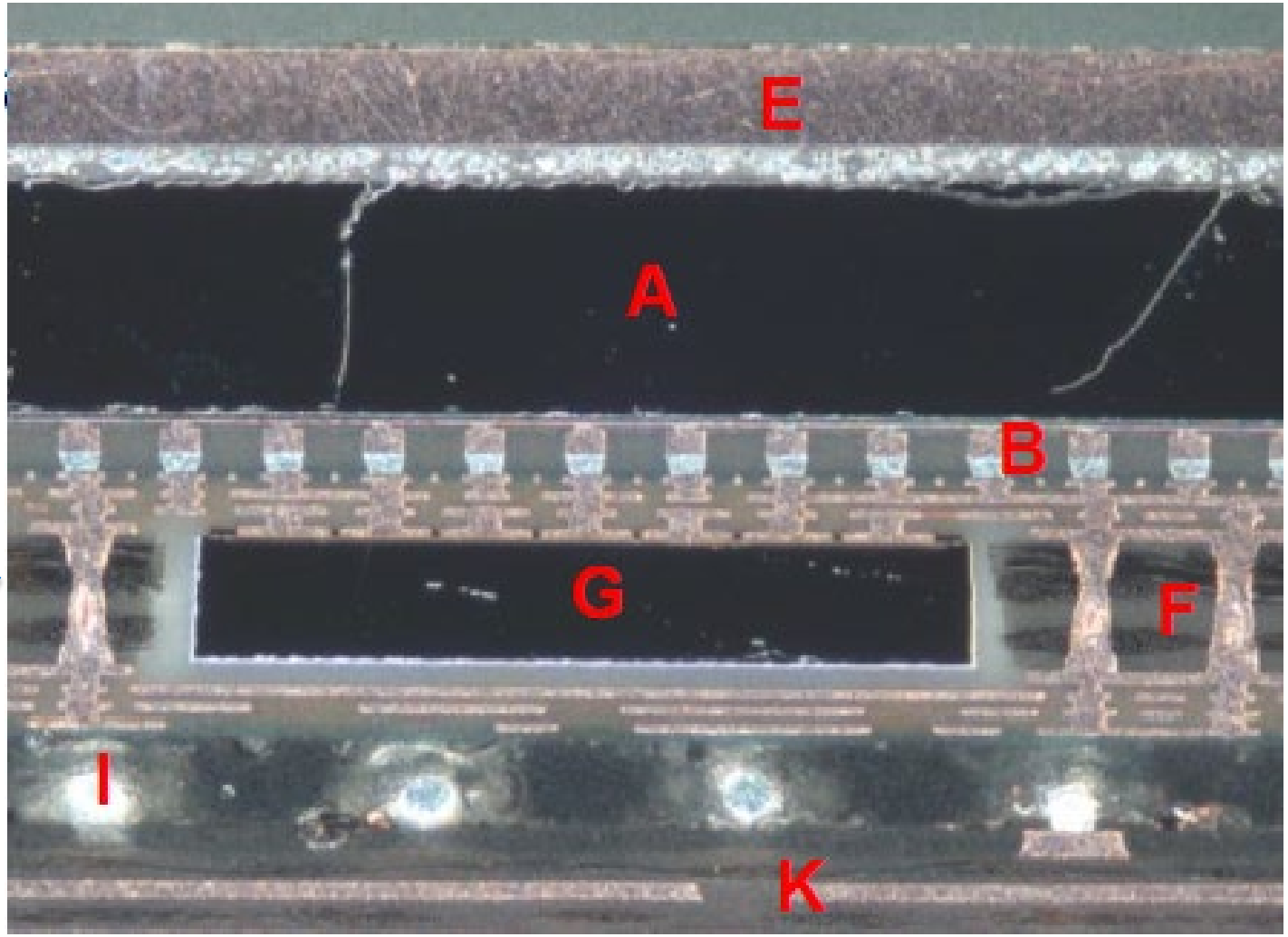
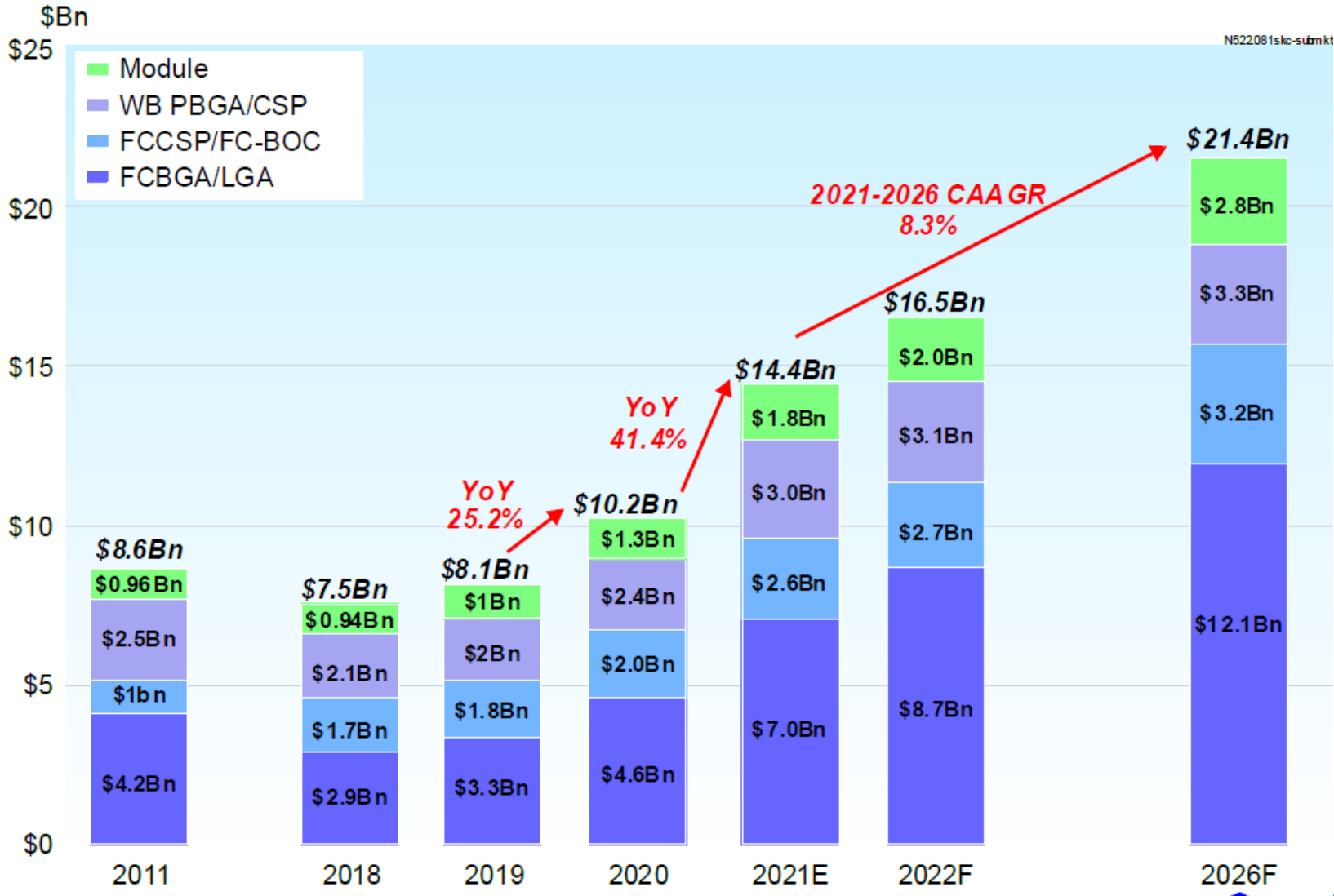


Image source: Prismark/Binghamton University

IC substrate market trend

- Substrate market has seen drastic growth since 2018.
- Market was $7.5 billion in 2018 to around $14.5 billion in 2021.
- Growth is expected to continue through 2026.



Technologies utilized

- There are multiple technologies utilized for constructing substrates.
- Each application has different requirements, but they all require uniform surfaces.

	Subtractive	mSAP	ETS/mSAP	SAP w/ABF
Substrate	Wirebond, BGA, CSP, SiP, FC BOC	Stacked CSP, FCCSP, SiP	FCCSP	FCBGA
Application	Memory, Logic, Module	Memory, Logic	AP, AP/BB	CPU, GPU, ASIC/FPGA, Logic
Surface Metal	Cu Foil	Cu Foil	Cu Foil	ABF/ Electroless Cu
Plating Type (Plating thickness, um)	Panel Plating (9-12)	Pattern Plating (2-12)	Pattern Plating (2-12)	Pattern Plating (5-15)
Dielectric	Prepreg	Prepreg	Prepreg	ABF Film
Adhesion requirement(Kg/cm)	0.4	0.4	0.4	0.4
Dielectric surface roughness Rz (um)	2.5-3.5	1.5-2		<1.5
Minimum L/S (um)	15-25	12-15	8-9	6-9
Comments	Cost sensitive	Lower profile Cu	Flat carrier	Rapid growth, looking for fine L/S

Typical IC substrate requirements

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- IC substrate requirements can be difficult to meet simultaneously. What helps one feature may hurt another.

Typical IC Substrate Requirements	
Typical via geometry (opening diameter x height)	40-65µm x 20-40µm
Via dimple/bump	< 2 µm
Via cavity volume	Void free
Surface Copper	12-18 µm
Examples of Substrate Package Sizes (mm)	24x27, 57x25, 57x36, 65x72…
Variation in surface Cu	Variable
Trace profile	Minimize
Within Panel Uniformity (WIP%)	< 5%
Plating speed	15-20 minutes

Why IC substrates are becoming more challenging

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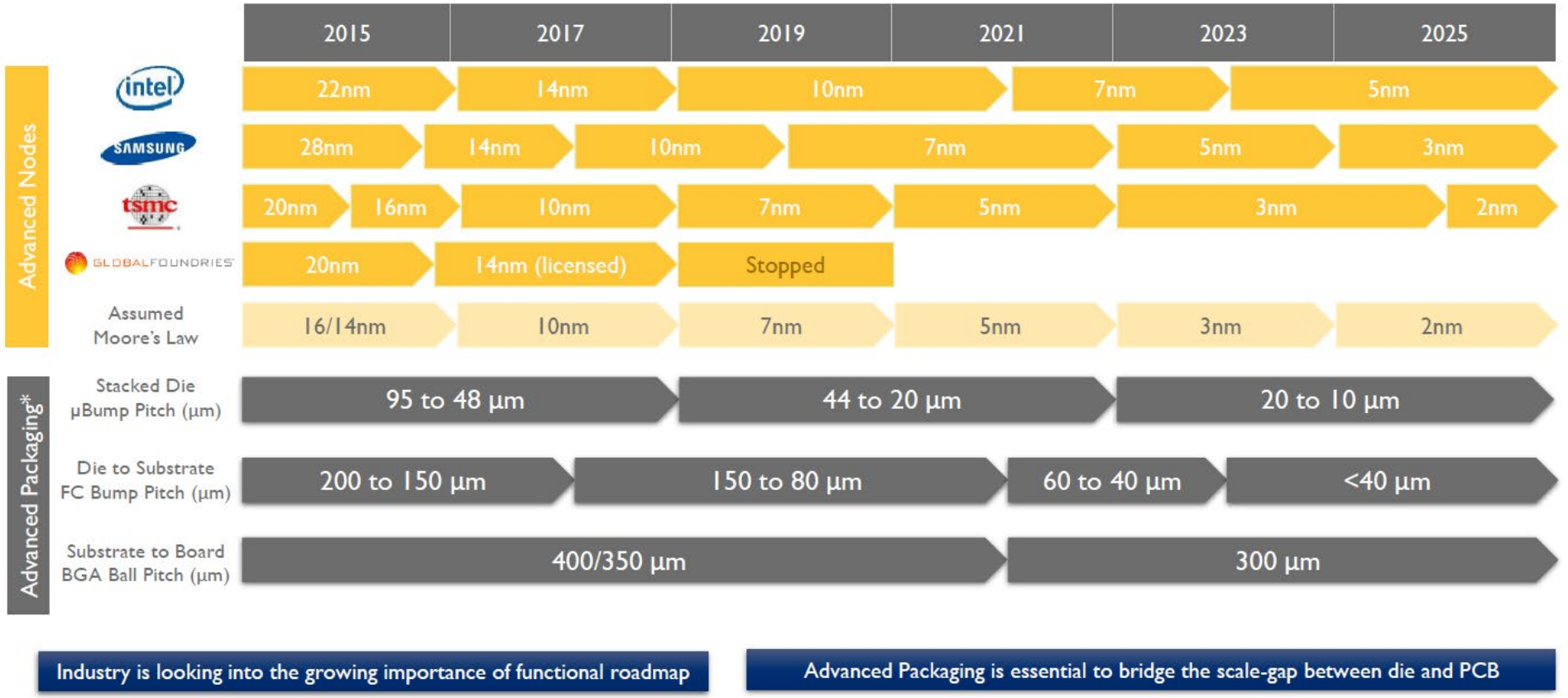
- IC substrates need continuous advancement to meet the complexity of dies
- Not only is the market growing, but the requirements are becoming more advanced. This includes progressing miniaturization and increased functionality.

TECHNOLOGY ROADMAP: FROM NANO-SCALE TO MICRO-SCALE..



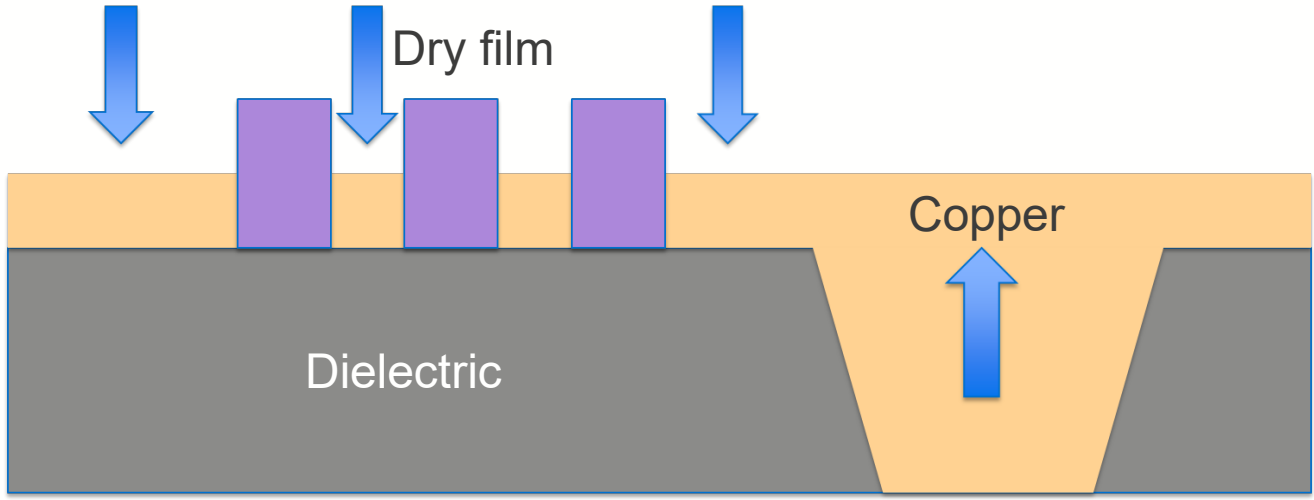
YOLE Développement

Average trends based on technology and industry expectation
*Minimum dimension

12

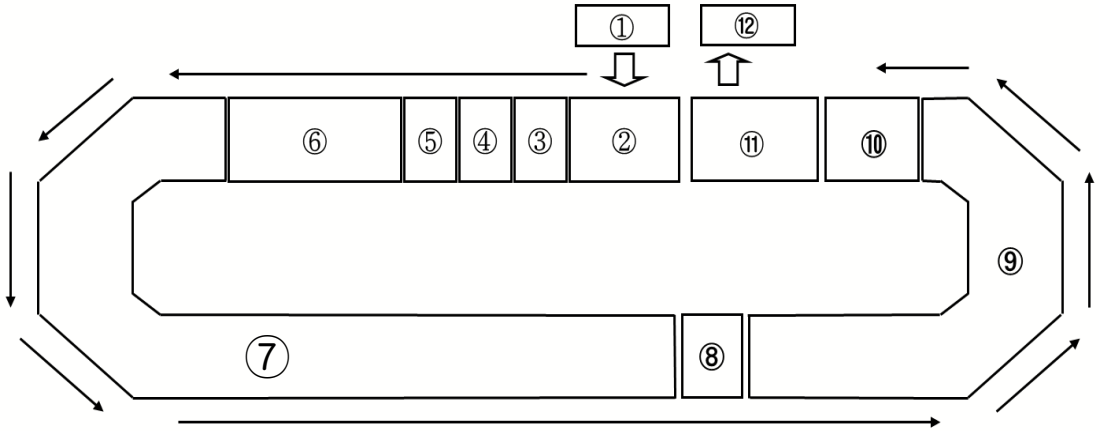
Technical challenges for 2 in 1 RDL features

- Drive for finer lines to increase feature density
  - Opportunity to reduce layer count & reduce cost
  - Possibility to reduce manufacturing steps.
- Technical challenges for acid copper plating process
  - Coplanarity on fine lines, pads and vias becomes more difficult as lines become smaller.
  - Feature profile – plated bump shape
  - Within Panel Uniformity (WIP%)
  - Plated copper physical properties – Reliability
  - Processability
    - Tool/chemistry interaction
    - Wide operation window
    - Compatibility to photoresist
- Factors that control ECD Cu
  - Organic additives strongly influence the characteristics of deposited copper.
  - Plating tool design, the type of anodes, VMS, plating CD, board design



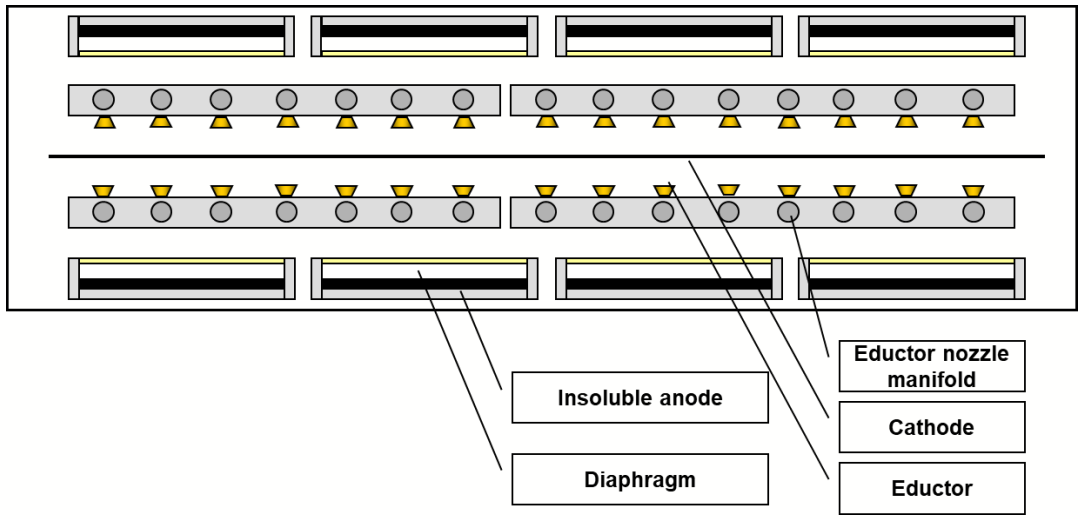
VCP configuration

- Typical vertical continuous plater (VCP) for high volume production
  - Panels progress through the tank, passing each anode and nozzle manifold, which provides consistent plating.
  - Typical plating conditions: CD = 1-3 ASD, bath temperature = 20-25 °C, plating time 50-60 minutes



① Load ② Acid Clean ③ Rinse ④ Rinse ⑤ Rinse
⑥ Acid dip ⑦ ETS Acid Copper Plating ⑧ DI Rinse
⑨ Antitarnish ⑩ DI Rinse ⑪ Dryer ⑫ Unload

Top view of VCP plating line



High speed panel processing tool

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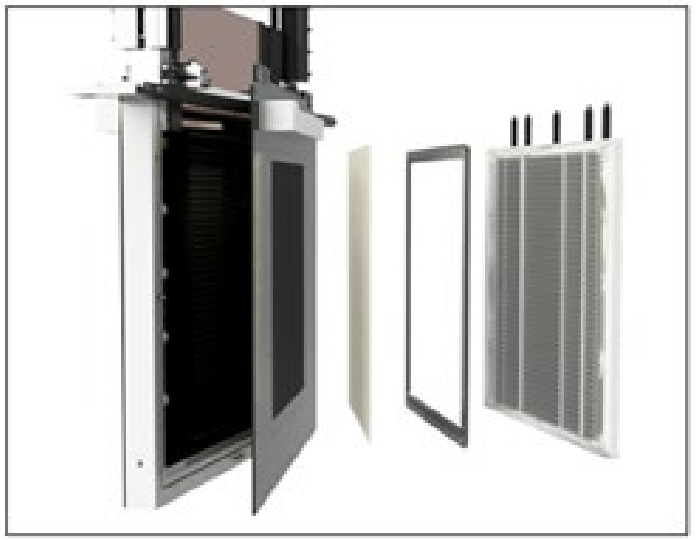
- ASMPT NEXX P500 plater for high CD/high speed applications
  - Single panel process modules, multi-zone anodes provide great control over current distribution. Ion exchange membranes reduce additive consumption.
  - Typical plating conditions: CD = 3-7 ASD, bath temperature = 25-35 °C, plating time **15-20 minutes.**



Contents of one side of a plating cell, including segmented anode and close-edge shield. The panel holder is shown on the left side.

Multiple chambers for multiple panels with each plating cycle

Plating process and parameters

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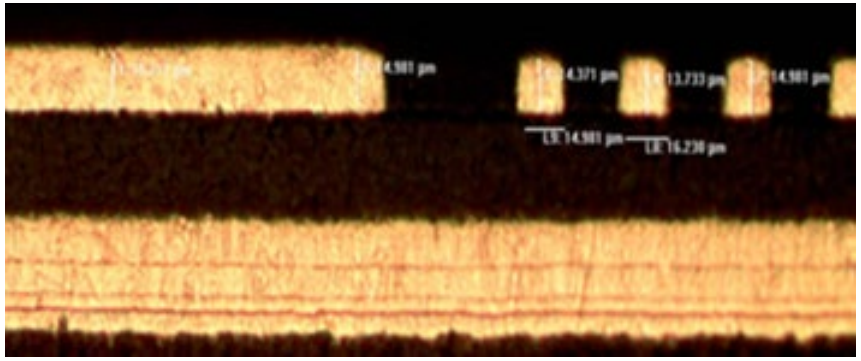
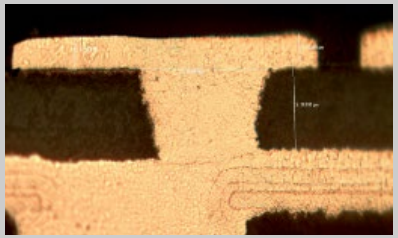
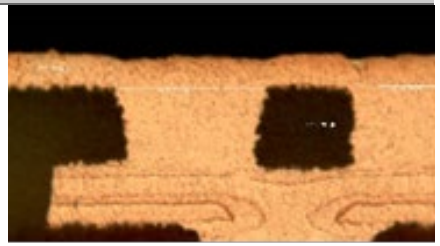
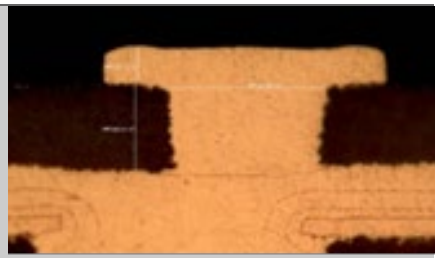
Plating conditions and concentrations

	Chemistry	Concentration	Function
VMS	**$CuSO_4$**	**200 – 240 g/L**	Source of copper ion
	H_2SO_4	**40 – 120 g/L**	Conductivity, prevents the precipitation of basic salts
	Cl^-	**50 ppm**	• Enhance the adsorption and inhibition effect of the wetter. • Integral to acceleration mechanism • Affects the appearance, structure, and internal stress of ECD copper
Additives	**Wetter**	**10-20 ml/L**	Suppressor
	Brightener	**2-5 ml/L**	Anti-suppressor, it is also called accelerator
	Leveler	**2-5 ml/L**	Secondary suppressor, critical to improve uniformity & performance
Plating Parameters	**CD**	**1.0-6.0 ASD**	Lower CD for VCP style plating tool, higher CD for single-panel plating tool
	Temp	**25-35 ºC**	Lower temperature for VCP style plating tool, higher temperature for single-panel plating tool, such as AMSPT NEXX P500 plater
	Solution agitation	**Eductor or shear plate**	VCPs utilize eductors for solution agitation whereas the P500 plating tool uses shear plate agitation.

VCP tool results

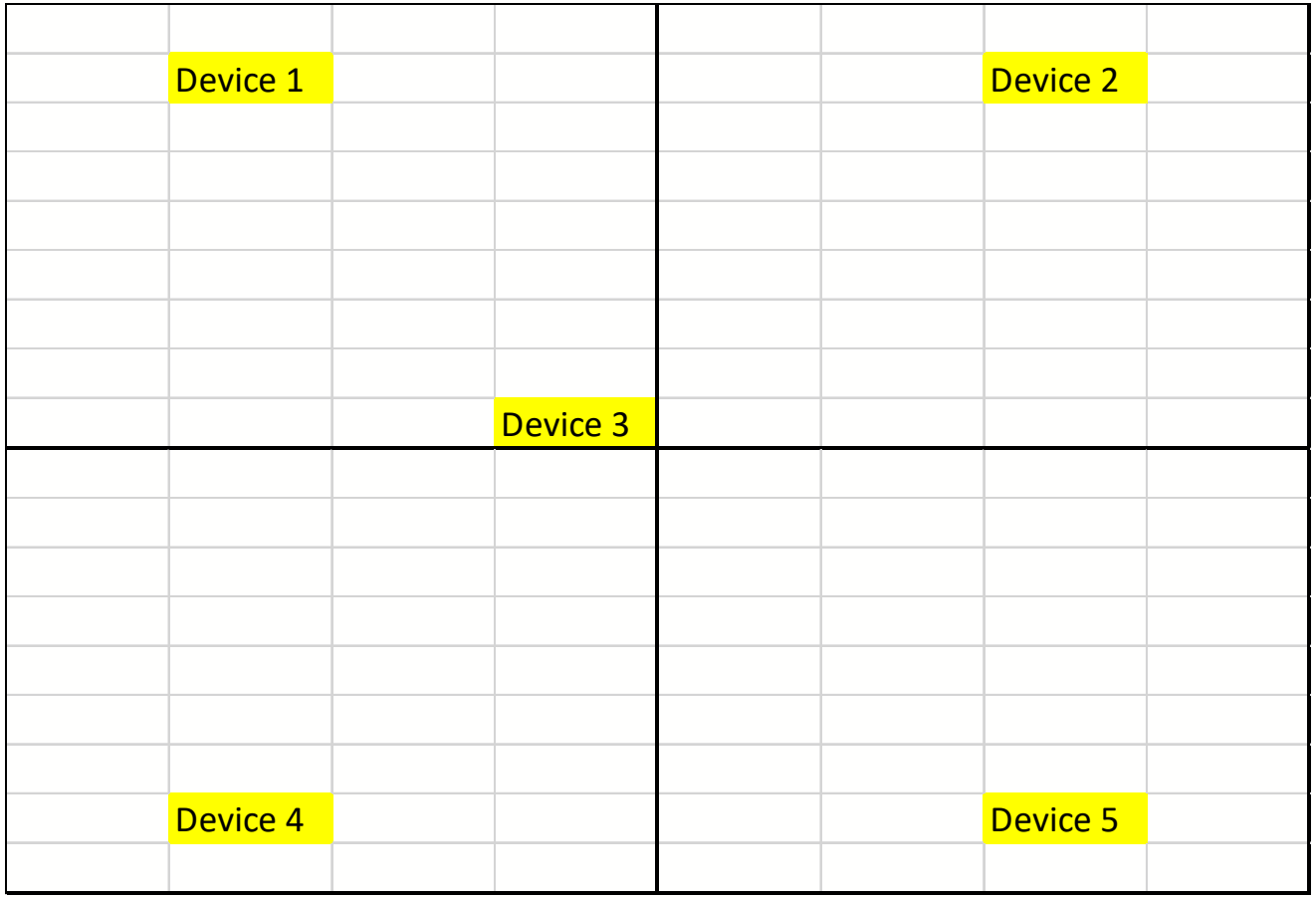
- 2-in-1 RDL panels were plated in VCP style tools at various conditions.
- 55x30 µm vias were filled while maintaining good uniformity between lines and pads.
- Full panels were not evaluated. Uniformity was analyzed by comparing features within unit.



CD (ASD)	Plating time (min)	Bath temp. (°C)	Via dimple	R value (µm)	Images
1.2	60	25	None	1.7	
4.5	15	25	None	2.7	
4.5	15	35	None	1.3	

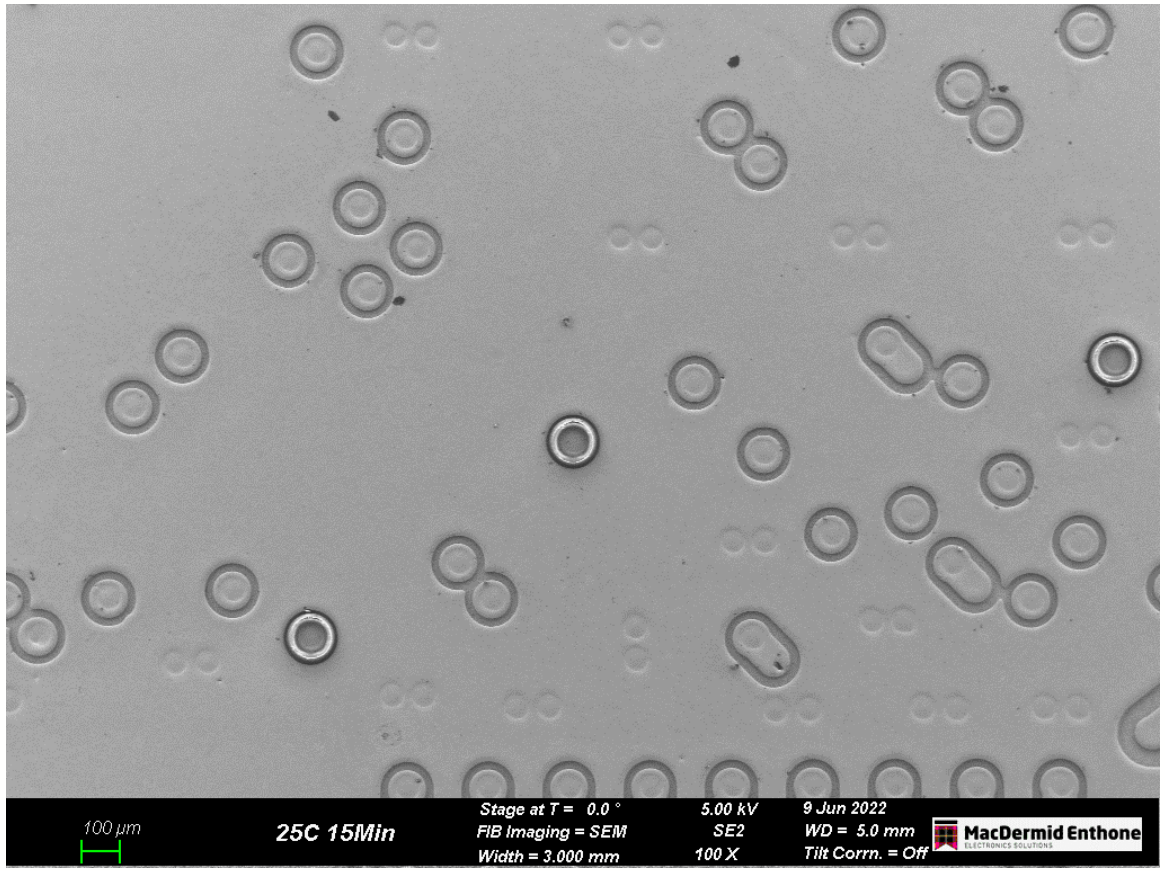
High speed panel plating results

- Panel size = 510 x 515 mm
- 5 dies were measured, per side, via Keyence VK-X1000 for the uniformity of WID and WIP
- Throughout trial, surface Cu was monitored and current density was adjusted across segmented anodes to minimize variation.

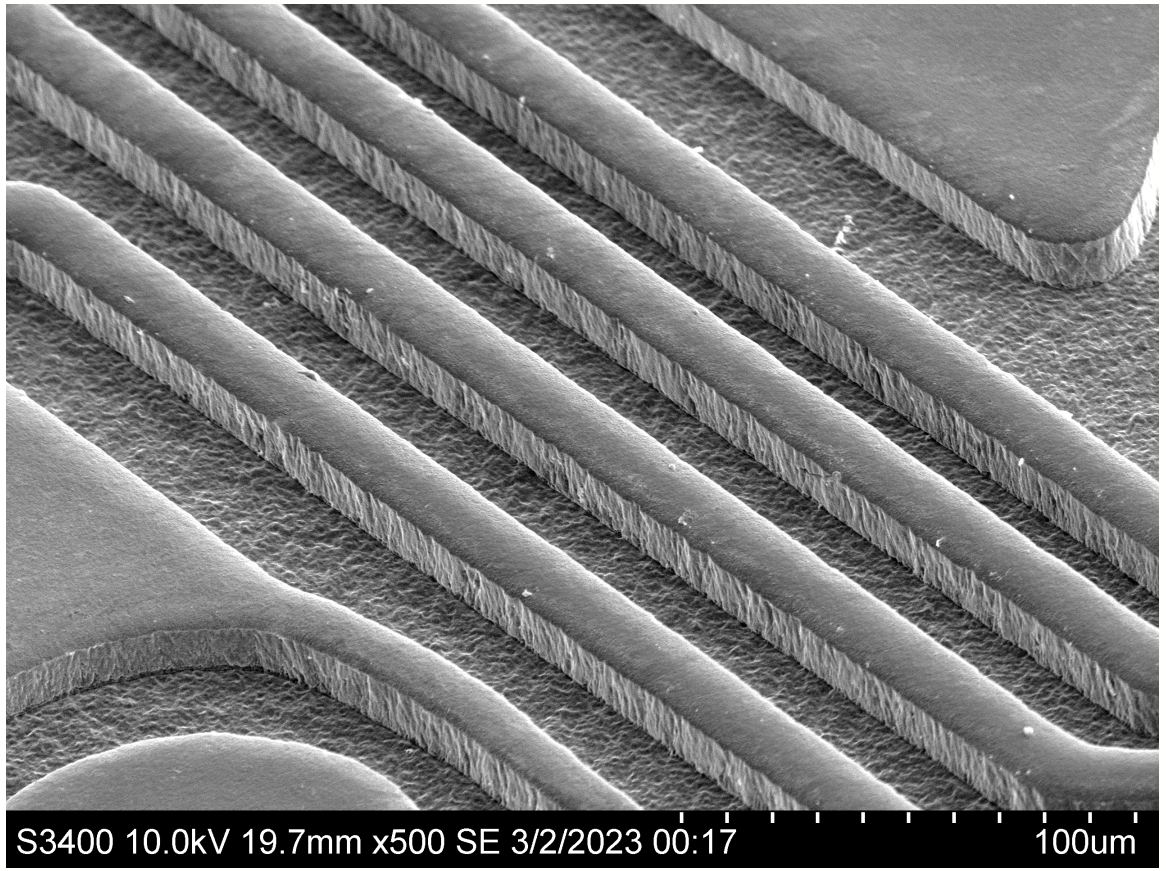


Plated IC Substrate features

- SEM images of Cu plated IC substrate



100X



500X

Example of profile measurements

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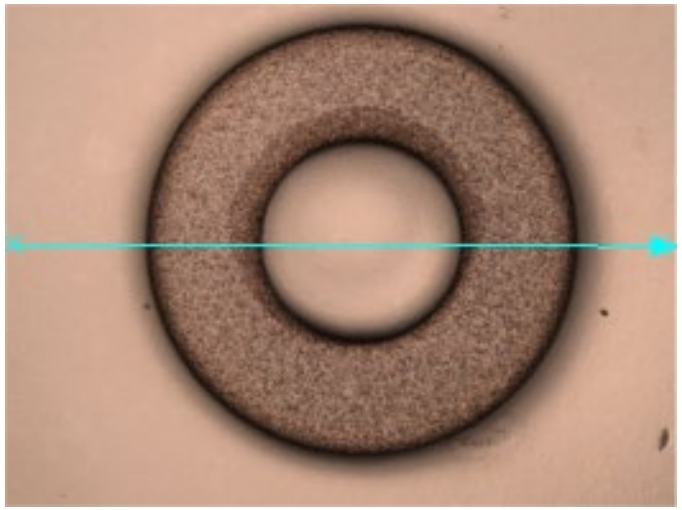
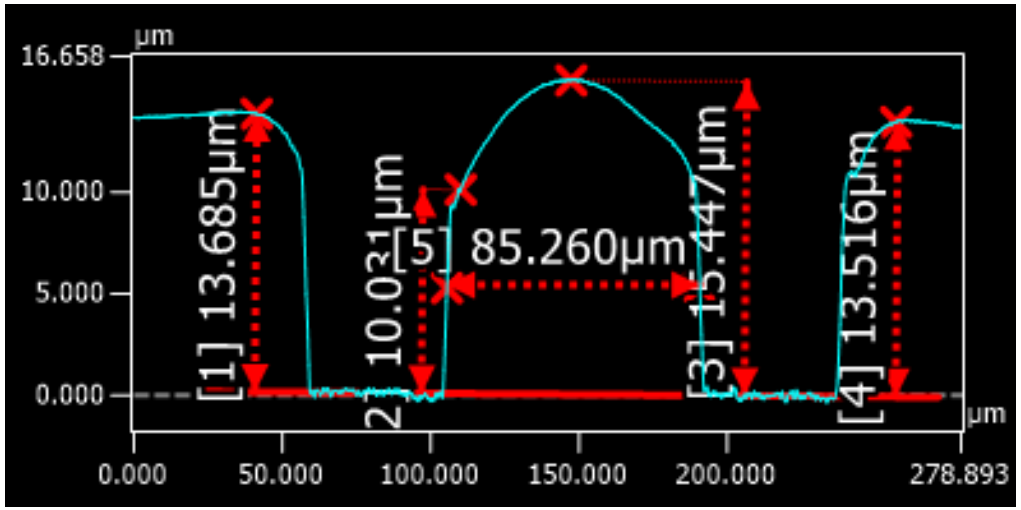
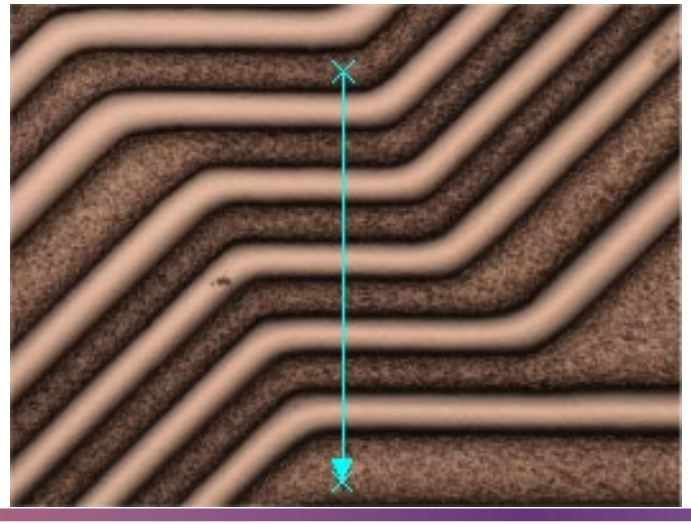
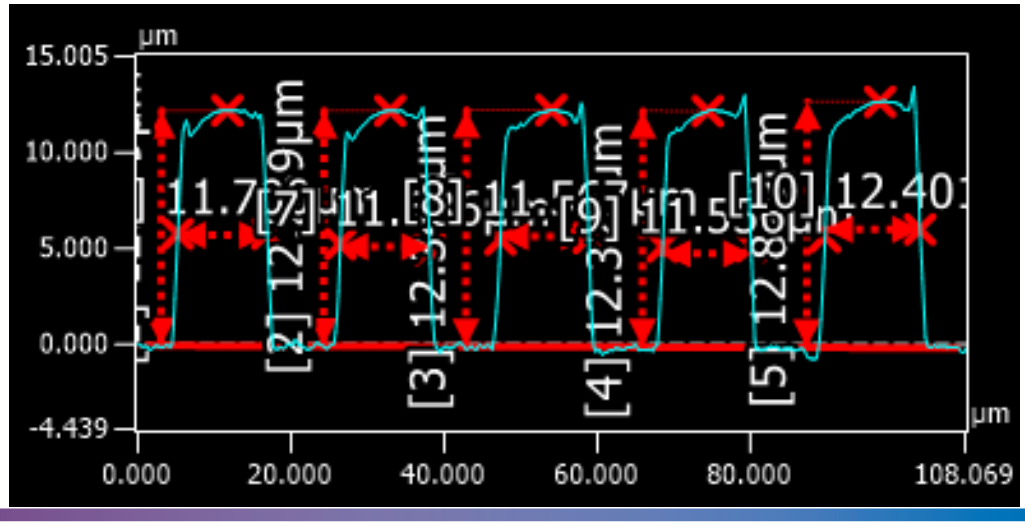
- Features were measured with and without dry film.
- Examples shown to the right have had the dry film removed.
- Feature above is a filled via. Feature below is a concentration of 12µm wide lines.









High speed panel plating results

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Panel with smaller vias, 40x15 µm, line width, 13 µm, CD at 4.5 ASD, 15 min, bath at 35 °C

- Both front and back sides were measured
- The uniformity of WID, ($Height_{pad}$ – $Height_{line}$) was 1.2 µm
- The uniformity of WIP% was about **5%** from both sides

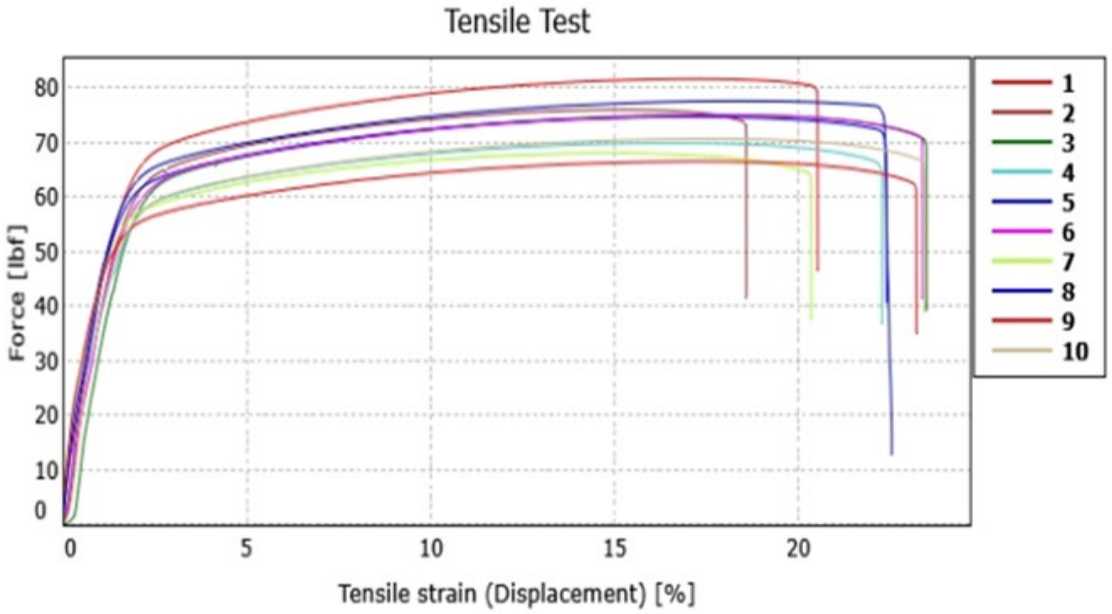
$$WIP\% = \left[\frac{Height_{Max} - Height_{Min}}{Height_{Avg} * 2}\right] * 100$$

Front side	Die 1	Die 2	Die 3	Die 4	Die 5
Fine line 1 height (µm)	12.3	11.4	12.1	12.4	12.1
Fine line 2 height (µm)	11.4	11.4	12.2	12.3	12.0
Fine line 3 height (µm)	12.2	11.6	12.1	12.2	12.1
Pad height (µm)	12.6	11.8	11.7	11.9	11.8
Uniformity WID (µm), H_{max}-H_{min}	1.2	0.4	0.5	0.5	0.3
Uniformity WIP (µm), H_{max}-H_{min}	1.2				

Back side	Die 1	Die 2	Die 3	Die 4	Die 5
Fine line 1 height (µm)	11.7	12.3	12.1	12.1	12.4
Fine line 2 height (µm)	12.0	12.3	12.0	12.4	12.5
Fine line 3 height (µm)	12.0	12.1	11.9	12.3	12.0
Pad height (µm)	12.2	12.3	11.4	11.3	11.7
Uniformity WID (µm), H_{max}-H_{min}	0.5	0.2	0.7	1.1	0.8
Uniformity WIP (µm), H_{max}-H_{min}	1.2				

Physical properties of deposit

- Physical properties are consistent after plating at various conditions.
- Elongation was greater than 20%.
- Physical properties exceeded IPC class III specifications.

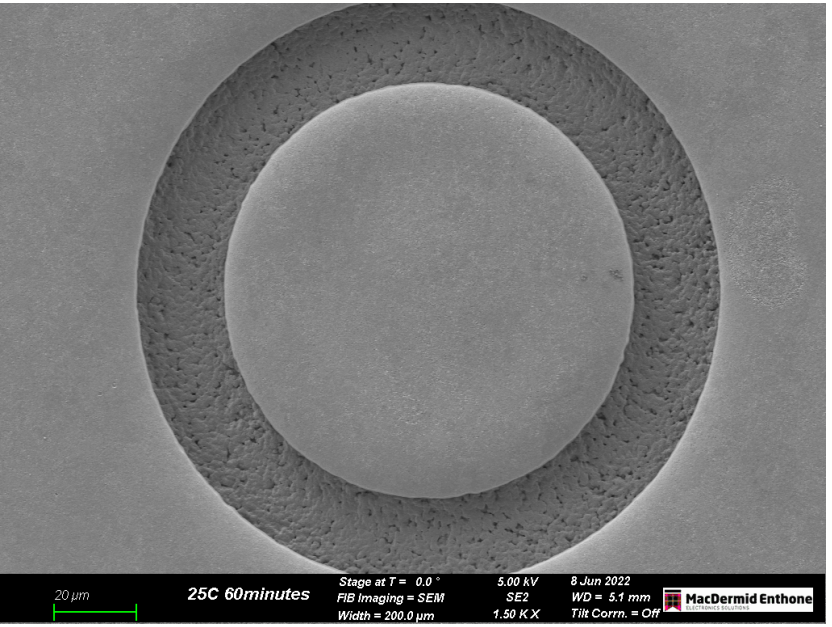


Plating Condition	2.0 ASD, 25 C	4.5 ASD, 35 C
Elongation%	22.0%	20.1%
Tensile Strength (PSI)	40.4 K	40.4 K
Internal Stress (tensile)	0.87 (Kg/ mm^2)	0.85 (Kg/ mm^2)

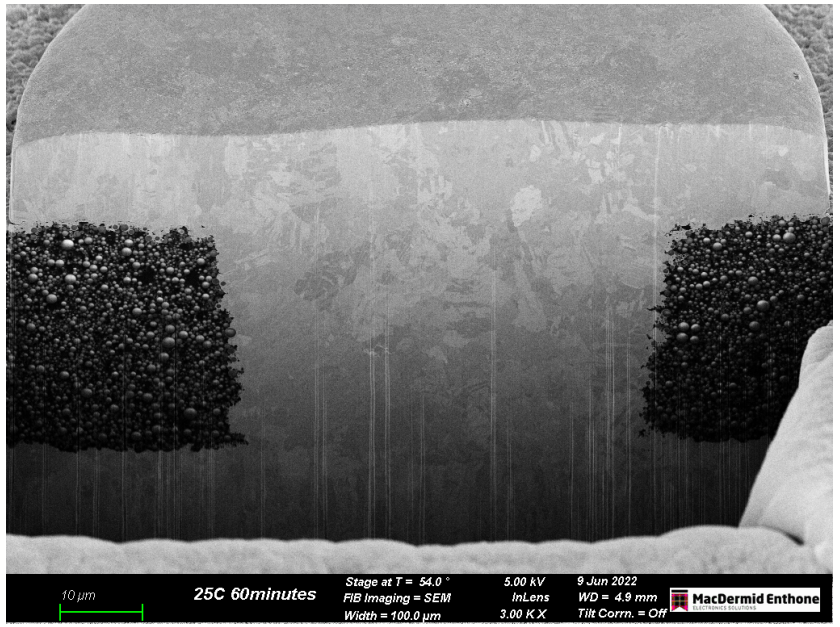
Grain structure evaluation

Sample was plated with a VMS of 200/100/50.

- Flat filled via as shown in cross-sections and profilometry measurement
- Deposit had equiaxial grain structure
- Grain structure was consistent under different plating conditions



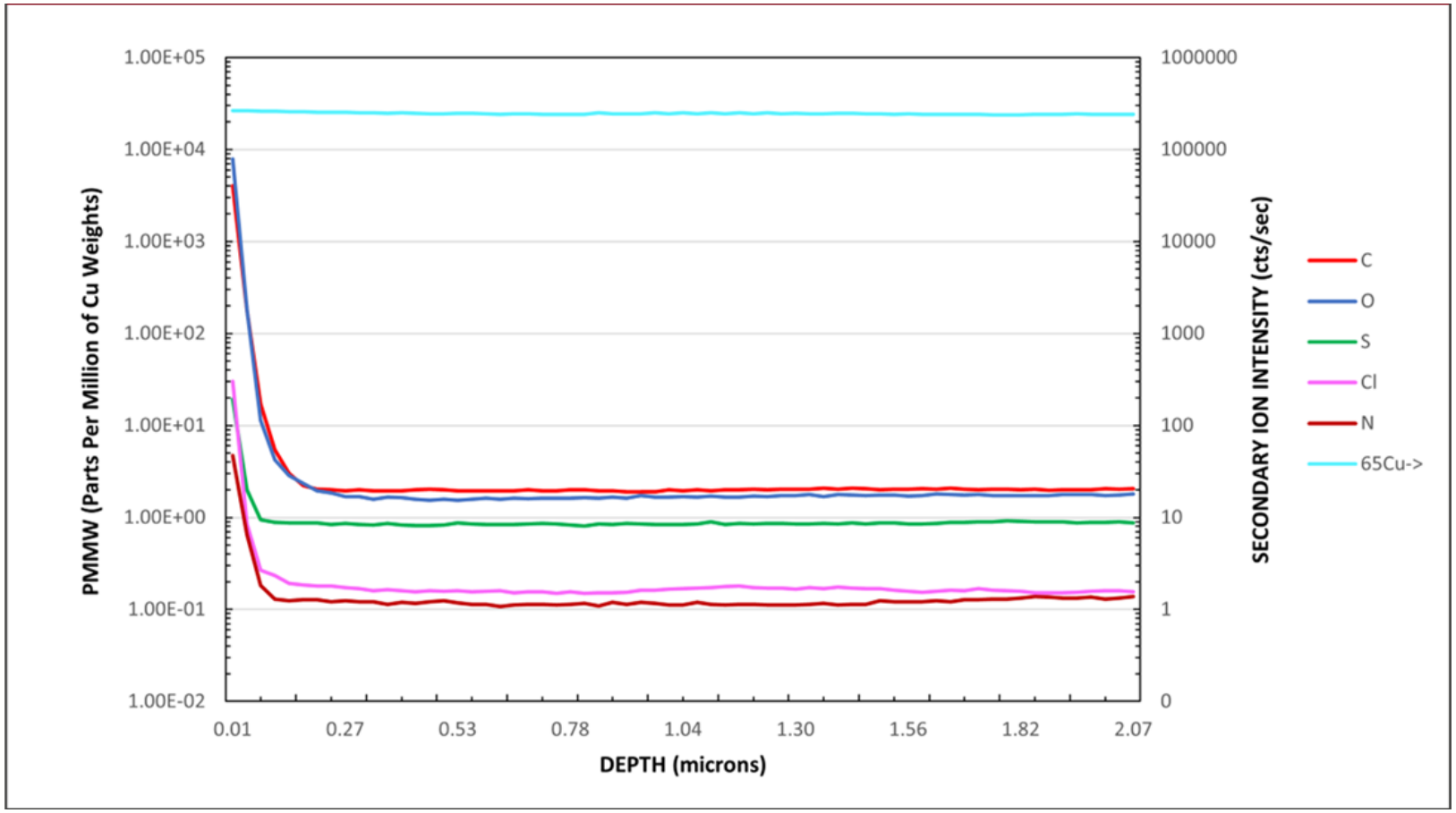
1500X



3KX

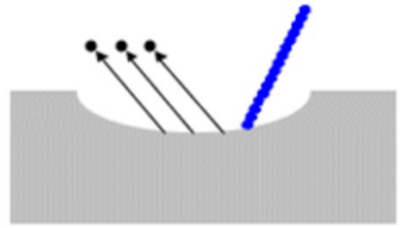
3KX – imaged via ion beam

SIMS Analysis – Cu deposit



Element	Concentration (ppmw)
Sulfur	0.848
Carbon	1.98
Oxygen	1.66
Chlorine	0.163
Nitrogen	0.114

Dynamic SIMS



- DC constant current (Cs^+, O_2^+)
- Material removal
- Elemental analysis
- Depth profiling
- Specific species
- Mass spectrometer: magnetic sector, quadrupole, time-of-flight (TOF).

Conclusion

- The acid copper plating process presented is designed for 2-in-1 via fill and RDL plating in SAP technology for IC substrate applications.
- VCP style plating tools or high-speed single panel plating tools, such as the AMSPT NEXX P500 plater, can be used to plate these types of features. System must be optimized for specific tool.
- The system (additives + plating tool) can provide excellent uniformity, both WID and WIP, if operating conditions are optimized.
- When the P500 tool was utilized, WID variation was below 1.2 µm, WIP% was below 5% across the panel (panel size of 510 x 515 mm).
- The copper deposits had low internal stress. Tensile strength and elongation passed IPC class III criteria.
- The deposits' physical properties and grain structures were consistent when plated at different current densities and bath temperatures.

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Thank you!
Questions?

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