Incorporating Hierarchical Construction for Advanced IC Packaging

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Hierarchy in IC Package Design

- LEF cell library definition
- DEF represents designs with multiple levels of hierarchically
- Technology constraint driven route planning
- Netclass partitioning
- Hierarchical block design creation
- RTL synthesis to standard cell library
- Material based models for stress and thermal
- Hierarchical circuit models in SI/PI
Hierarchy with Building Blocks

Primary Building Blocks
- SoC C4 PDN 1
- SoC C4 PDN 2
- Std HBM C4 Bumps

Intermediate Building Blocks
- SoC C4/UBM PDN 1
- HBM C4/UBM PDN1
- Top Bumps
- Bottom Bumps
- bnkB, bnkA

Soft IP SoC
- SoC Top and Bottom Bumps
- SoC C4/UBM PDN 1
- SoC C4/UBM PDN 2
Hierarchy with Parameterization

Dynamic planes for power/ground networks – parameterized by constraints and plane class

Technology driven bumps and vias with constraint driven (parameterized) trace routing
Connectivity in IC Design

Key Attribute
Connectivity remains in hierarchical context unless promoted by the tool
Connectivity in IC Package Design

Key Attribute
All defined connectivity promoted to the floorplan level
Chiplet Integration Workflow

System Inputs

Co-Design Planning & Prototyping

Physical Implementation

Sign-off & Verification

Modeling Fidelity

Predictive

In-Process

Final

SI/PI/EM Analysis

Thermo-Mechanical Stress Analysis

Substrate Verification

Assembly Verification

Data Management / Trust & Assurance

Ecosystem Integration – PDK/ADK/CDK and MCAD
Chiplet Integration Planning & Prototyping

**Design**
- Planning Cockpit
  - Eliminate iterations & drive better decisions
  - ML driven System Technology Co-Optimization
  - Predictive Analysis
  - Balance PPA & Cost
  - Eliminate problematic spreadsheets

**Mechanical Integration**
- NX
- HyperLynx, mPower
- Calibre xACT

**Signal & Power Integrity**
- STA
- 3rd Party
- Simcenter
- Tessent Multi die
- Calibre 3DSTACK
- Calibre nmDRC

**Thermal Analysis/Stress**
- DFT

**Package Assembly Verification**

**Substrate Verification**
- Physical Design
  - Xpedition Package Designer
  - Xpedition PCB
  - Aprisa P&R
  - 3rd Party P&R

**Logic Data**
- Verilog
- KYN
- CSV/TXT
- Schematic

**Silicon Data**
- LEF/DEF, GDS
- CSV/TXT

**PCB/PKG Data**
- ODB++, AIF
- CSV/TXT
- Die/BGA.txt

**ADK/PDK**
- Foundry
- OSAT
- Substrate Supplier

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Importing Building Blocks for Floorplanning

Bump map interface specification for fixed die – typically represented in csv format

Interface imported into floorplanning tool as a graphical part

Bump map of the JESD235B HBM Ballout A highlighting repeating die to die signal channel support regions in the 4097-bit wide interface.
Applying Building Blocks to HBM

Imported part from specification

Disaggregate into building blocks with BGA bump primary blocks

Reassembled design with BGA bumps
Managed Die to Die Interface

- Partition channels and signal groups for faster layout implementation and analysis
- Routing and SI/PI completed on a single bank of HBM routes and preserved into a parent block (Physical Reuse) circuit
- Hierarchical placements of parent block adapt to connectivity
Managed Die to Die Interface

Apply repeatable, reliable physical layout strategy to managed interface
Arrayed Building Blocks for BGA

Imported part from specification

Partition into building blocks with back-side bump primary blocks

Reassembled design with back-side bumps
Fast Design Iterations

Update bumps and connectivity in the L0 (level 0) block

Apply automation to update hierarchy and create unique signal interface at top using pin regions
“Smart” Pin Regions

Enables rapid hierarchical prototyping of complex ASICs and chiplets by using “smart regions”

- Smart Regions are parametric regions that can auto synthesize arrays of pins
- Region anchoring provides automatic region move when a region is resized
- Complete pin regions along with pin-numbering, signal assignments and net connections are automatically generated

VERY rapid design of complex bump arrays and implement design changes in seconds vs. days to weeks
Floorplan without Bumps

Streamline tool memory usage while floor-planning with the information that is relevant to the human brain.
Flood full chip with power/ground bumps

• Regenerate “h0PGcore” pin regions

• Apply expression-based pin numbering

• Auto Assign pins to checkerboard VDD/VSS
• Setup high speed interface pin region with staggered pin pattern, low impedance bump, 3x pitch and adequate “To Region Spacing”

• Regenerate pins, pin numbers and signals for high-speed interface
Staged Bump Generation – Step 3

- Setup high density interface pin regions with hexagonal pin pattern with various pin pattern radius
- Define sub-regions to generate signal sets
- Regenerate pins, pin numbers and signals high speed interface
Interactive Region/Groups Properties

- Total pin count shown in Regions / Groups Properties window
Define BGA Bumps

- Comprised entirely of parameterized pin regions
  - Geometric outline of SoC with notches for HBM building blocks
  - No Connect bumps to meet assembly rules on edges
  - Nested IO regions at bottom and top embedded with VDD and VSS
Assemble Full Design

- Placement of generated Soft IP SoC with hard HBM die to die building blocks
- Placement of generated BGA bump building block
- Placement of 4 HBM parts defined by imported CSV specification
- BGA bump signal assignments optimized with unraveling

Simply update region boundaries and regenerate pins and connectivity to accommodate design iterations
Summary

Two new methods introduced to Incorporate Hierarchy in your package design

• Hierarchical Building Blocks
• Parameterized “Smart” Pin Regions

Intuitively generate a complete silicon interposer package floorplan with imported building blocks and “Smart” pin regions

• Leverage your managed die-to-die interface blocks
• Define power/ground and signal bumps with a set of geometrical shapes
• Bypass need for the tool to render bumps during early design

“Smart” Pin regions with interactive graphical editing enable fast and intuitive design updates
Thank You