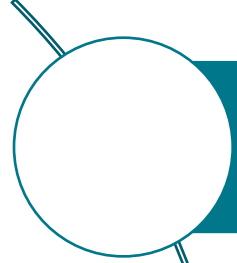




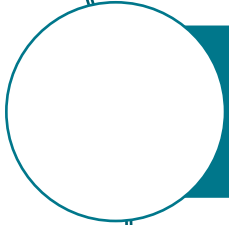
Enabling Co-Design of 3D Heterogeneous Packages

John Park
Product Director

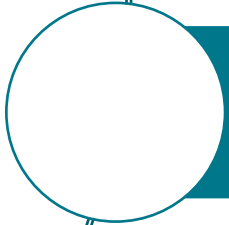
Outline



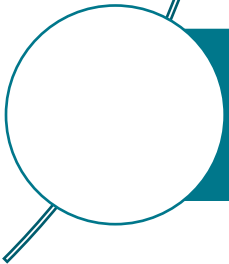
Trends



Challenges



Solutions



Conclusion

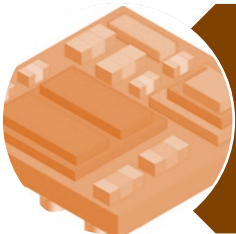
The Beginning of the “More Than Moore” Era



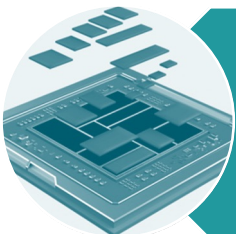
For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore's Law. But things are changing...The economics of semiconductor logic scaling are gone...



Gordon Moore knew this day would come. He also predicted that *"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."*



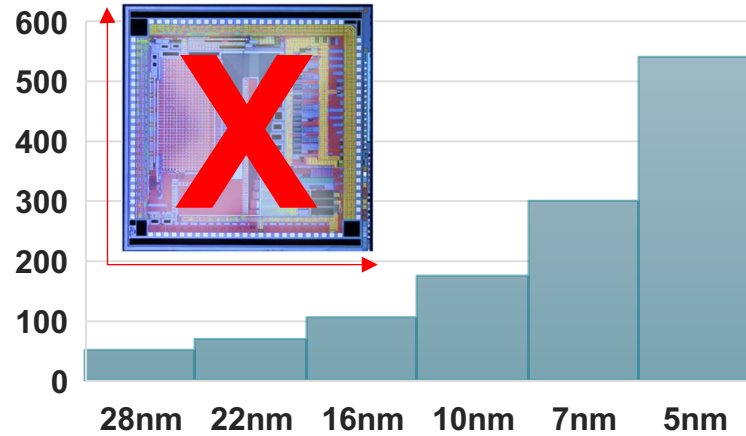
Providing a possible alternative to advanced monolithic SoCs, multi-chiplet SiPs have become a very attractive option for cost-sensitive complex designs



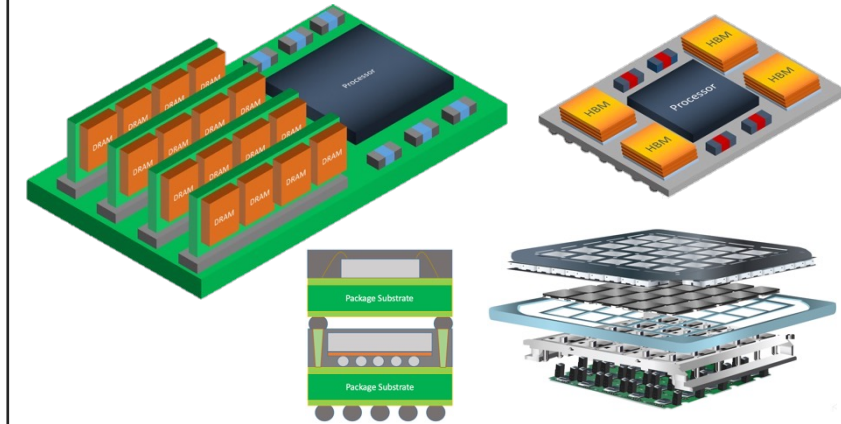
The generation of “More Than Moore” is here...

Simply Following Moore's Law Alone is No Longer the Best Technical and Economical Path Forward

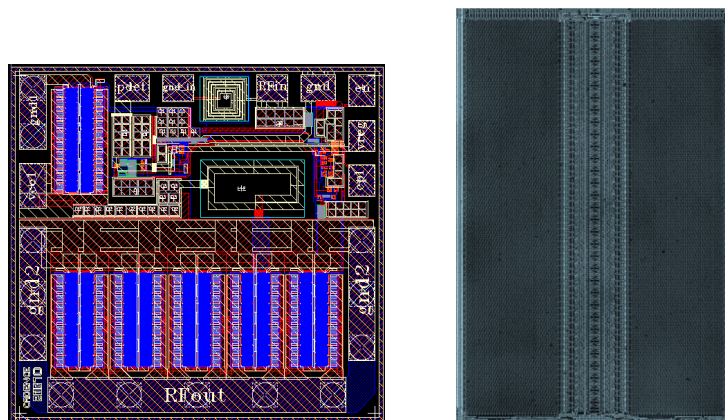
Cost & Yield & Size



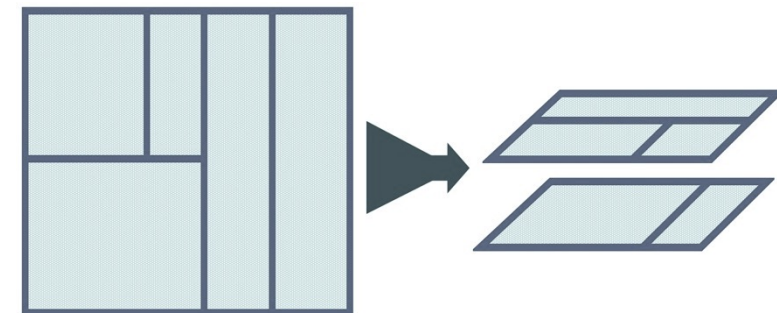
Lower Memory Wall



Analog/RF, I/O & Memory

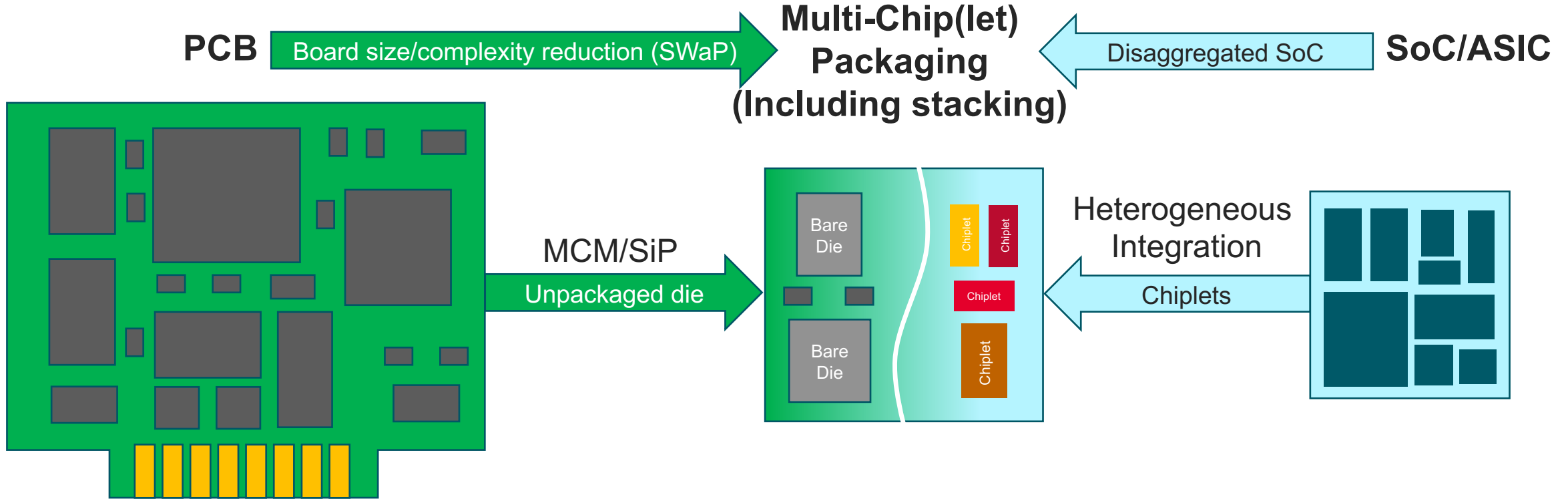


Form-Factor & Modularization



SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures

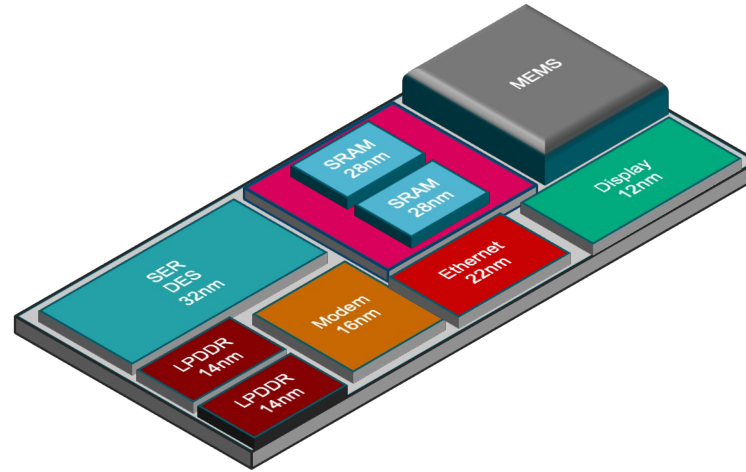
The transition from system on a chip (SoC) to system in a package (SiP)



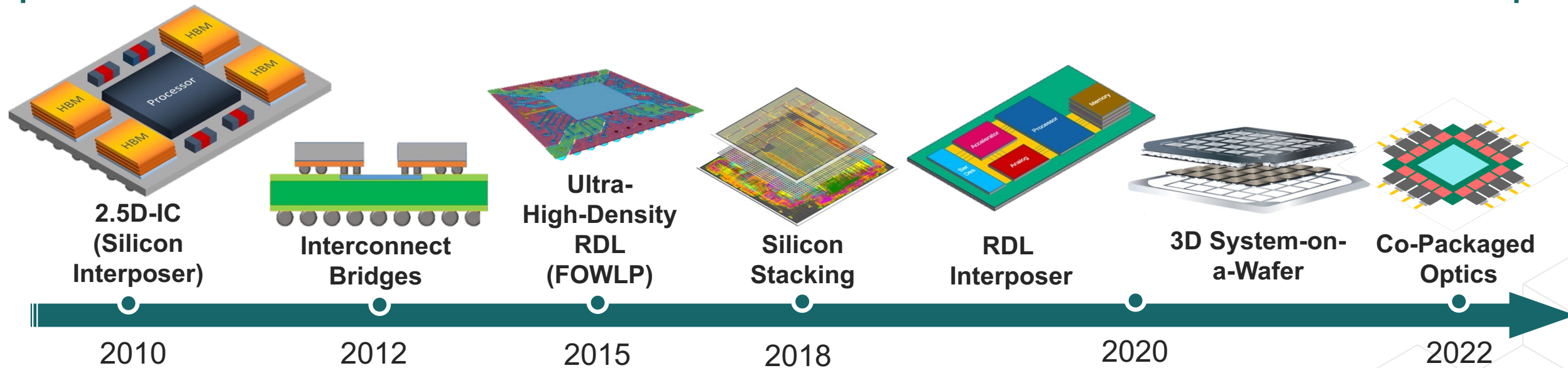
PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

Heterogenous Integration Leverages Multiple Packaging Technologies



Heterogeneous Integration



The Needs of IC and Systems Designers are Converging

OSATs (SWaP)

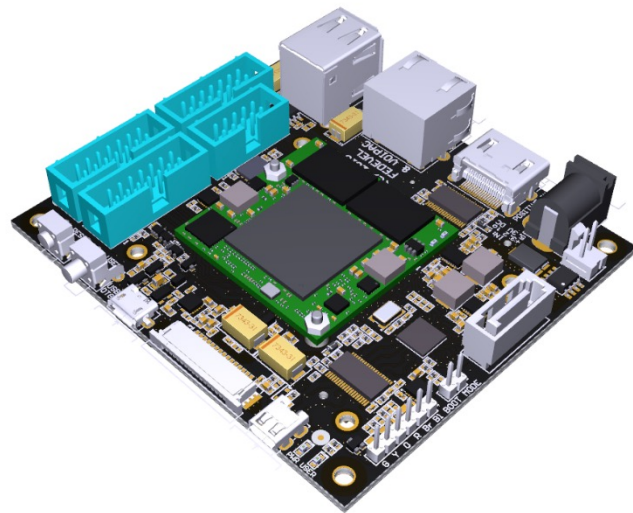
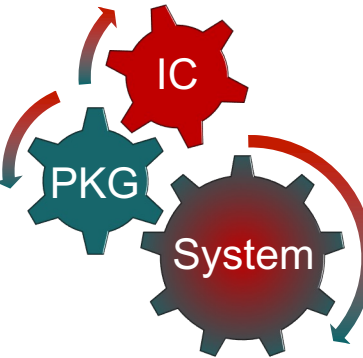
Board design impact on packaging

1980-2010

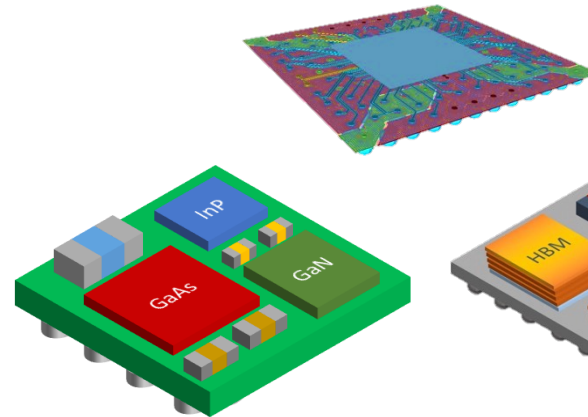
Foundries (PPA)

IC design impact on packaging

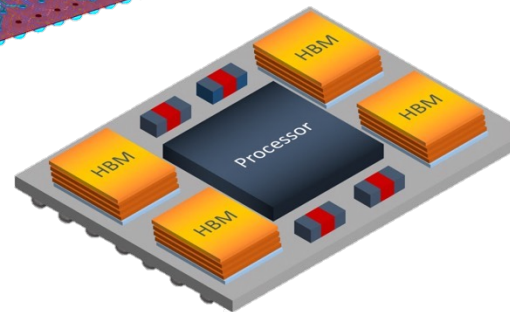
2011-Now



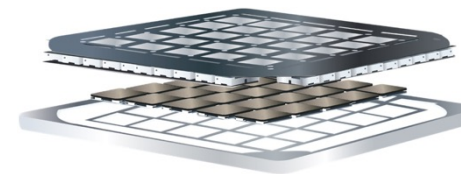
PCB Layout Flow
System-Level Analysis



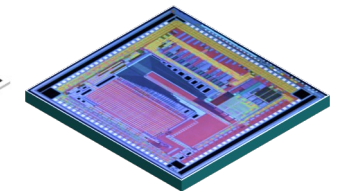
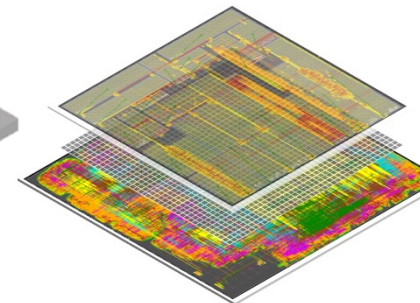
PCB-like Flow
System-Level Analysis



IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis



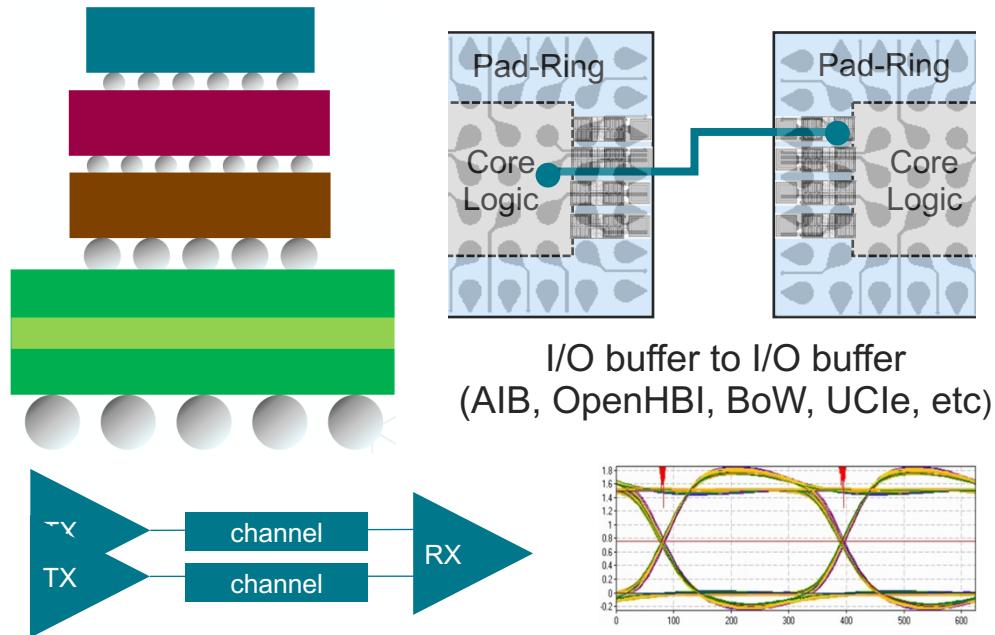
IC Flow
IC signoff Methodology



3D Packaging Versus Silicon Stacking (3DHI)

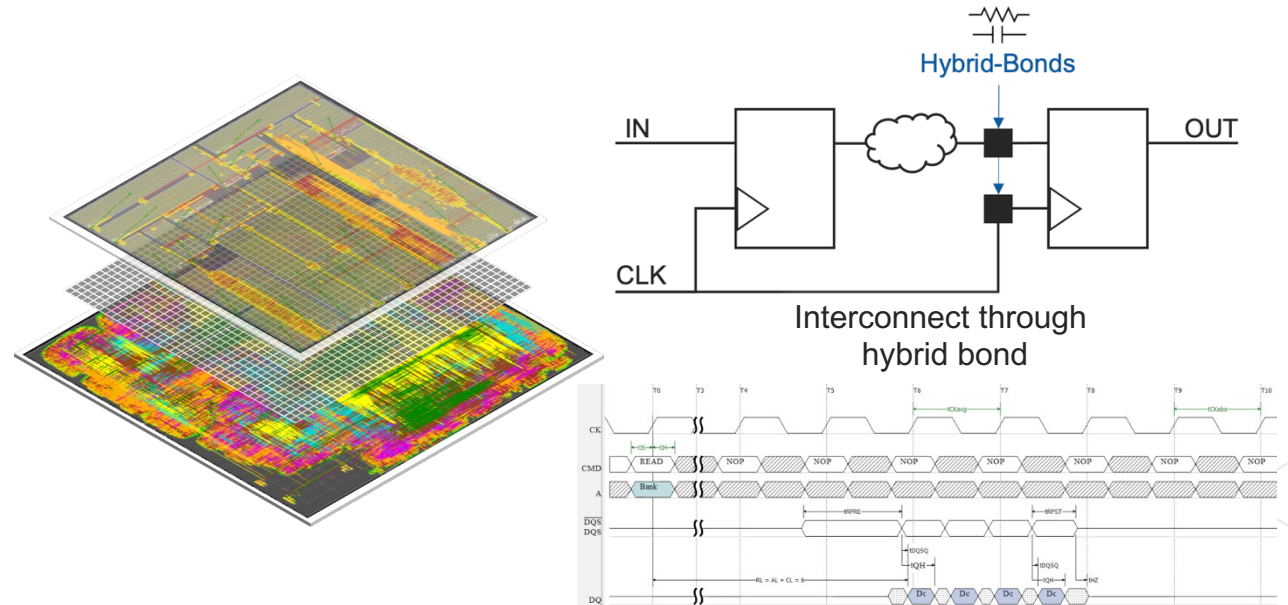
3D Packaging

- Solder-based connections ($>25\mu\text{m}$)
- Each die designed independently
 - Black-box abstracts used for layout
- I/O buffer to I/O buffer signaling



Silicon Stacking

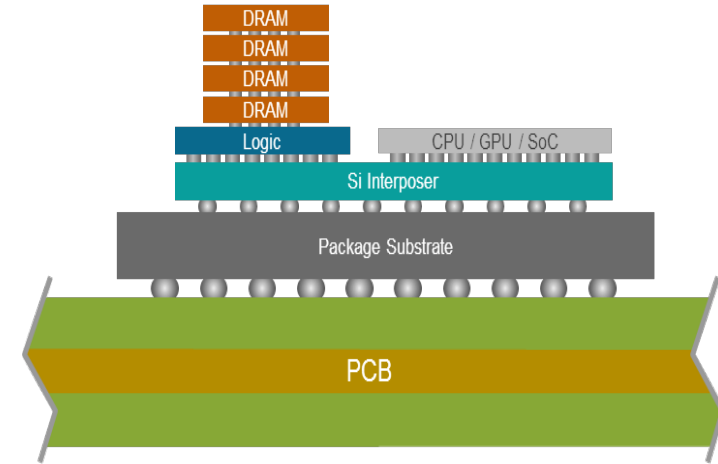
- Solder-free connections ($<10\mu\text{m}$)
- Single RTL partitioned at implementation
 - Full detail of IC required for layout
- DBI, hybrid-bond, cu-to-cu, direct connection



Times Have Changed...

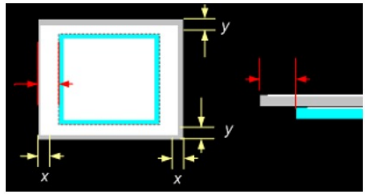


- Yesterdays Advanced IC Packaging
 - *Necessary evil*
 - Avoid negative impact on chip
 - Electrical, Thermal
 - Protect chip from the outside world
 - Redistribute IO to pitch more suitable for the PCB layout

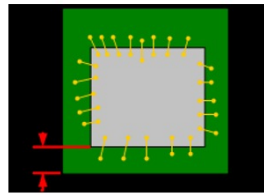


- Today's advanced IC packaging is about *adding value* to end products
 - Multi-chip(let) solutions leading the way for “More than Moore” vision
 - Companies leveraging packaging technologies to create value and differentiation from their competitors
 - TSV, WLP and 3D stacking technologies providing a tremendous number of packaging options for all form-factors and budgets

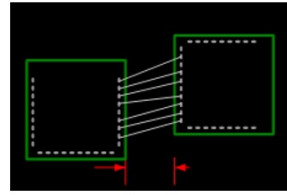
Multi-Chiplet 3D Diverse Ecosystem Challenges



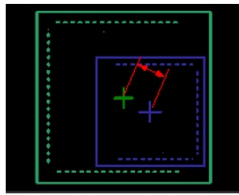
Die/Chiplet Overhang



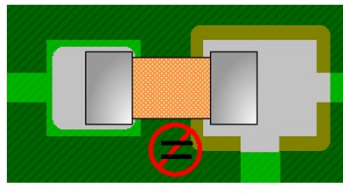
Die/Chiplet Spacing to Substrate Edge



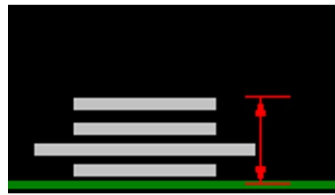
Die/Chiplet to Die/Chiplet Spacing



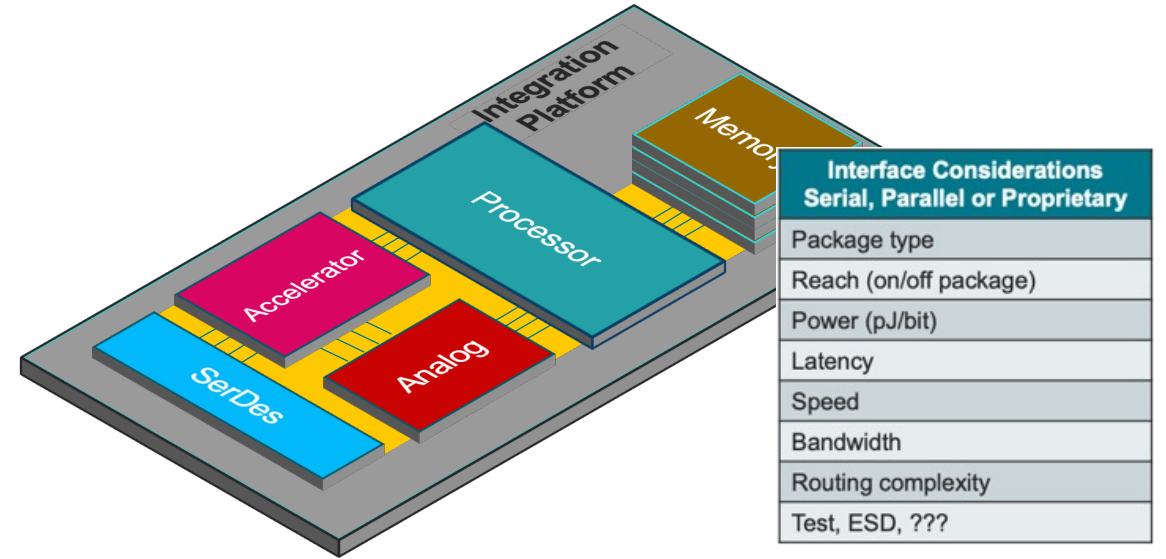
Die/Chiplet Center to Center Offset



Tombstone Effect (% size diff)



Die/Chiplet Stack Height



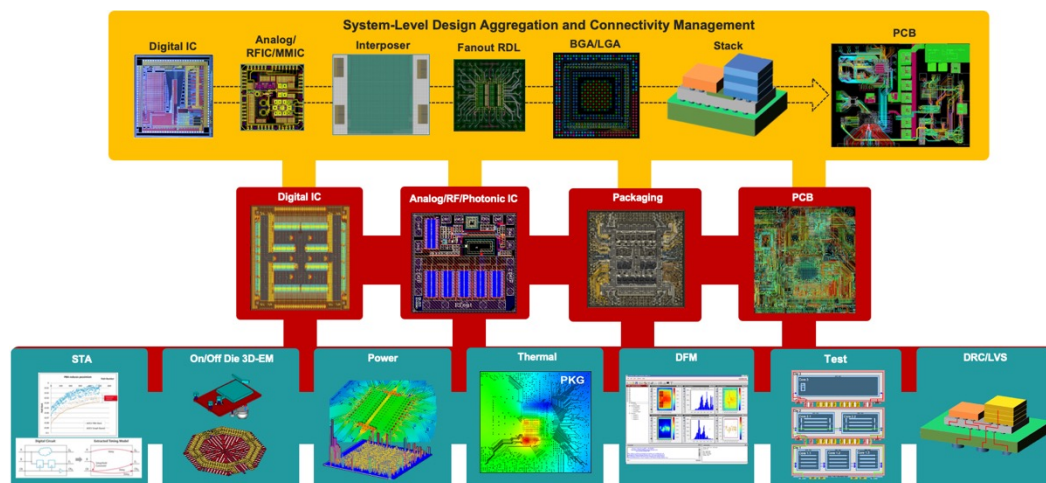
Assembly Design Kits

- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
- Foundries need to provide the packaging engineer all the data he/she needs to produce manufacturing output of a design that can be assembled and tested
- Contents; tech files, libraries, assembly rules, substrate DFM, rule decks, and design templates
- Security and Test solutions

COTS Chiplets

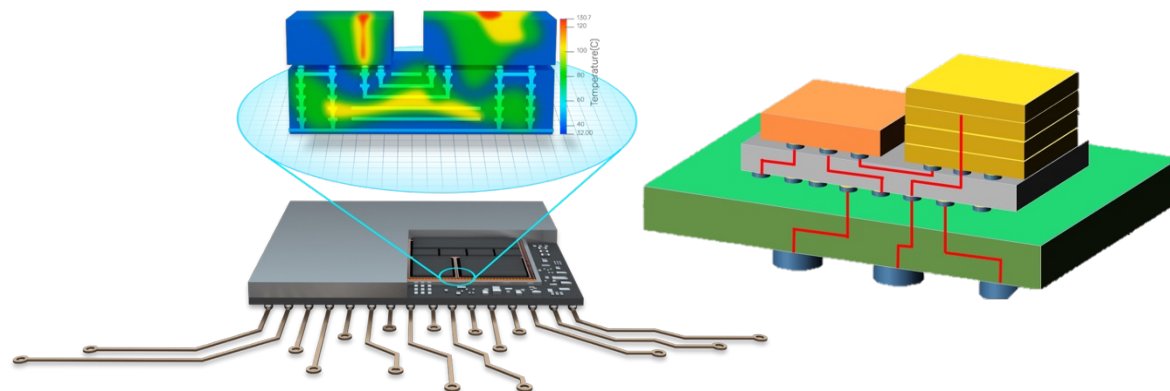
- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
 - CHIPLET.US
- Progress with chiplet exchange formats
 - CDX, 3Dblox™
- Common communication interface
 - AIB, UCIe, BoW, ...
 - Too many packaging options to standardize on a single interface

Multi-Chiplet 3D Flow Challenges



Design Tools/Flows

- Explosion in the number of design tools and required expertise mean complex design flows
- **Co-design/co-analysis across die/chiplet/package is now mandatory**
- Capacity and performance impact on tools
- Support of existing and emerging 3D-IC standards
- Silicon stacking breaks abstract die representation use model
- Package designers pivoting to foundry-based design and sign-off requirements

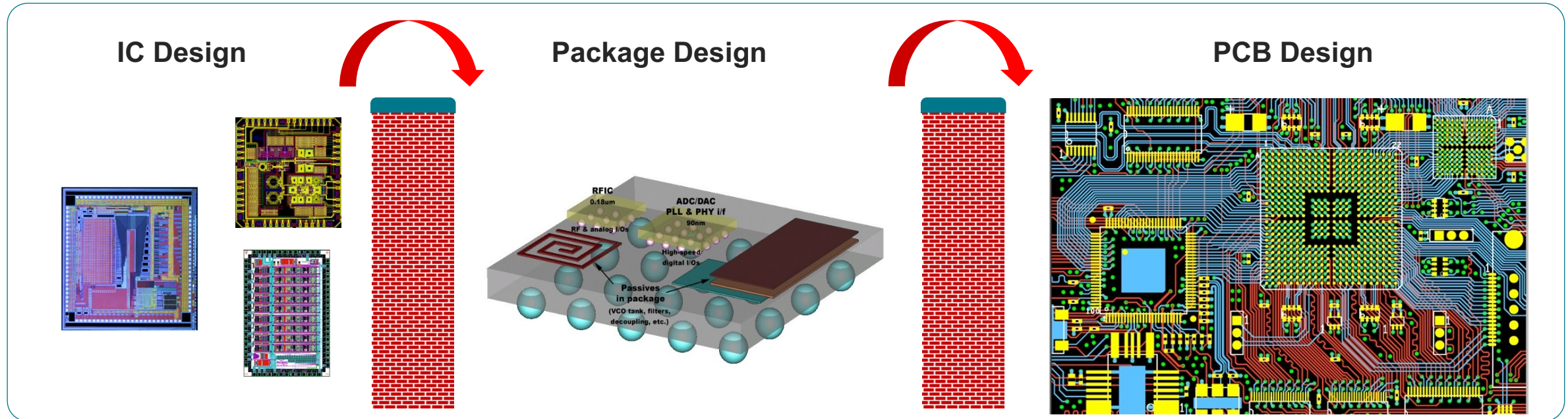


Analysis and Sign-Off

- Early-stage and signoff-level thermal/power analysis
- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Stacked-die EMIR
- Stress and CMP planarity checks
- New 3D-IC test standards
- High-capacity EM/SI/PI to support very large structures (billions of instances)
- Compliance kits for new chiplet-to-chiplet communication standards

Over-the-Wall Approach Fails For Analog/RF 3D HI Packaging

- Separate logic/design capture means no system-level LVS (SystemLVS) and redundant schematic/libraries.
 - Many manual steps between domains
- IC designers use estimated package and PCB layout parasitics, leading to unexpected performance limitations



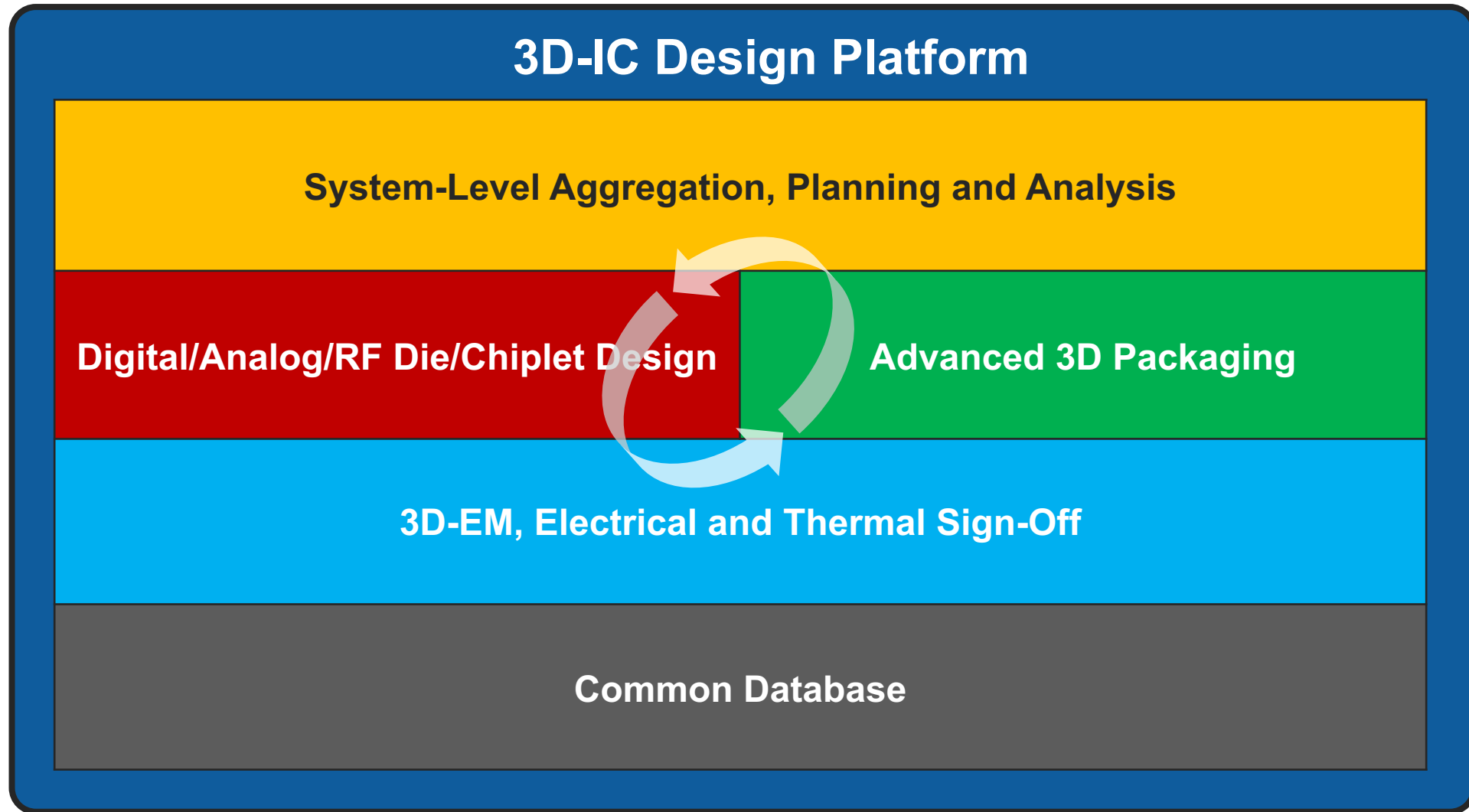
- Traditional design methodologies are breaking down

Why Can't We Have One Layout Tool For Everything?

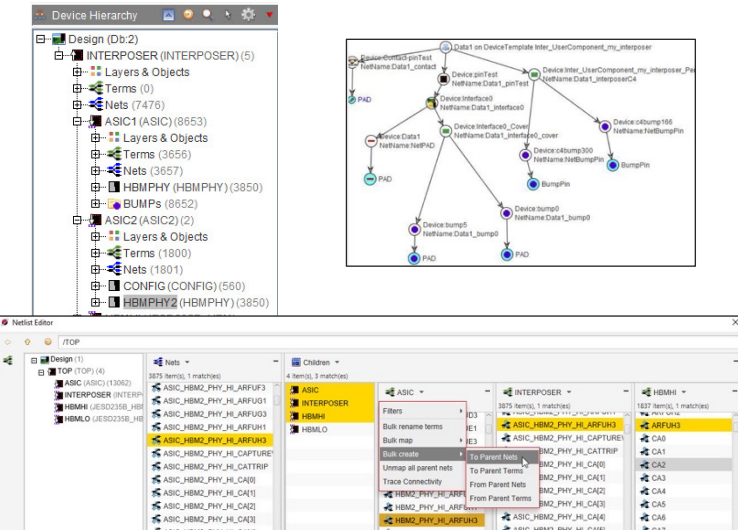
- Each platform has inherent advantages and disadvantages
- Capacity should be considered
- Two or more platforms often required to create optimal design
- Cross-platform solutions improve domain to domain data exchange/co-design

	Package/PCB	Analog/RF IC	Digital IC
Architecture	GUI-centric layout	Schematic capture, hierarchical layout	Language-driven flat design
Package Type	BGA/LGA, FOWLP, PoP, Si bridges	RF module, Photonics	2.5D-IC, 3D-IC
Die Model	Blackbox abstract	Transistor level	Standard Cell level
Routing Styles	Constraint-driven, push/shove 45-degree routing	PDK-driven, 90/45 degree/CurvyCore™ routing	Timing-driven routing, 45-degree RDL routing
Capacity/Perf	100,000s	1,000,000s	1,000,000,000s
Extraction/Analysis	3D-EM, SI and PI	RC Extraction + 3D-EM	RC Extraction
Manufacturing Outputs	Board/Substrate Foundry	Foundry	Foundry
Physical Verification	Only required in some applications	Sign-Off DRC and LVS	
OS	 Windows, Linux	Linux	Linux

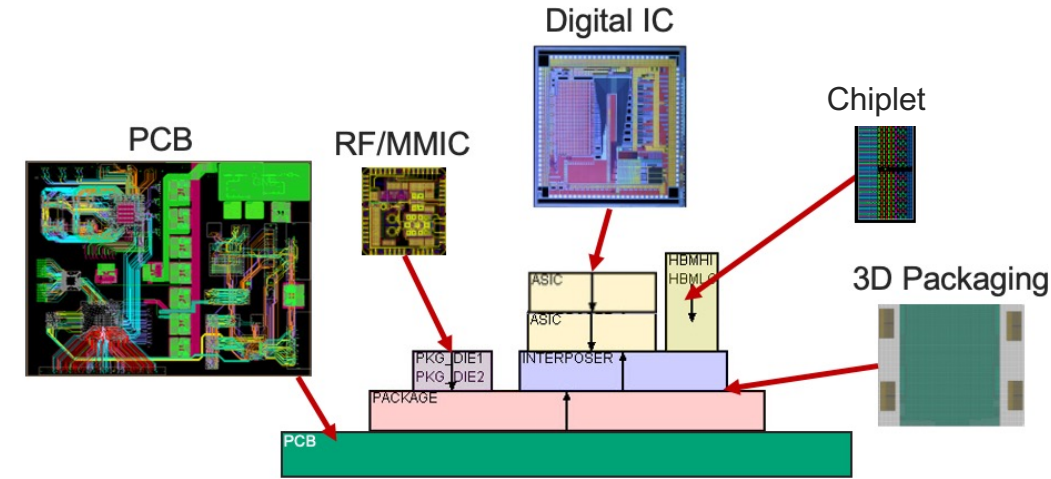
High-Level Co-Design Flow



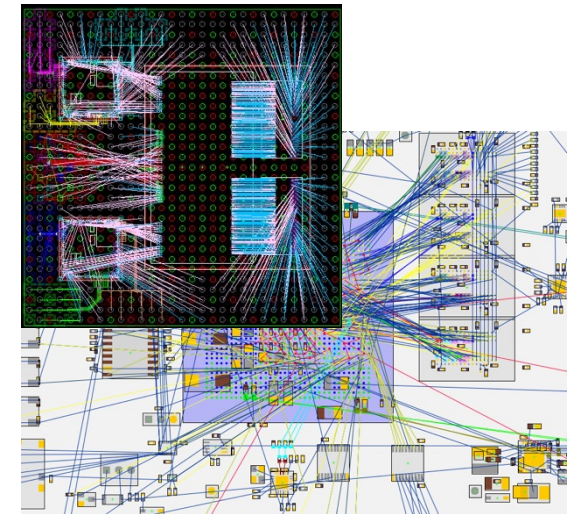
Digital-Centric Top-Level Aggregation, Co-Design and Optimization



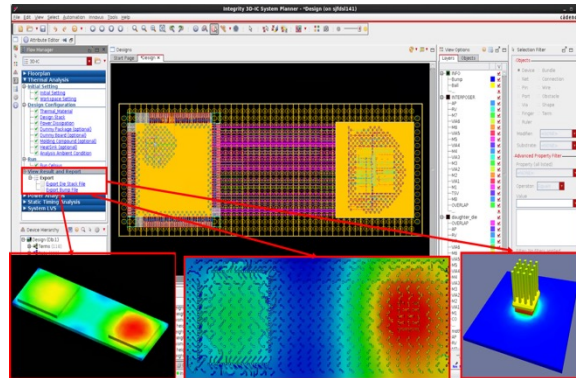
Multi-design management with chip(let)-chip(let)-package-board signal-mapping



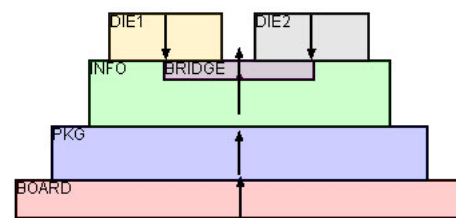
Hierarchical Planning and Optimization of System-Level Design and Connectivity



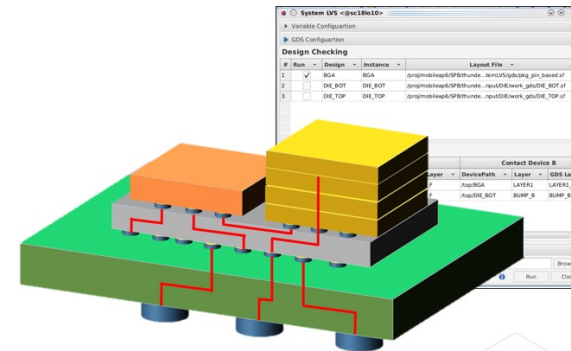
System-level co-optimization



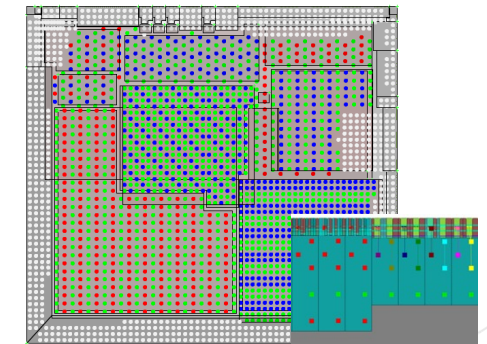
Early-Stage Thermal/Power Analysis



Stack management (Supports 3Dblox™)



System-level connectivity/stack alignment verification (SystemLVS)



Advanced bump/TSV planning

Flexibility Importing Design Data Into Co-Design Platform

Flow Manager

General flow (Default)

New Layer stackup...

IC

- Import
 - DieAbstract...
 - LEF/DEF...
 - Die CSV...
 - OIO...
 - Die TexT...
- Create Device...
- Create Devices Pattern

PKG

- Import
 - Allegro DRA...
 - Allegro BRD, SIP, or MCM...
 - Package CSV...
 - OIO...
 - AIF...
 - SPEED...
 - BGA Text...
- Create Device...
- Create Package...
- Create Pins Pattern

PCB

- Import
 - DieAbstract...
 - LEF/DEF...
 - Allegro DRA...
 - Allegro BRD, SIP, or MCM...
 - Die CSV...
 - Package CSV...
 - OIO...
 - AIF...
 - SPEED...
 - BGA Text...

TSMC 3Dblox™ Standard

Chiplet + Stack + Connection Information

DieID	DieID	DieID
DieID1: 001	DieID2: 002	DieID3: 003
loc: [100, 100]	loc: [100, 100]	loc: [100, 100]
face: down	face: down	face: down
orient: R180	orient: R180	orient: R180

3DFabric™ Design Templates

- InFO-3D
- SoIC
- CoWoS-L
- CoWoS-S

TSMC 3Dblox™

Build On-The-Fly

Create Package Parametrically

Substrate (BGA) > Package (U1) > Ring > Bound

Pin Pattern

Pattern Type: Center Array with Two Outer Rings

Start Pin Numbers: Center Array with Two Outer Rings

Outer Ring: Center Array with One Outer Ring

Inner Ring: Center Array with One Outer Ring

Center Array: Center Array with One Outer Ring

Columns: 20 Rows: 20 Pin Pitch: X 2000.00 Y 2000.00

Ring Depth: 2 Stagger Pins

Pad Template: Rotation 0.00

Unit: micron

Assembly Design Kits (ADK)

- TechFiles
 - Layer stack-up
 - Material
 - Properties
 - Thickness
 - Physical/Electrical layout constraints
 - Line and space
 - Differential signaling
 - Customized in-design DRCs
 - Design templates
- Design Libraries
 - Footprints & Power/Thermal models
 - Chiplets
 - Discrete
 - BGA/LGA/Interposer
 - TSV
 - ubump
 - C4
 - STEP Models
- Assembly Rules
 - Device placement constraints based on assembly pick & place equipment
 - Device to device spacing
 - Device to obstacle
 - Device to edge
 - Max stack height
- Compliance Kits
 - Electrical spec validation of chip(let)-to-chip(let) interfaces
 - Interconnect library
 - IO libraries
 - Eye masks
 - Jitter tolerance
 - Insertion loss
 - Return loss
- Manufacturing Rules
 - Board/substrate manufacturing process
 - Substrate checks
 - Soldermask checks
 - Soldering issues
 - Silkscreen checks
 - Tech file compare

ECO Flow With Layout Tools

Compare DeviceTemplate 'BGA' to 'BGA'

	BGA	BGA
AK4 net	DTB1[27]	DTB1[28]
AL4 net	DTB1[28]	DTB1[27]

Net Changed (2)

Port Location Changed

Current Difference

Pin 'AL4' net was changed from 'DTB1[28]' to 'DTB1[27]' for DeviceTemplate 'BGA'.

Select Show

Next Merge Accept Selected Accept All Filter... Write... Done

Industry Standard
Formats

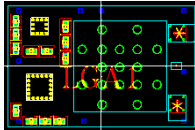
Assembly Design Kits (ADK)

ECO Flow With Layout Tools

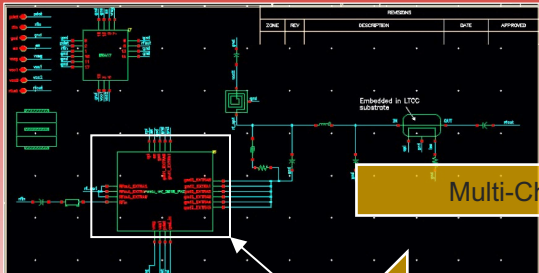
Schematic Driven (Analog/RF) Co-Design/Analysis Flow

- Chip(let)/package (multi-PDK) co-design/analysis solution built on IC design platform

System-Level Libraries

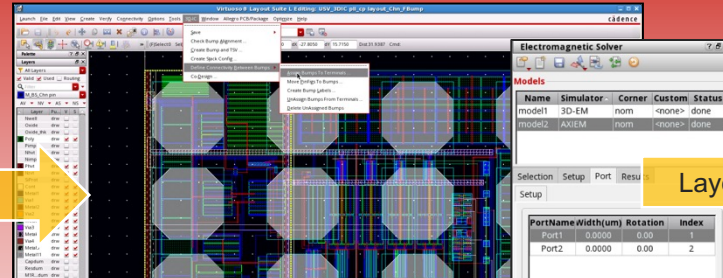


Schematic-Driven Multi-PDK Design
Single system-level hierarchical schematic to drive multi-chip(let) design and verification

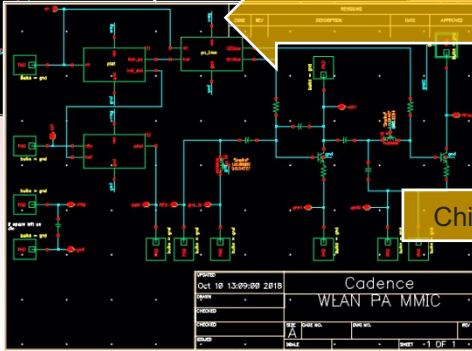


Multi-Chip(let) Layout

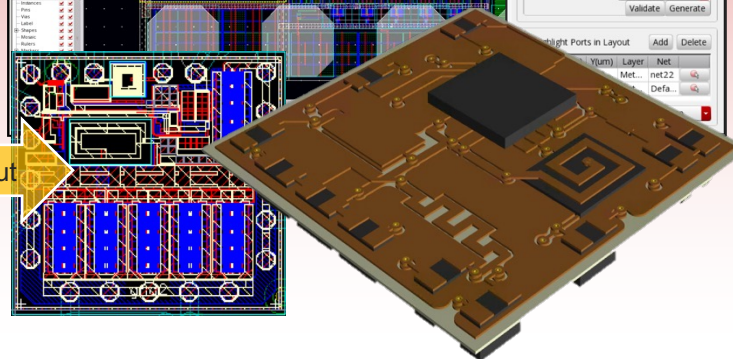
Cross-Platform Layout
Seamless cross-platform **co-design** of chips, chiplets, packages, and modules



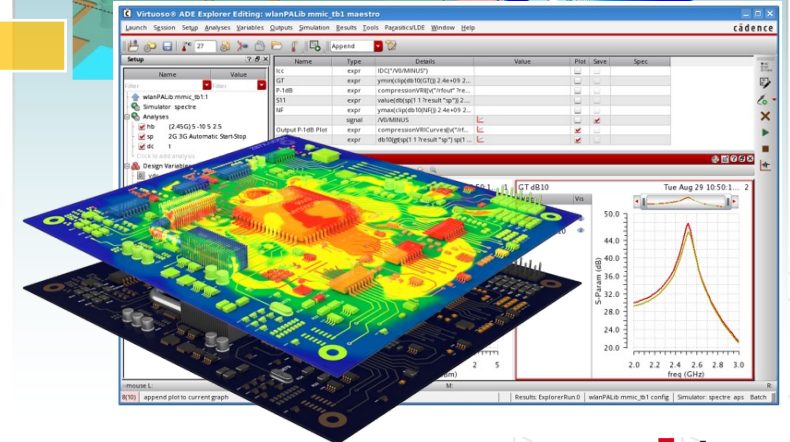
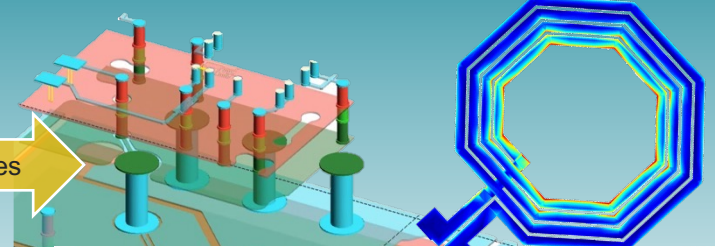
Seamless Layout/Device Parasitic Model Stitching



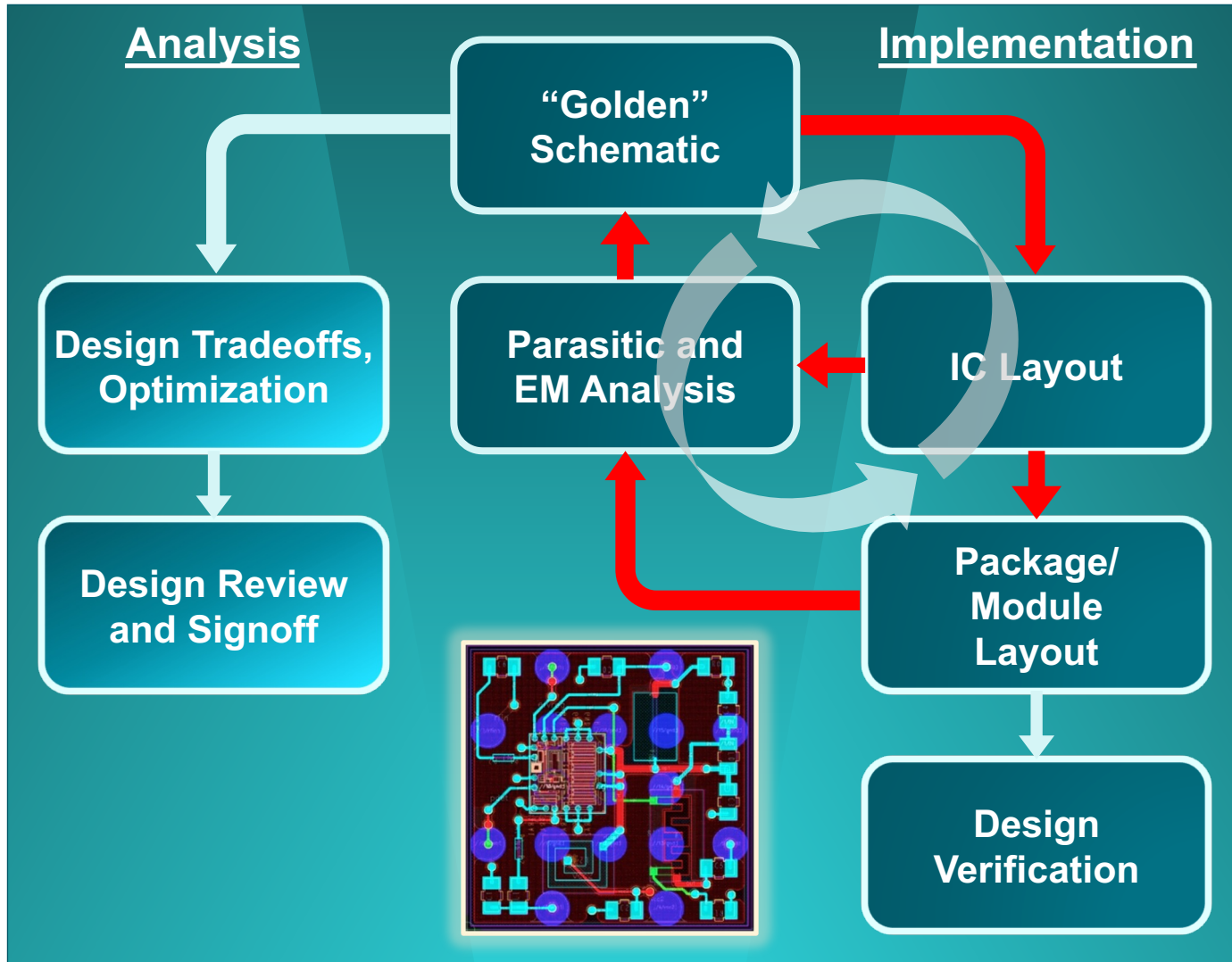
Chip(let) Layout



On-Chip/Off-Chip EM/Thermal Modeling
Seamless integration with multiple EM extraction engines with automated schematic stitching and simulation flow

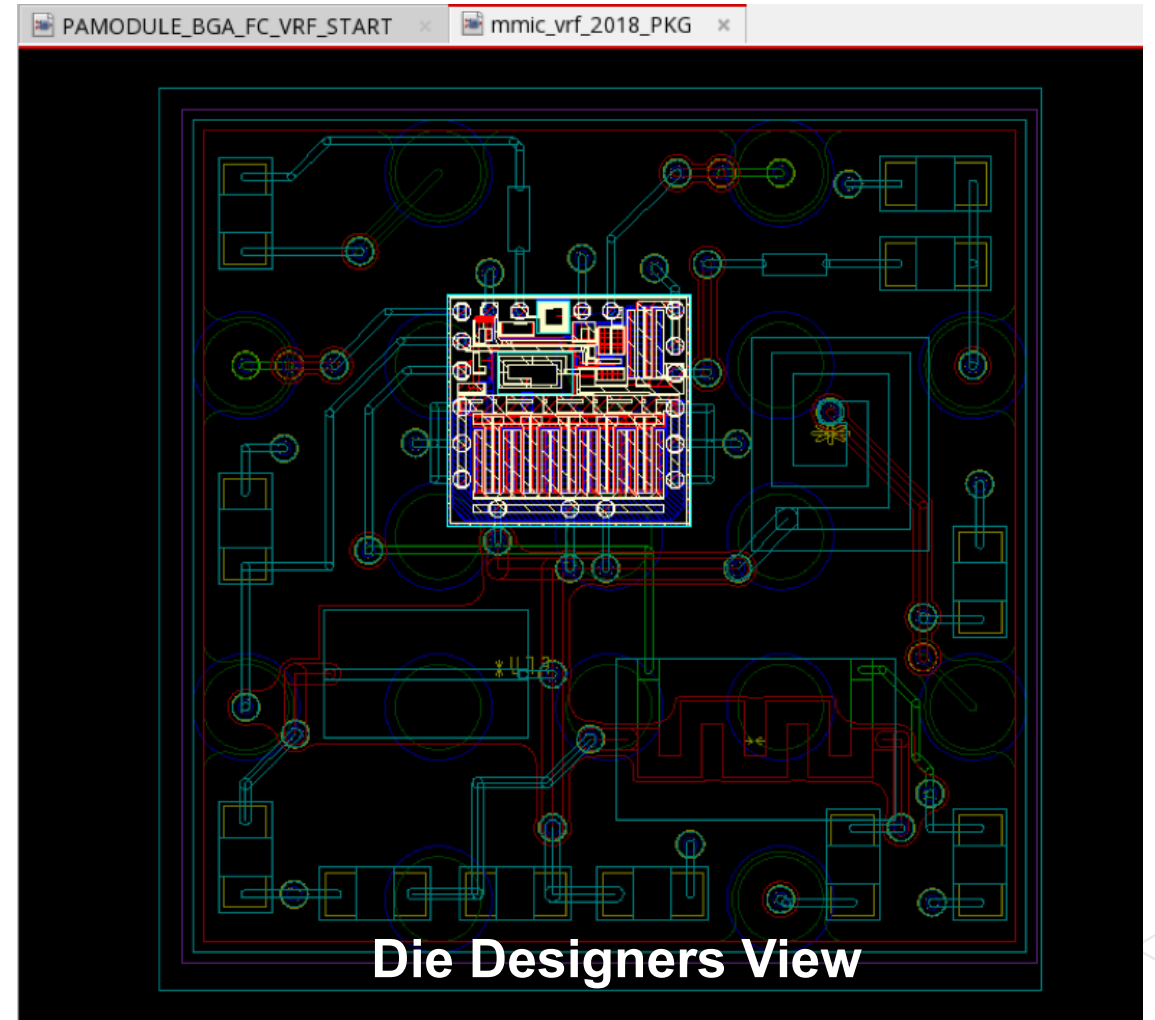
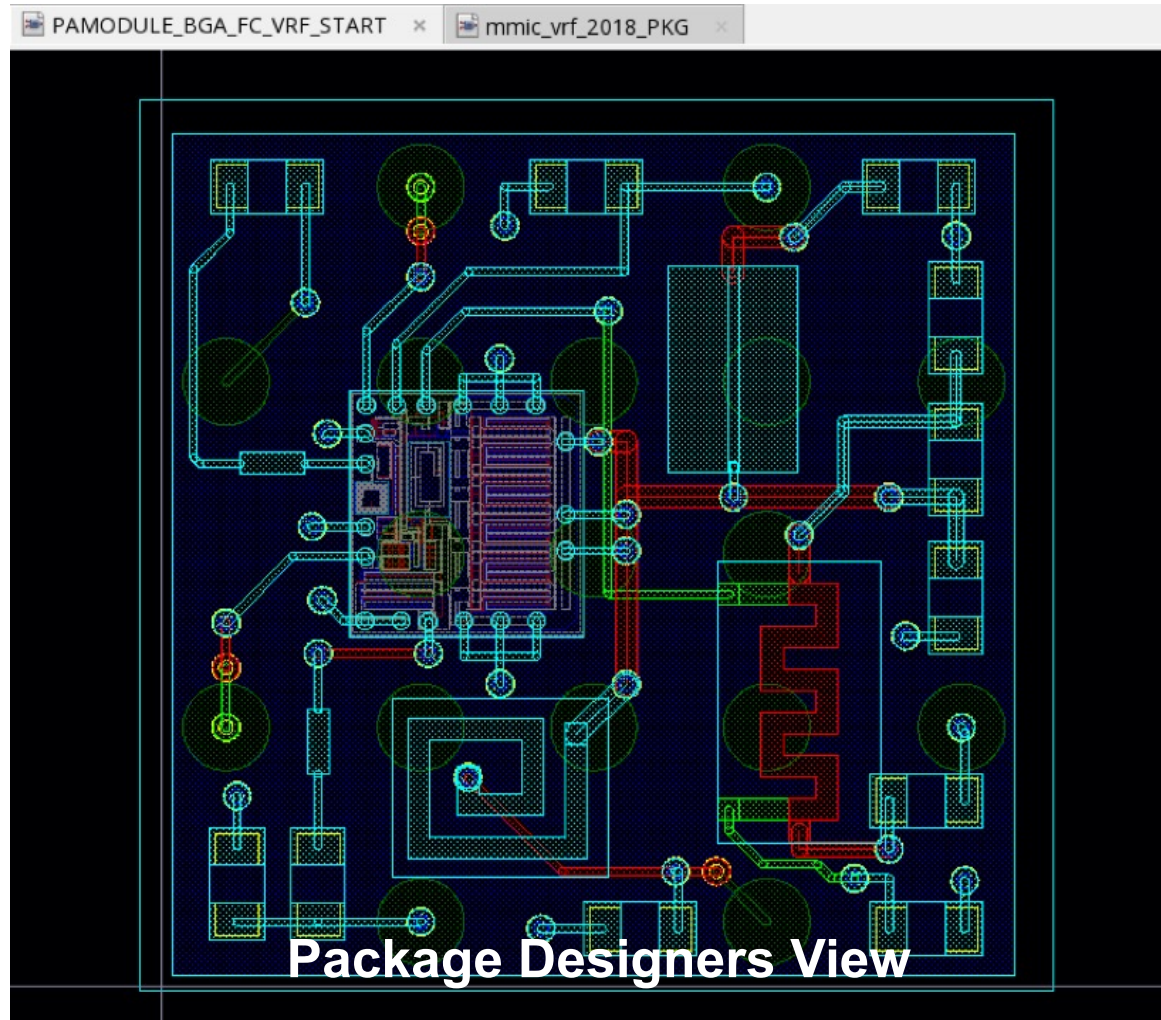


Analog/RF Co-Design and Co-Analysis Flow



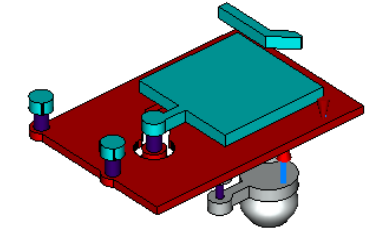
- Schematic-driven layout flow for die, chiplet, package and module design
- Merged IC and package/module layout, to enable co-design across multiple PDKs
- Smart electromagnetic and parasitic analysis, integrating multiple solver technologies
 - Geometry and mesh viewing
 - Automatic stitching of EM models into golden schematic
- Functional circuit simulation with embedded on-die and off-die layout parasitics
- Physical verification and manufacturing outputs

Designer Perspective Views for IC/Package Co-Design



System-Level Layout Parasitic Back-Annotation and Simulation

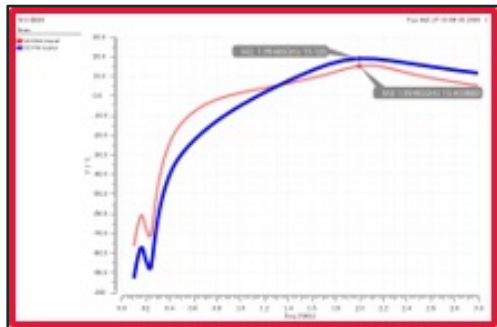
- Coupled 3D-EM extraction between chip(let), package, and PCB layout databases
 - Multiple 3D-EM engines integrated through assistant
 - Support for partial/full nets, groupings, and device-level modeling
 - Direct pin mapping and eliminates double-counting of discrete devices
 - S-parameters (freq. domain) and RLGC (time domain) models
- Automatically create schematics (extracted views) that include the layout parasitics from the package and PCB
 - Must support multi-PDK, multi-die solutions (namespace collision avoidance)



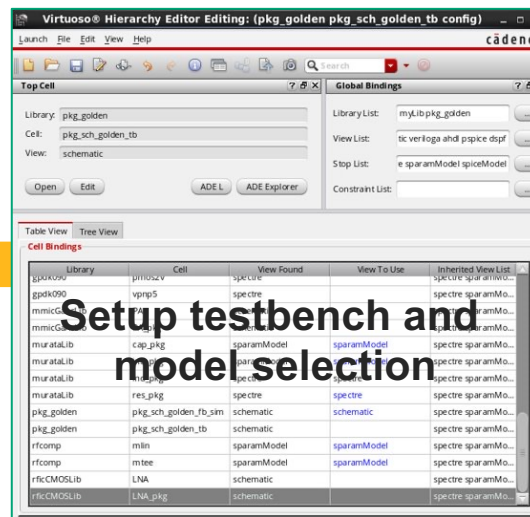
```
PowerSI Version: 16.0.0.02891.0 800
Computer Host Name: lnx-cm011

TouchstoneFormatFlag = 1
GNDNET ON
! NETS:LIST RX34_39OUT, RX34_39_IN, RX40A, RX40_3B, RX41A, RX41A_OUT, RX41B_IN, RX41B_OUT, RX7_OUT,
RX_34_39_OUT, SENSEA_FLT, TX40B, TXRF1_A, TXRF1_IN, TXRF2_IN, TXRF3_IN, TXRF3_OUT, TXRF4_IN, TXRF4_OUT,
TXRF5_IN, TX_SENSEA
! Port 1 = BP_235_FILT1-6 RX34_39OUT
! Port 2 = UL-18 RX34_39OUT
! Port 3 = LGA-01 RX41B_IN
! Port 4 = BP_235_FILT2-2 RX41B_IN
! Port 5 = BP_235_FILT2-6 RX41B_OUT
! Port 6 = UL-11 RX41B_OUT
! Port 7 = LGA-01 RX34_39_IN
! Port 8 = BP_235_FILT1-2 RX34_39_IN
! Port 9 = BP_235_FILT1-6 RX_34_36_OUT
! Port 10 = UL-13 RX_34_36_OUT
! Port 11 = BP_235_FILT2-6 RX41B_OUT
! Port 12 = UL-26 RX7_OUT
! Port 13 = LGA-14 RX40A
! Port 14 = UL-12 RX40A
! Port 15 = LGA-17 RX40_3B
! Port 16 = UL-17 RX40_3B
! Port 17 = BP3-6 TXRF5_IN
! Port 18 = UL-18 TXRF5_IN
! Port 19 = LGA-D10 TXRF4_OUT
! Port 20 = BP4-2 TXRF4_OUT
! Port 21 = BP4-6 TXRF4_IN
! Port 22 = UL-3 TXRF4_IN
! Port 23 = LGA-B10 TXRF3_OUT
! Port 24 = BP3-2 TXRF3_OUT
! Port 25 = BP3-6 TXRF3_IN
! Port 26 = UL-4 TXRF3_IN
```

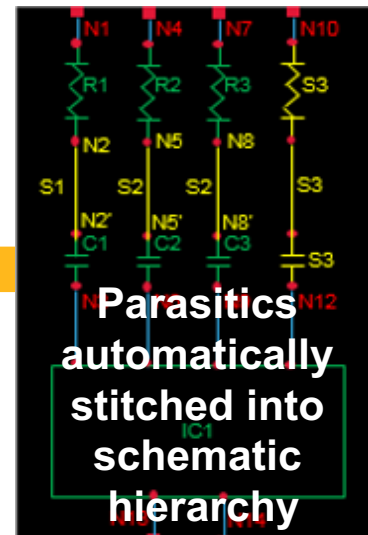
S-Parameter Model



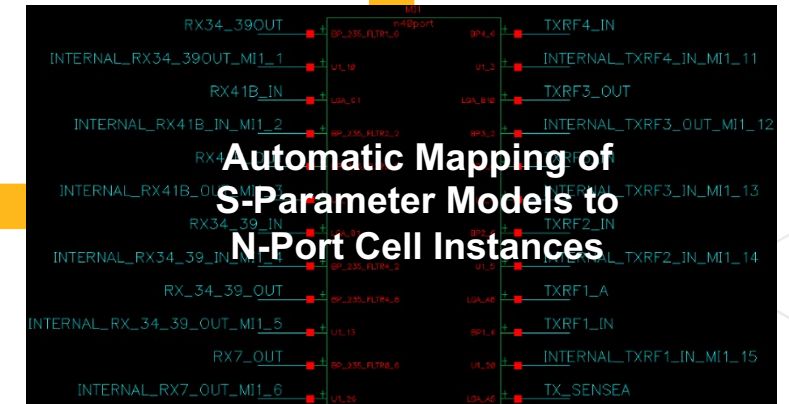
Simulate



Setup testbench and model selection

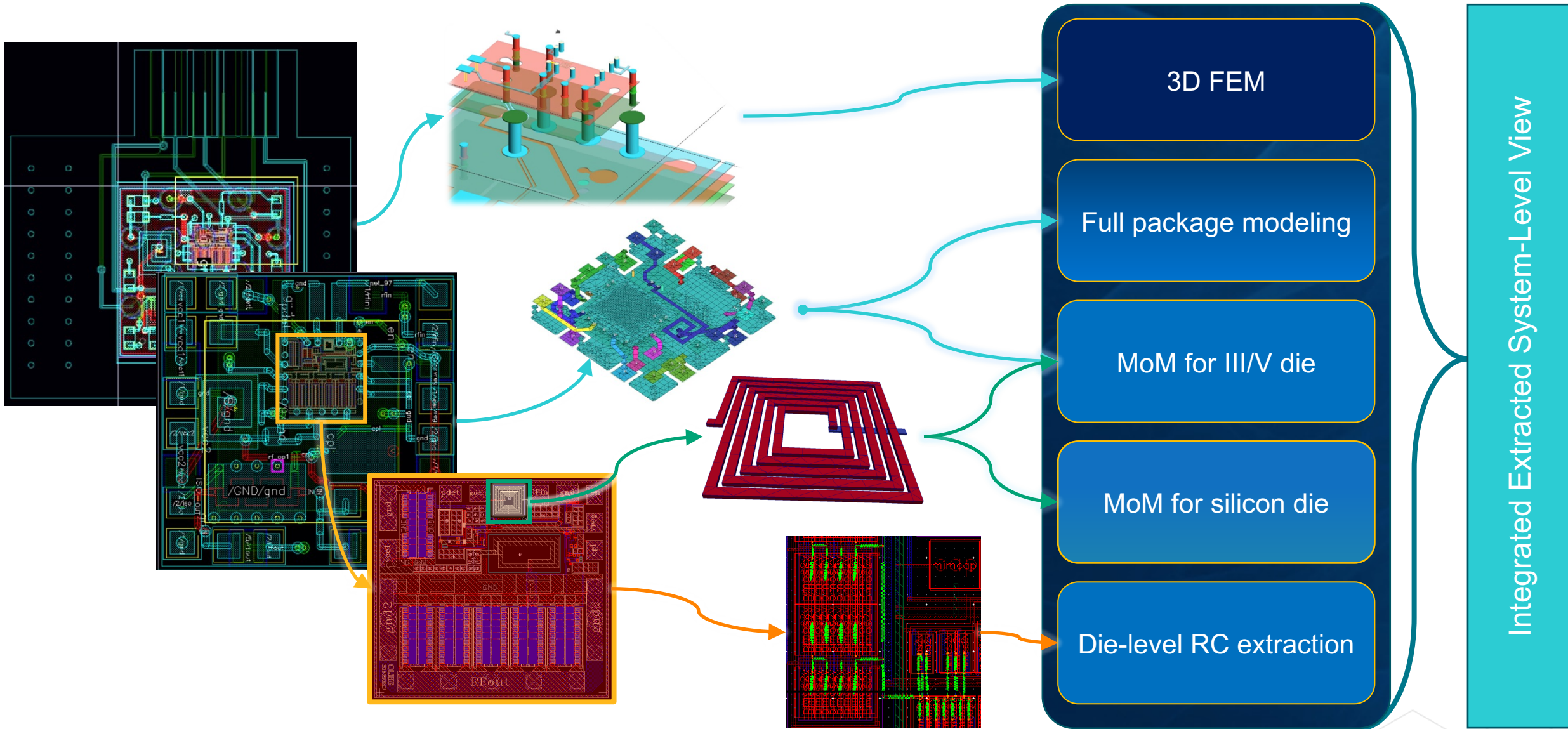


Parasitics automatically stitched into schematic hierarchy

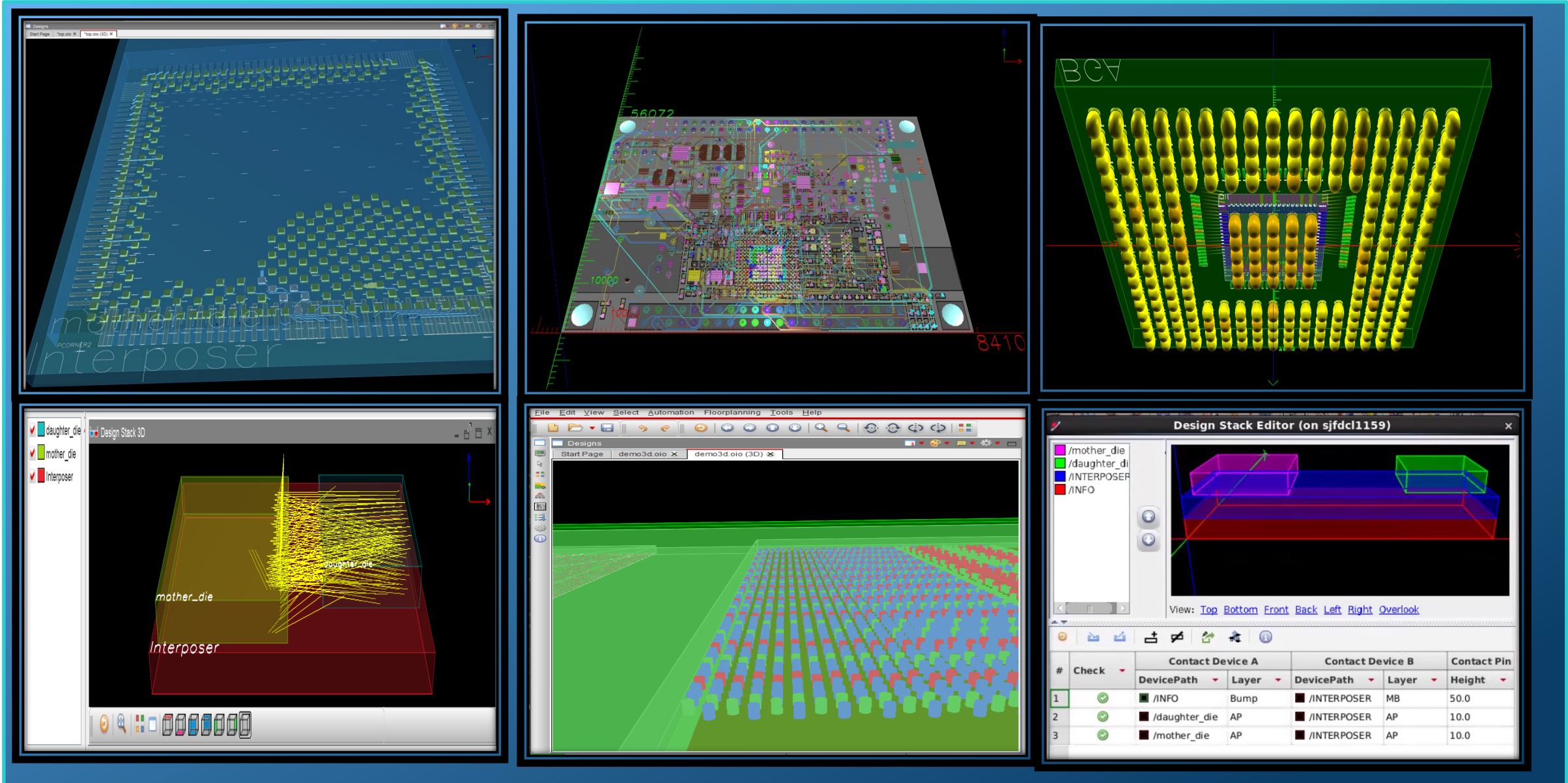


Automatic Mapping of S-Parameter Models to N-Port Cell Instances

Specialized EM modeling



3D Viewing Capabilities for 3DHI



Conclusion

- 1 The age of Moore-than-Moore has arrived, and packaging is a huge beneficiary
- 2 There are still many challenges to overcome to bring 3D heterogeneous integration to the mainstream
- 3 The worlds of IC designers and package designers are converging
- 4 IC/package co-design and analysis is imperative
- 5 There are EDA solutions today that enable co-design/co-analysis



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