Enabling Co-Design of 3D Heterogeneous Packages

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Outline

- Trends
- Challenges
- Solutions
- Conclusion

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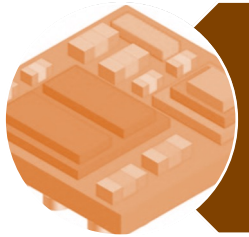
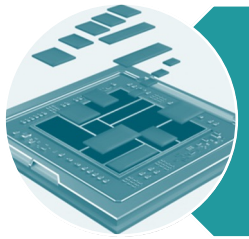
The Beginning of the “More Than Moore” Era

For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing…The economics of semiconductor logic scaling are gone…

Gordon Moore knew this day would come. He also predicted that *”It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”*



Providing a possible alternative to advanced monolithic SoCs, multi-chiplet SiPs have become a very attractive option for cost-sensitive complex designs



The generation of “More Than Moore” is here…

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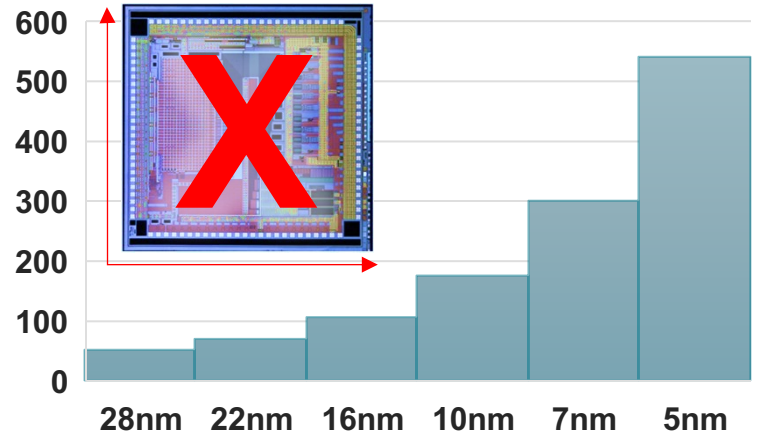
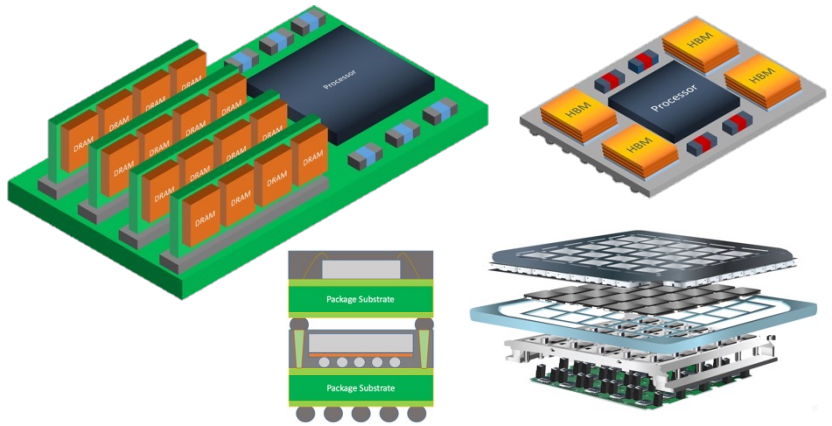
Simply Following Moore's Law Alone is No Longer the Best Technical and Economical Path Forward

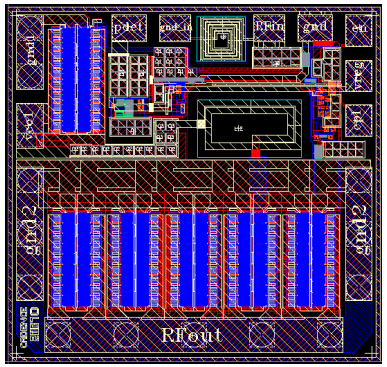
Cost & Yield & Size

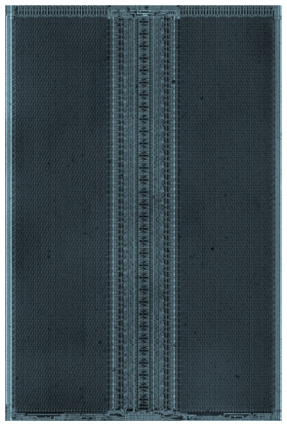


Lower Memory Wall

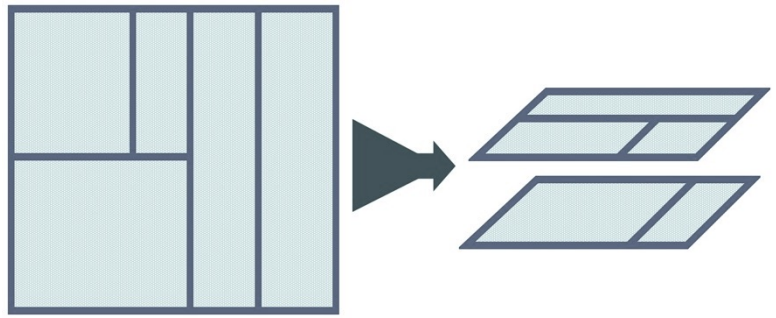


Analog/RF, I/O & Memory





Form-Factor & Modularization



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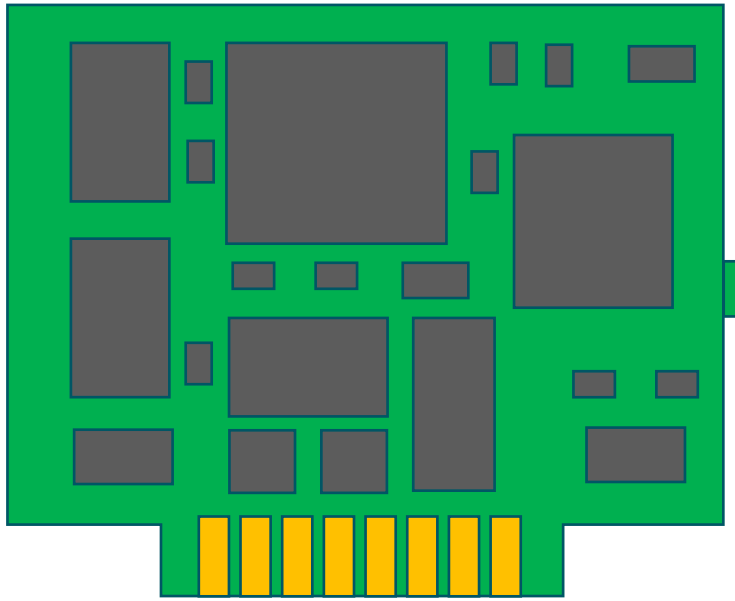
SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures

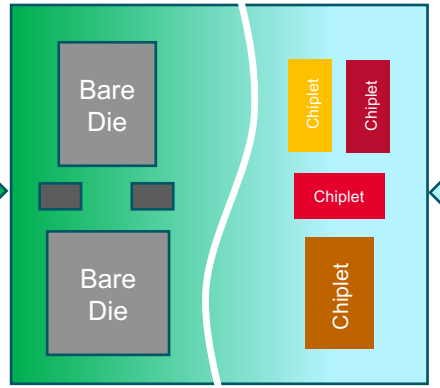
The transition from system on a chip (SoC) to system in a package (SiP)

PCB → Board size/complexity reduction (SWaP) → **Multi-Chip(let) Packaging (Including stacking)** ← Disaggregated SoC ← **SoC/ASIC**



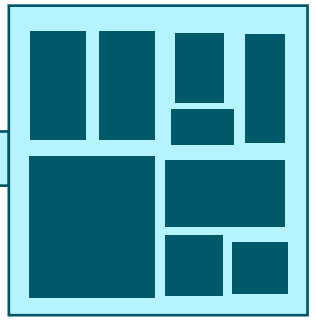
MCM/SiP

Unpackaged die



Heterogeneous Integration

Chiplets



PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

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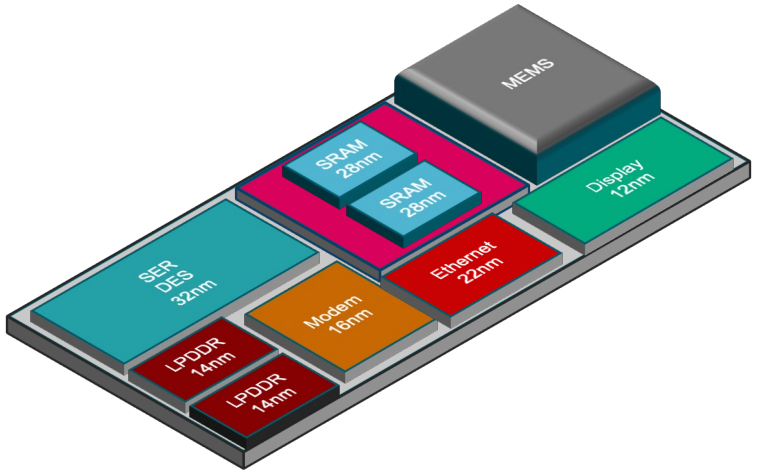
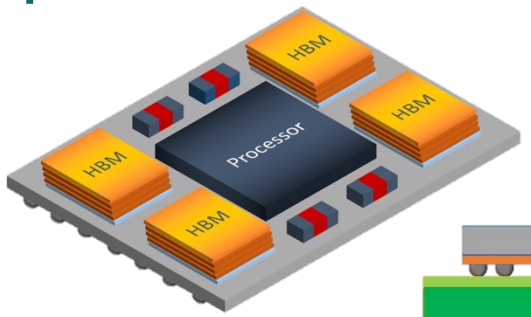
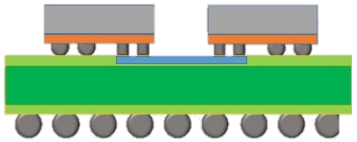
Heterogenous Integration Leverages Multiple Packaging Technologies



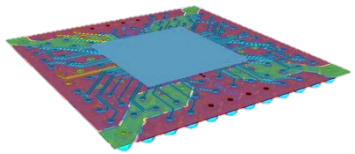
Heterogeneous Integration



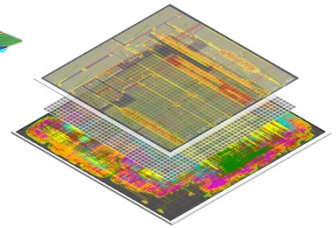
2.5D-IC (Silicon Interposer) — 2010



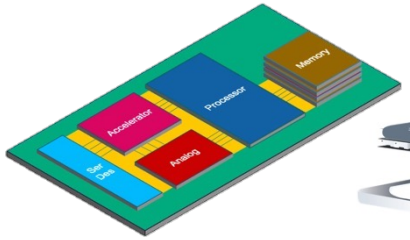
Interconnect Bridges — 2012



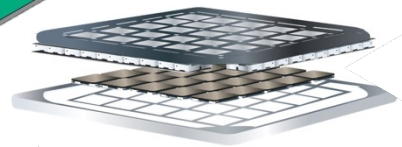
Ultra-High-Density RDL (FOWLP) — 2015



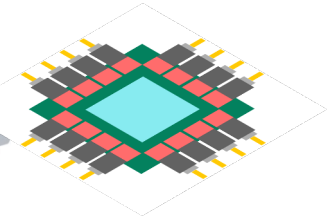
Silicon Stacking — 2018



RDL Interposer — 2020



3D System-on-a-Wafer



Co-Packaged Optics — 2022

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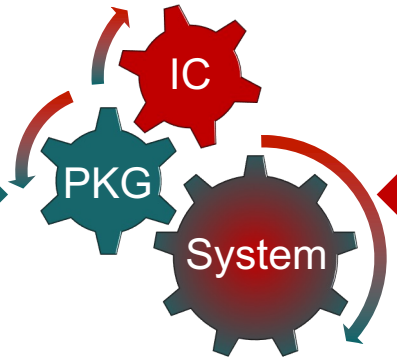
The Needs of IC and Systems Designers are Converging

OSATs (SWaP)

Board design impact on packaging

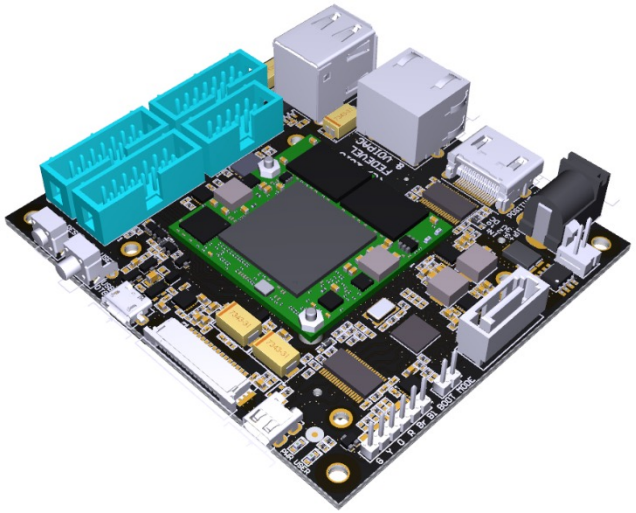
1980-2010



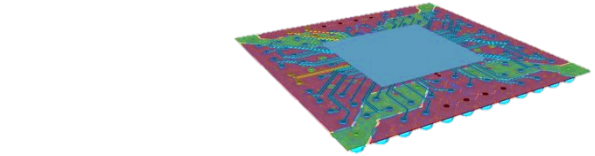
Foundries (PPA)

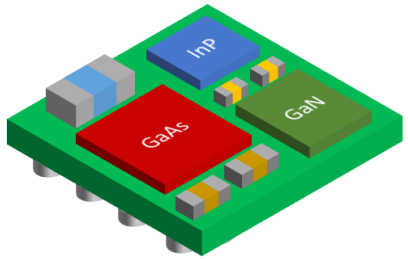
IC design impact on packaging

2011-Now

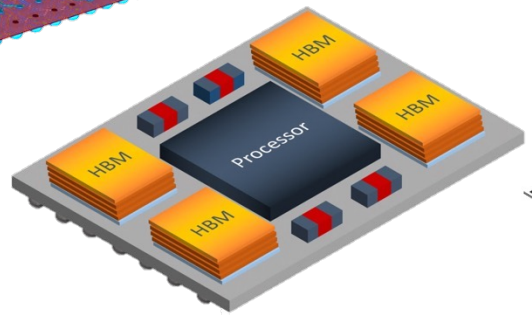


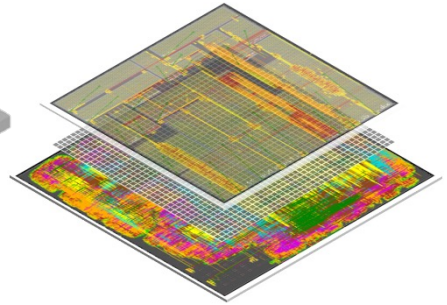
PCB Layout Flow
System-Level Analysis



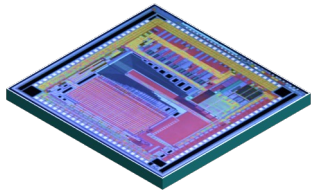


PCB-like Flow
System-Level Analysis





IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis



IC Flow
IC signoff Methodology

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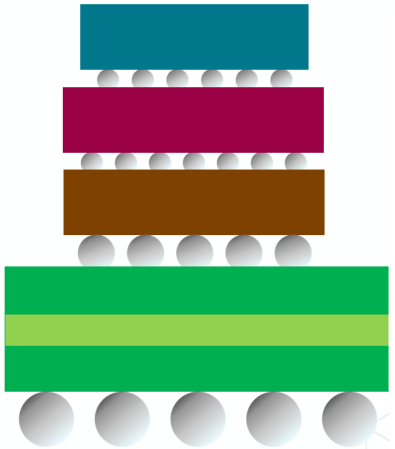
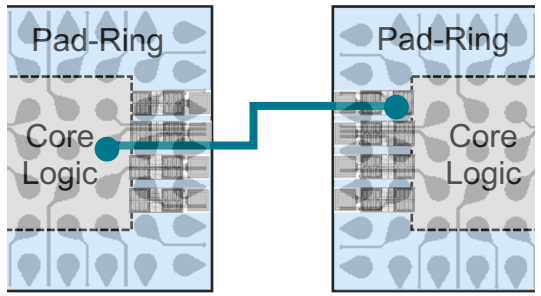
3D Packaging Versus Silicon Stacking (3DHI)

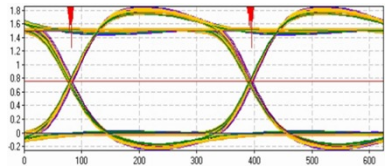
3D Packaging

- Solder-based connections (>25um)
- Each die designed independently
  - Black-box abstracts used for layout
- I/O buffer to I/O buffer signaling



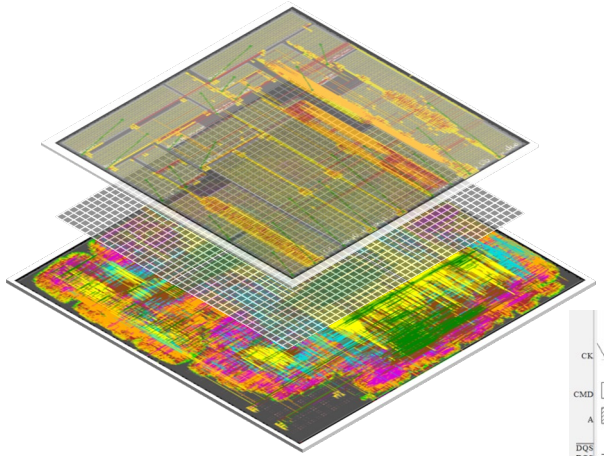


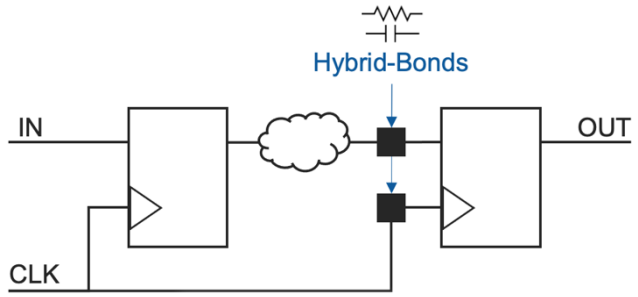
I/O buffer to I/O buffer
(AIB, OpenHBI, BoW, UCIe, etc)



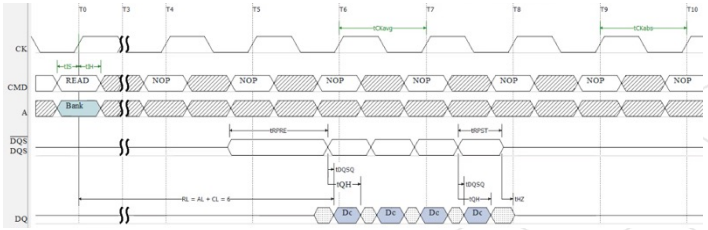
Silicon Stacking

- Solder-free connections (<10um)
- Single RTL partitioned at implementation
  - Full detail of IC required for layout
- DBI, hybrid-bond, cu-to-cu, direct connection





Interconnect through
hybrid bond



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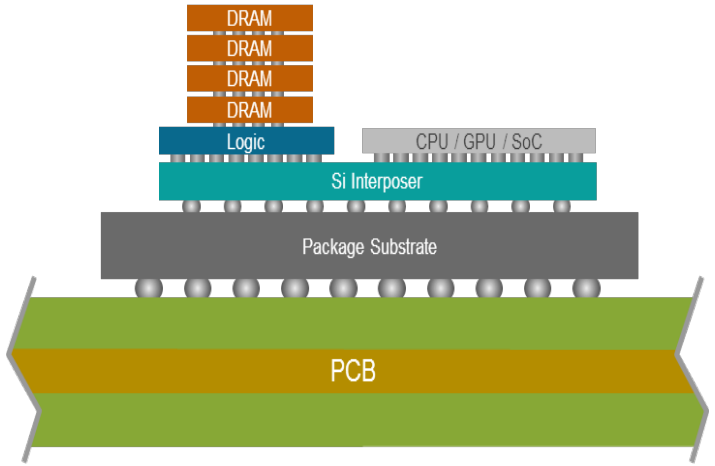
Times Have Changed…

- Yesterdays Advanced IC Packaging
  - *Necessary evil*
  - Avoid negative impact on chip
    - Electrical, Thermal
  - Protect chip from the outside world
  - Redistribute IO to pitch more suitable for the PCB layout



- Todays advanced IC packaging is about *adding value* to end products
  - Multi-chip(let) solutions leading the way for “More than Moore” vision
  - Companies leveraging packaging technologies to create value and differentiation from their competitors
  - TSV, WLP and 3D stacking technologies providing a tremendous number of packaging options for all form-factors and budgets

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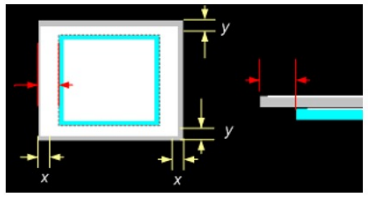
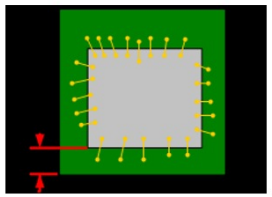
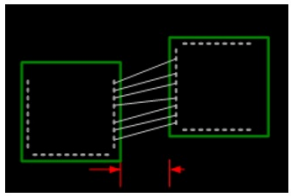
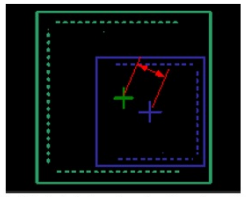
Multi-Chiplet 3D Diverse Ecosystem Challenges

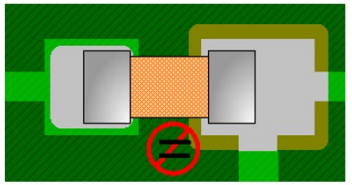


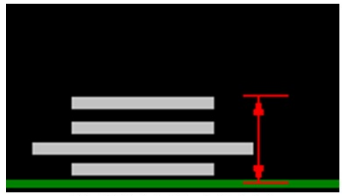
Die/Chiplet Overhang

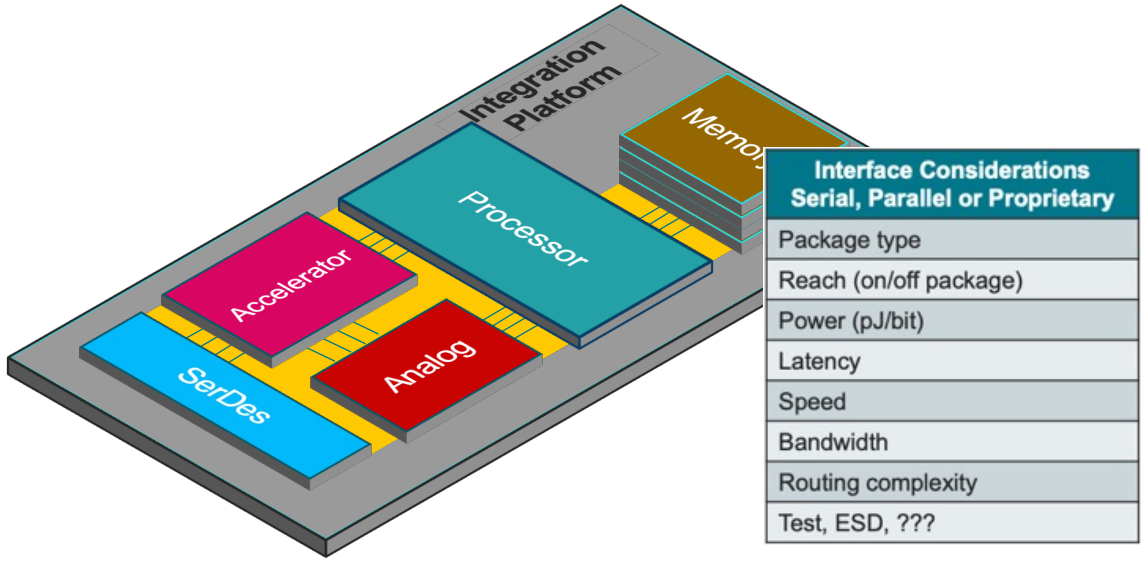

Die/Chiplet Spacing to Substrate Edge


Die/Chiplet to Die/Chiplet Spacing


Die/Chiplet Center to Center Offset


Tombstone Effect (% size diff)


Die/Chiplet Stack Height



Assembly Design Kits

- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
- Foundries need to provide the packaging engineer all the data he/she needs to produce manufacturing output of a design that can be assembled and tested
- Contents; tech files, libraries, assembly rules, substrate DFM, rule decks, and design templates
- Security and Test solutions

COTS Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
  - CHIPLET.US
- Progress with chiplet exchange formats
  - CDX, 3Dblox™
- Common communication interface
  - AIB, UCIe, BoW, …
  - Too many packaging options to standardize on a single interface

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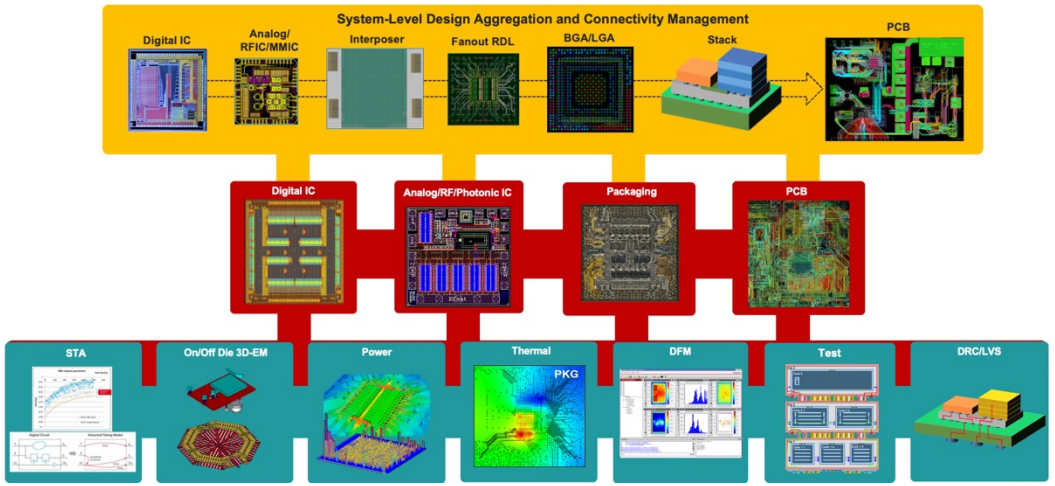
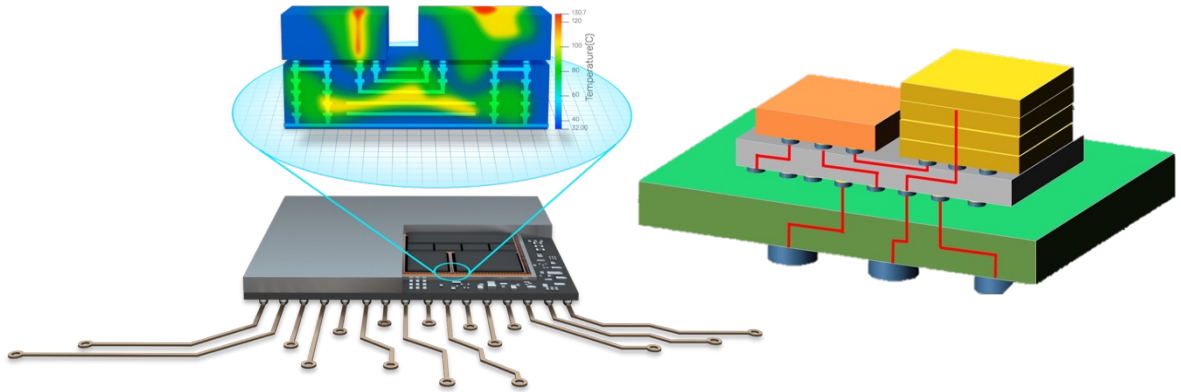
Multi-Chiplet 3D Flow Challenges





Design Tools/Flows

- Explosion in the number of design tools and required expertise mean complex design flows
- **Co-design/co-analysis across die/chiplet/package is now mandatory**
- Capacity and performance impact on tools
- Support of existing and emerging 3D-IC standards
- Silicon stacking breaks abstract die representation use model
- Package designers pivoting to foundry-based design and sign-off requirements

Analysis and Sign-Off

- Early-stage and signoff-level thermal/power analysis
- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Stacked-die EMIR
- Stress and CMP planarity checks
- New 3D-IC test standards
- High-capacity EM/SI/PI to support very large structures (billions of instances)
- Compliance kits for new chiplet-to-chiplet communication standards

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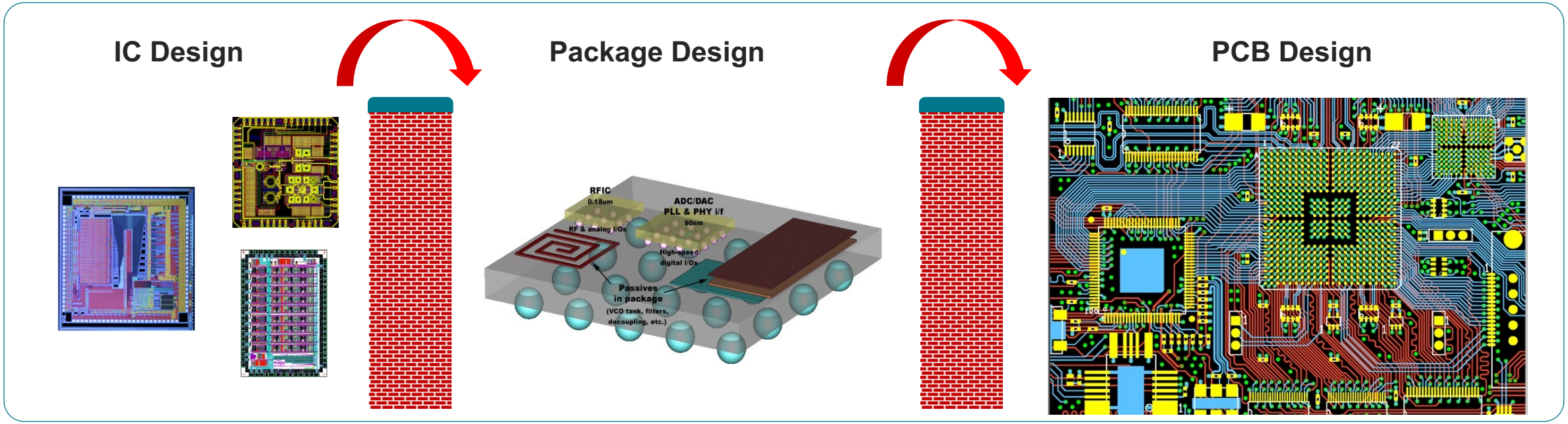
Over-the-Wall Approach Fails For Analog/RF 3D HI Packaging

- Separate logic/design capture means no system-level LVS (SystemLVS) and redundant schematic/libraries.
  - Many manual steps between domains
- IC designers use estimated package and PCB layout parasitics, leading to unexpected performance limitations



- Traditional design methodologies are breaking down

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Why Can’t We Have One Layout Tool For Everything?

- Each platform has inherent advantages and disadvantages
- Capacity should be considered
- Two or more platforms often required to create optimal design
- Cross-platform solutions improve domain to domain data exchange/ co-design

	Package/PCB	Analog/RF IC	Digital IC
Architecture	GUI-centric layout	Schematic capture, hierarchical layout	Language-driven flat design
Package Type	BGA/LGA, FOWLP, PoP, Si bridges	RF module, Photonics	2.5D-IC, 3D-IC
Die Model	Blackbox abstract	Transistor level	Standard Cell level
Routing Styles	Constraint-driven, push/shove 45-degree routing	PDK-driven, 90/45 degree/CurvyCore™ routing	Timing-driven routing, 45-degree RDL routing
Capacity/Perf	100,000s	1,000,000s	1,000,000,000s
Extraction/ Analysis	3D-EM, SI and PI	RC Extraction + 3D-EM	RC Extraction
Manufacturing Outputs	Board/Substrate Foundry	Foundry	Foundry
Physical Verification	Only required in some applications	Sign-Off DRC and LVS	
OS	Windows, Linux	Linux	Linux

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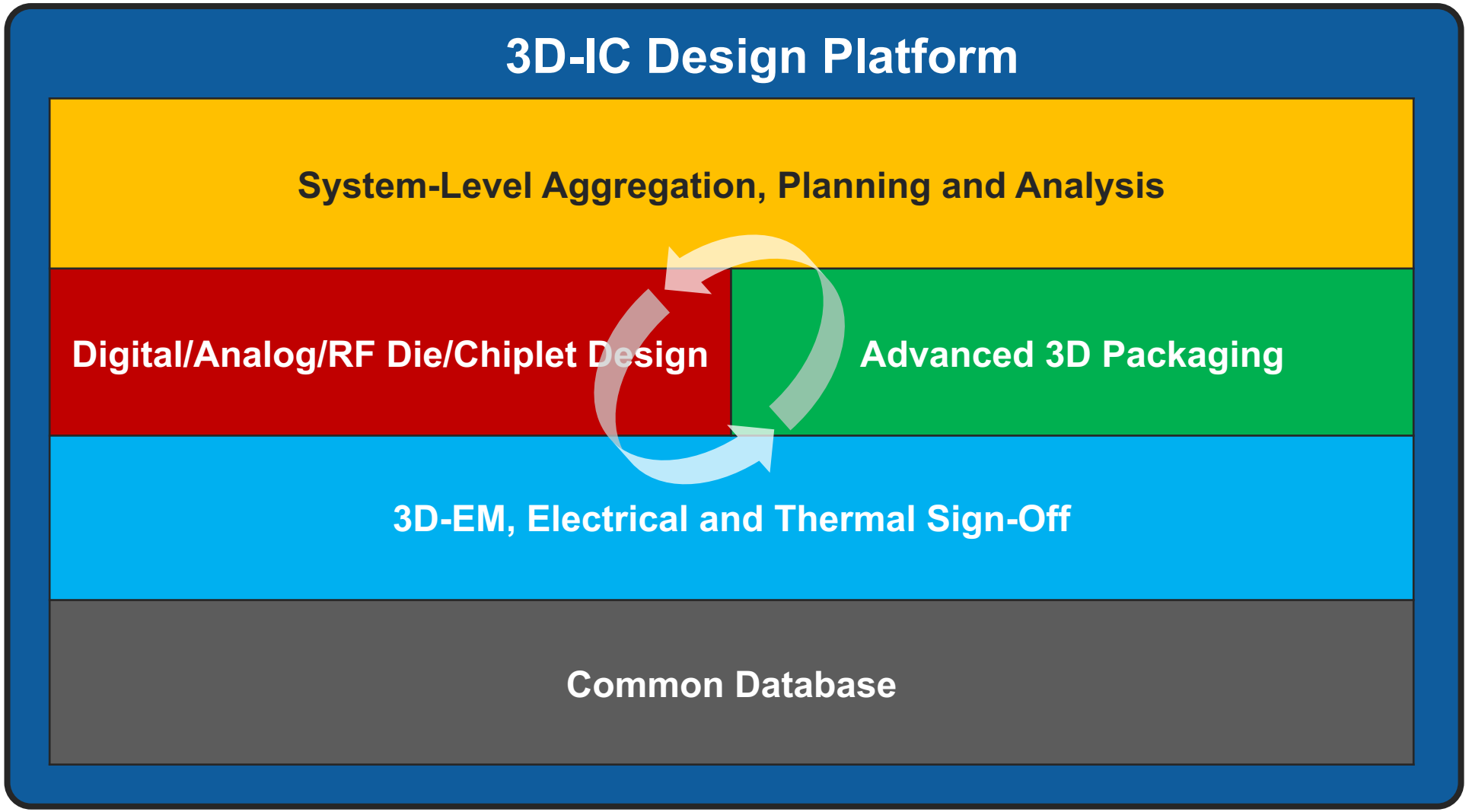
High-Level Co-Design Flow



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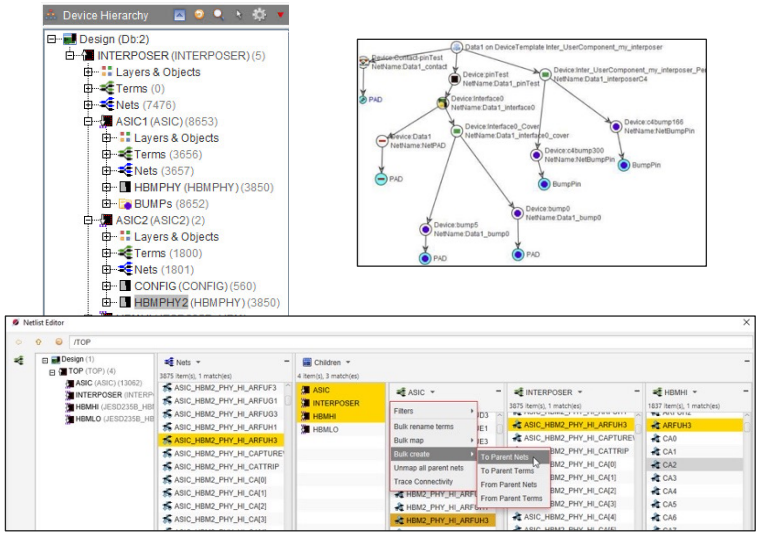
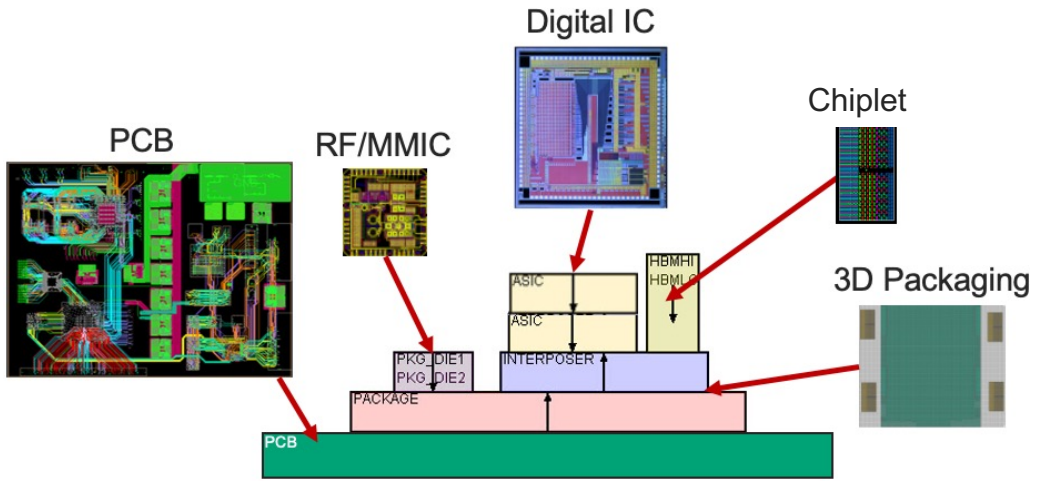
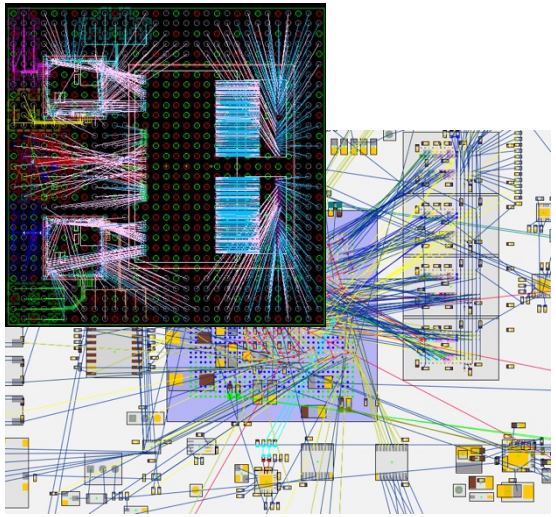
Digital-Centric Top-Level Aggregation, Co-Design and Optimization



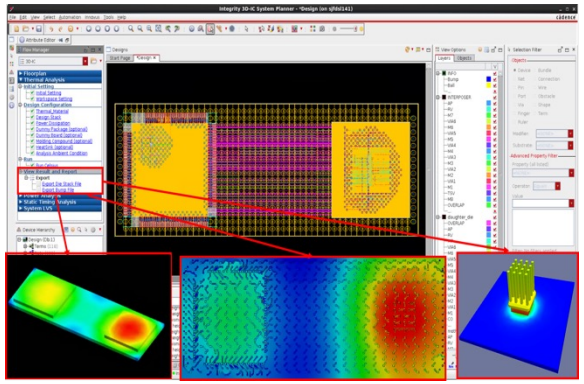
Multi-design management with chip(let)-chip(let)-package-board signal-mapping



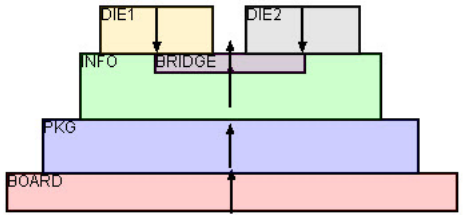
Hierarchical Planning and Optimization of System-Level Design and Connectivity



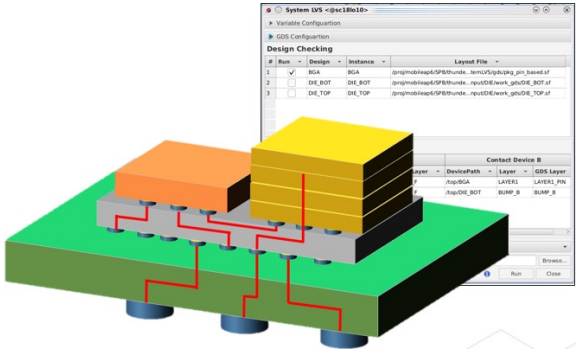
System-level co-optimization



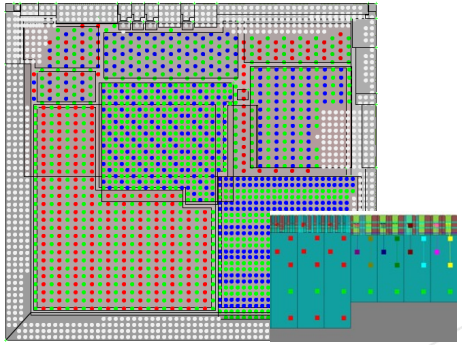
Early-Stage Thermal/Power Analysis



Stack management (Supports 3Dblox™)



System-level connectivity/stack alignment verification (SystemLVS)



Advanced bump/TSV planning

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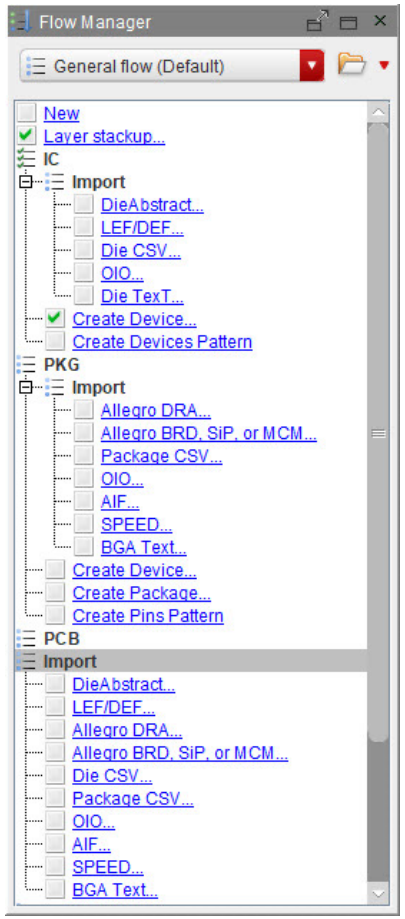
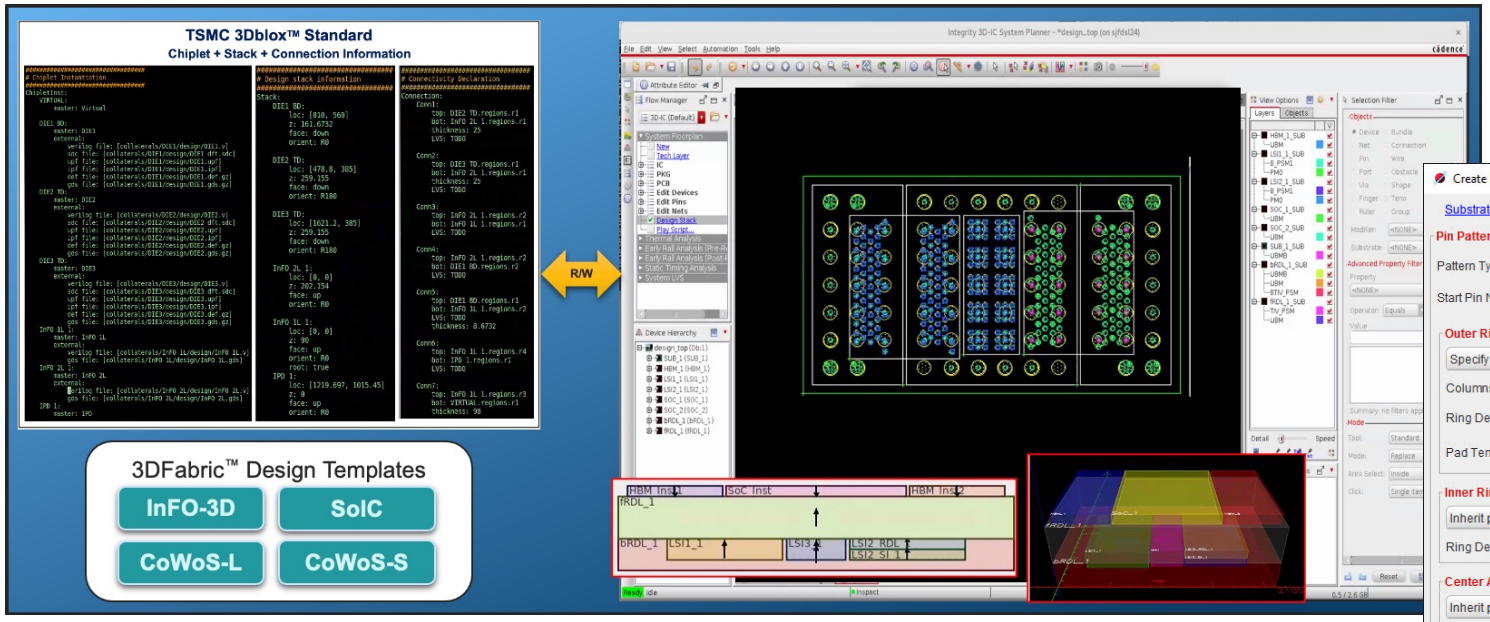
Flexibility Importing Design Data Into Co-Design Platform

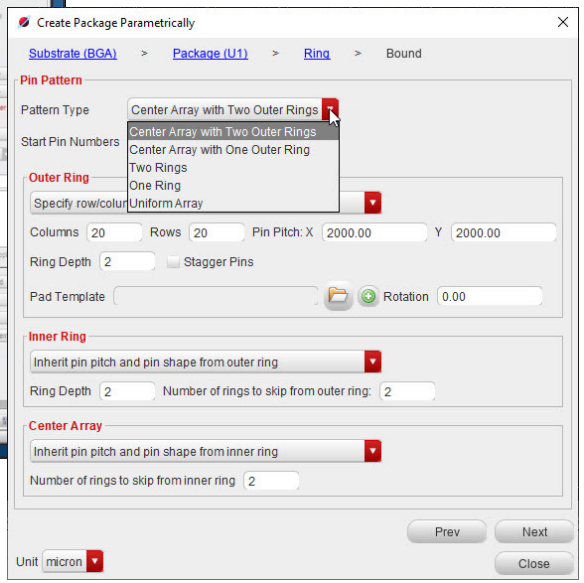


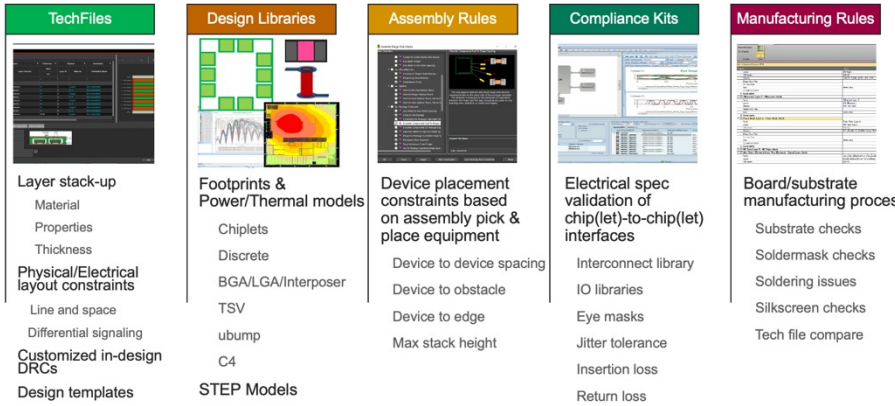
Industry Standard Formats



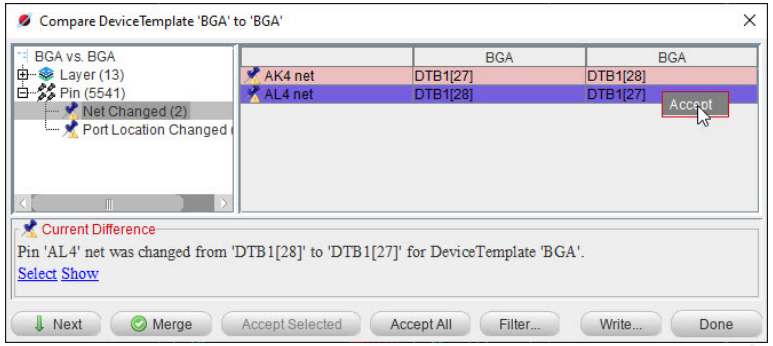
TSMC 3Dblox™

Build On-The-Fly





Assembly Design Kits (ADK)



ECO Flow With Layout Tools

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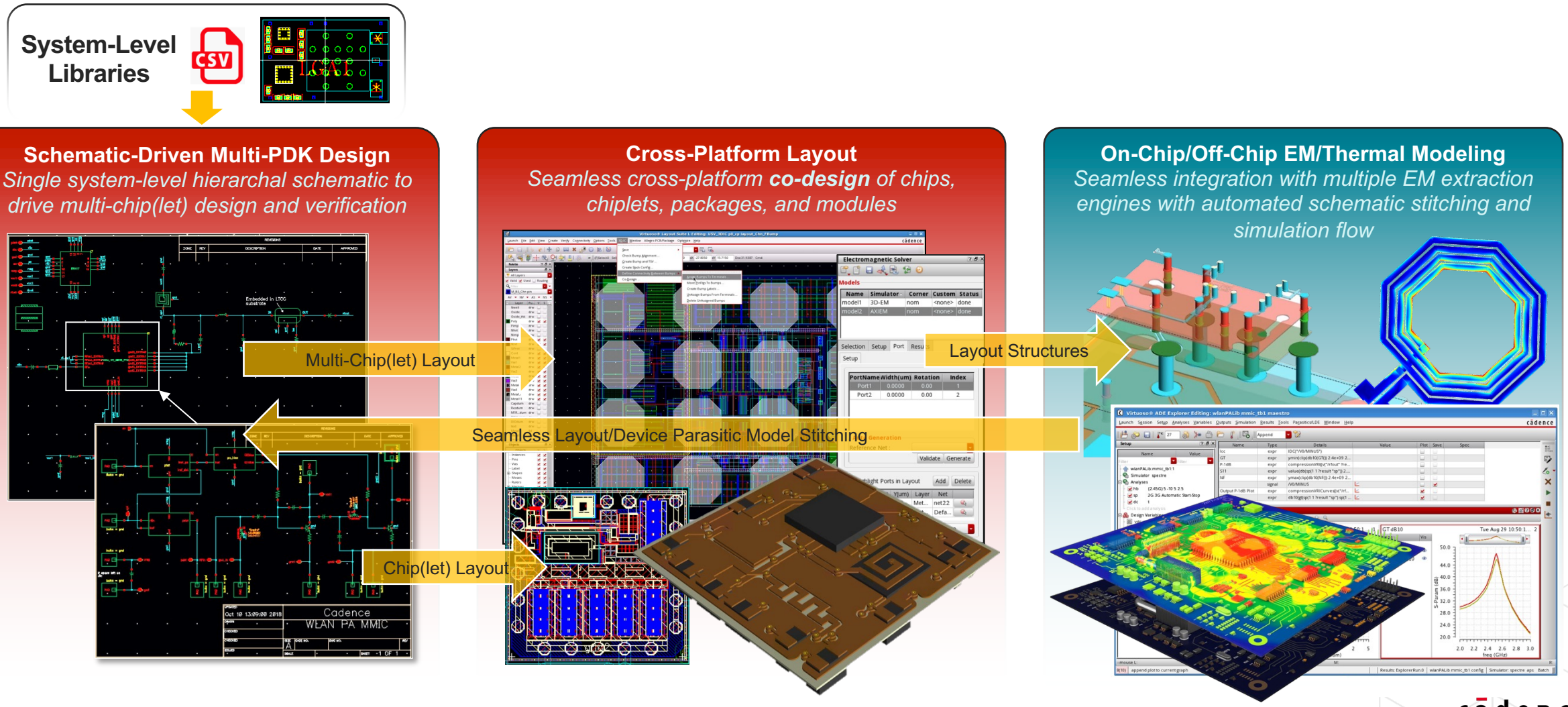
Schematic Driven (Analog/RF) Co-Design/Analysis Flow

- Chip(let)/package (multi-PDK) co-design/analysis solution built on IC design platform



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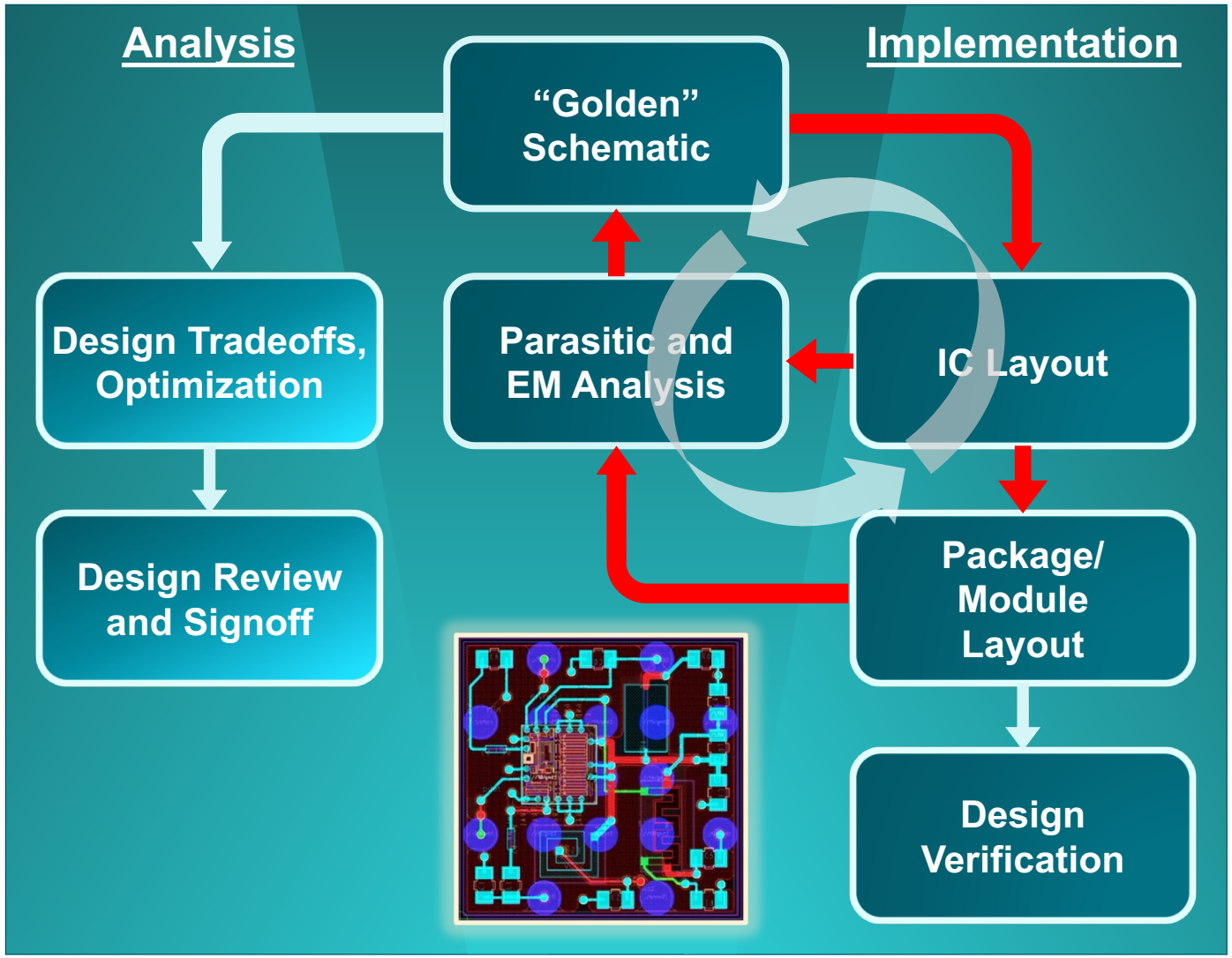
Analog/RF Co-Design and Co-Analysis Flow



- Schematic-driven layout flow for die, chiplet, package and module design
- Merged IC and package/module layout, to enable co-design across multiple PDKs
- Smart electromagnetic and parasitic analysis, integrating multiple solver technologies
  - Geometry and mesh viewing
  - Automatic stitching of EM models into golden schematic
- Functional circuit simulation with embedded on-die and off-die layout parasitics
- Physical verification and manufacturing outputs

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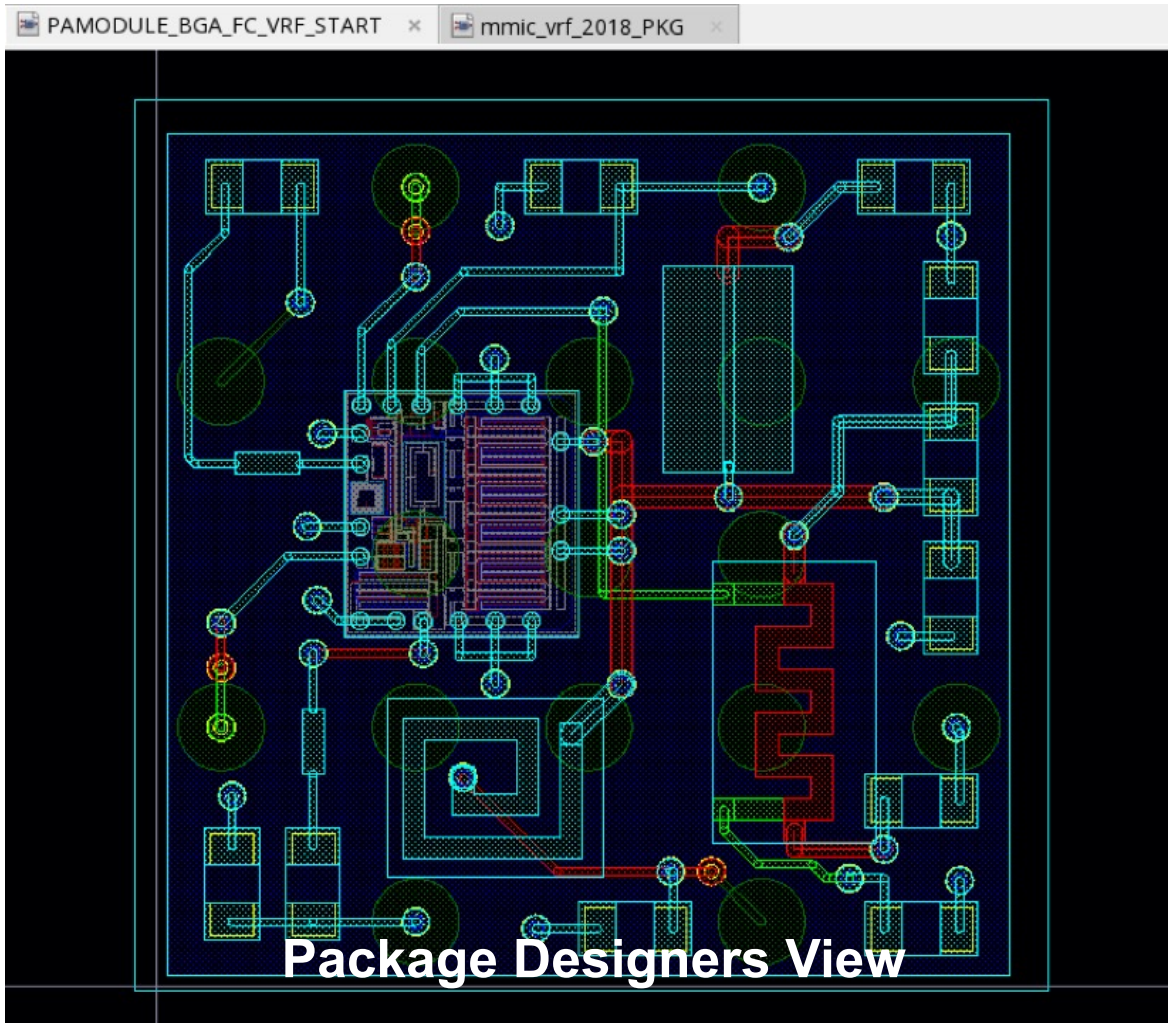
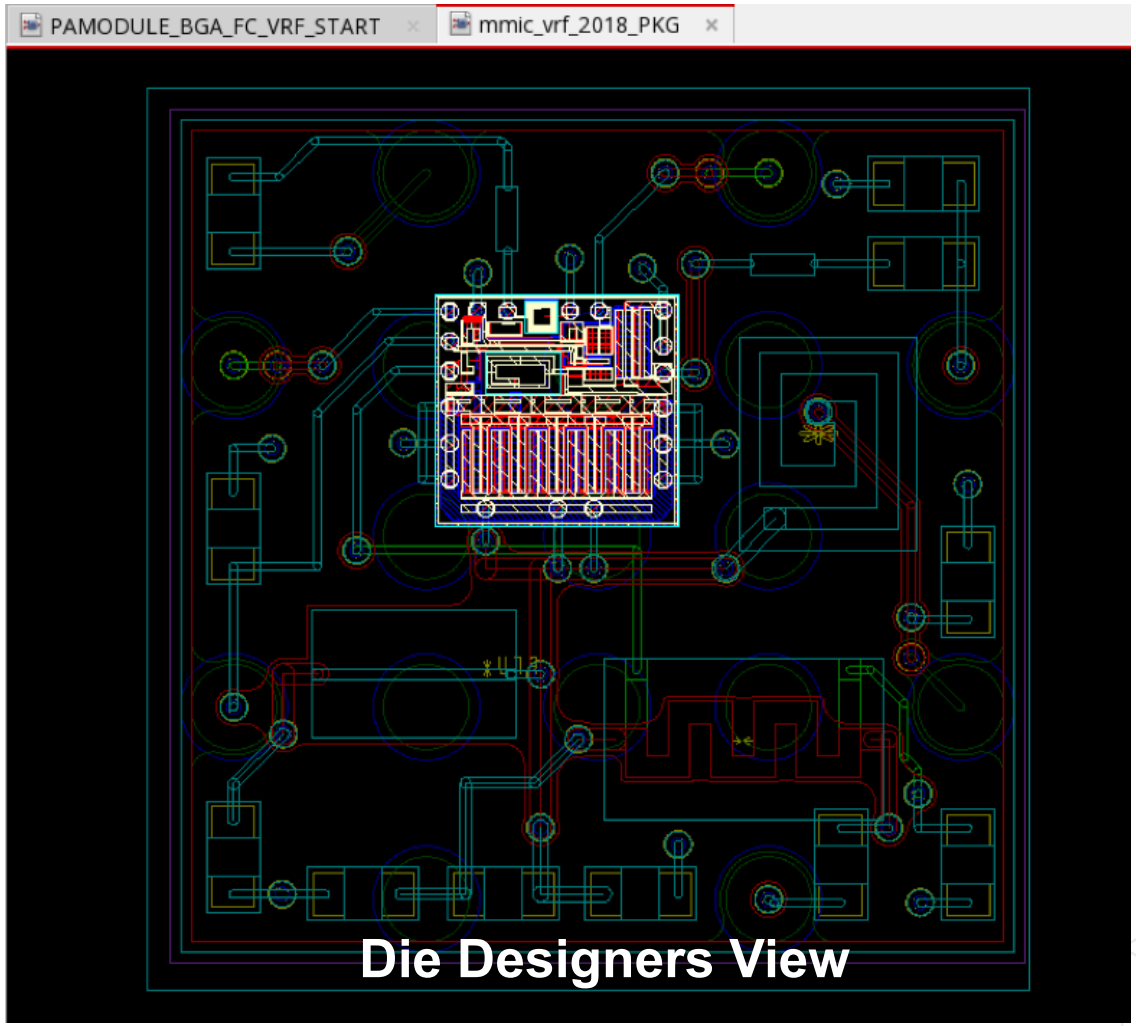
Designer Perspective Views for IC/Package Co-Design





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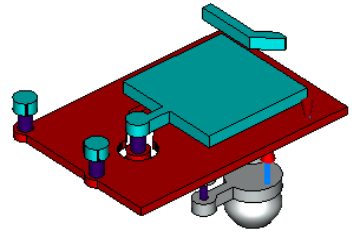
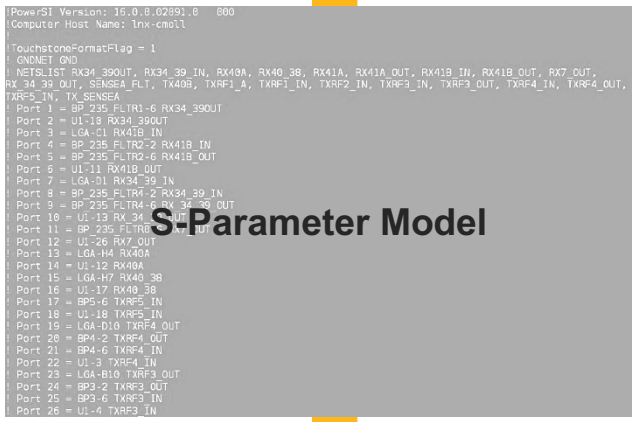
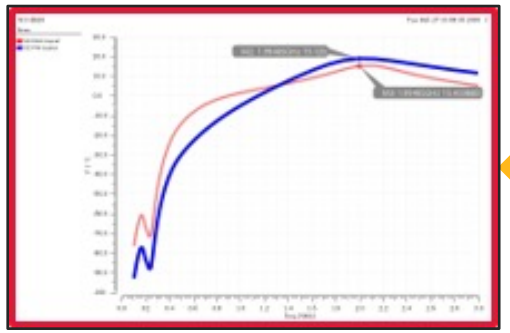
System-Level Layout Parasitic Back-Annotation and Simulation

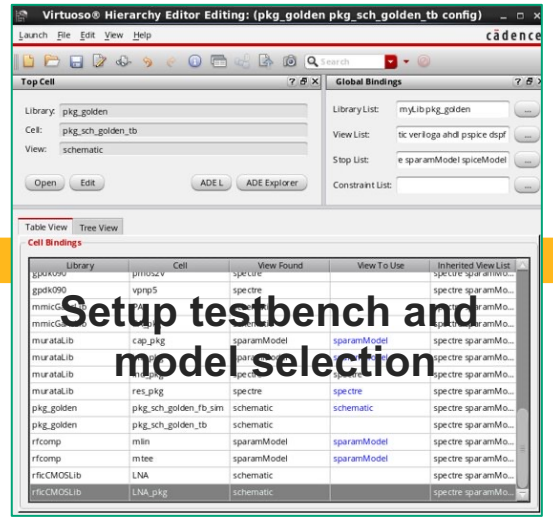
- Coupled 3D-EM extraction between chip(let), package, and PCB layout databases
  - Multiple 3D-EM engines integrated through assistant
  - Support for partial/full nets, groupings, and device-level modeling
  - Direct pin mapping and eliminates double-counting of discrete devices
  - S-parameters (freq. domain) and RLGC (time domain) models
- Automatically create schematics (extracted views) that include the layout parasitics from the package and PCB
  - Must support multi-PDK, multi-die solutions (namespace collision avoidance)



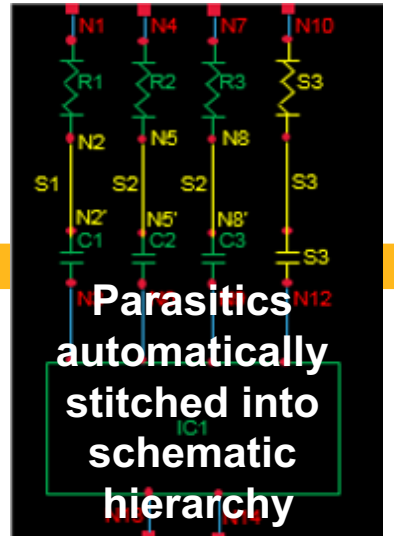


S-Parameter Model

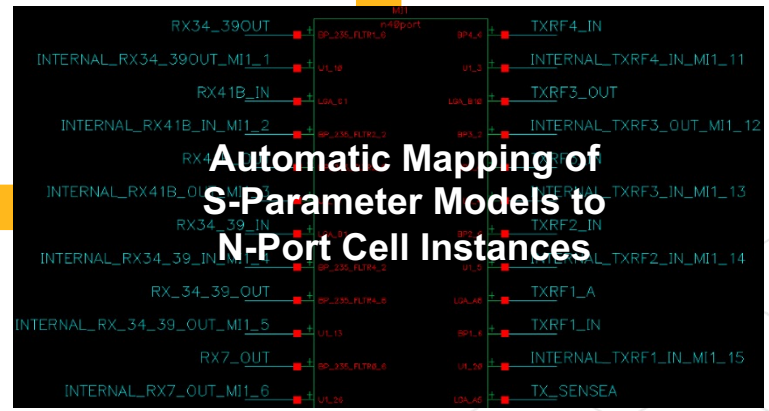

Simulate



Setup testbench and model selection



Parasitics automatically stitched into schematic hierarchy



Automatic Mapping of S-Parameter Models to N-Port Cell Instances

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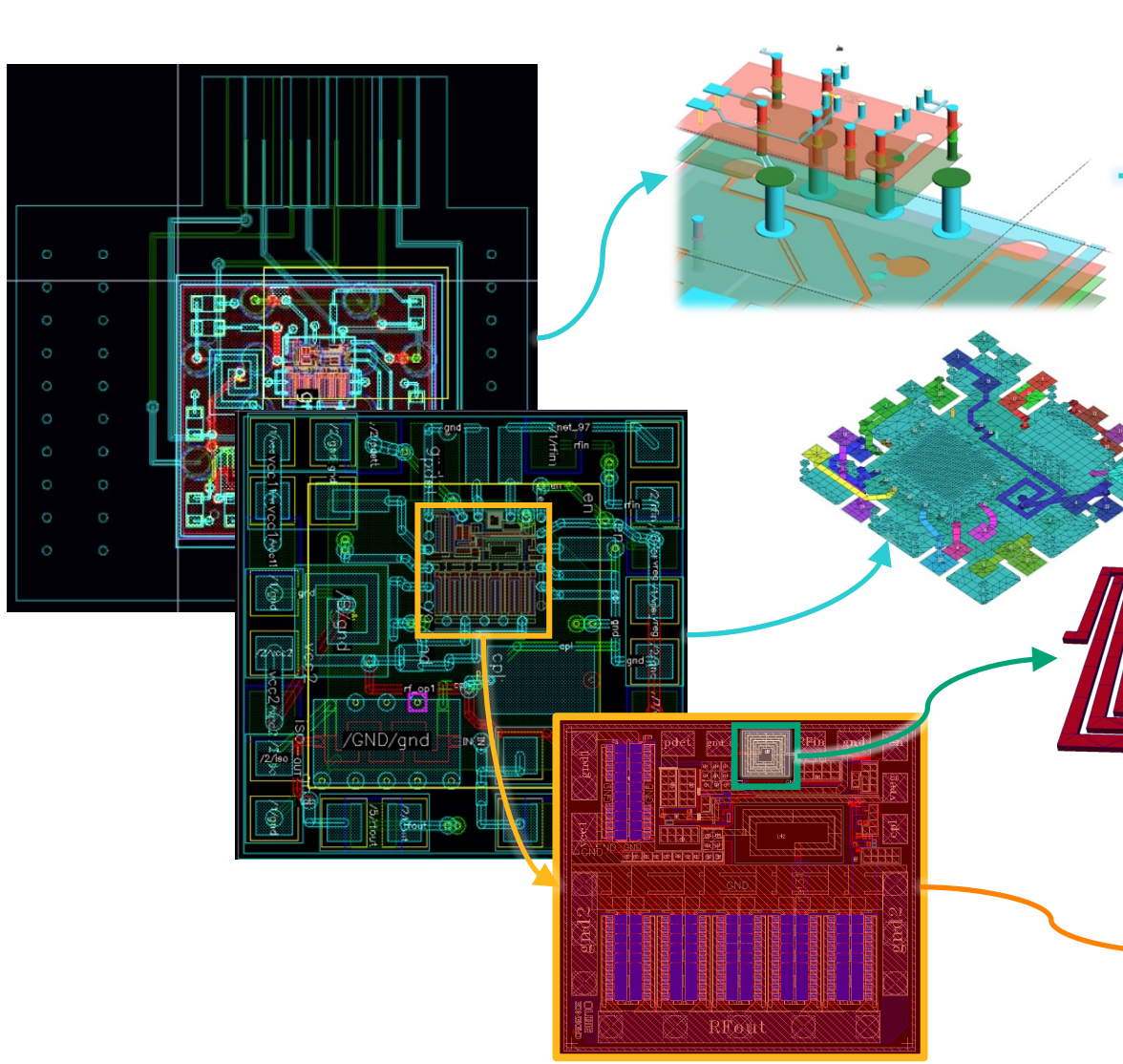
Specialized EM modeling



- 3D FEM
- Full package modeling
- MoM for III/V die
- MoM for silicon die
- Die-level RC extraction

Integrated Extracted System-Level View

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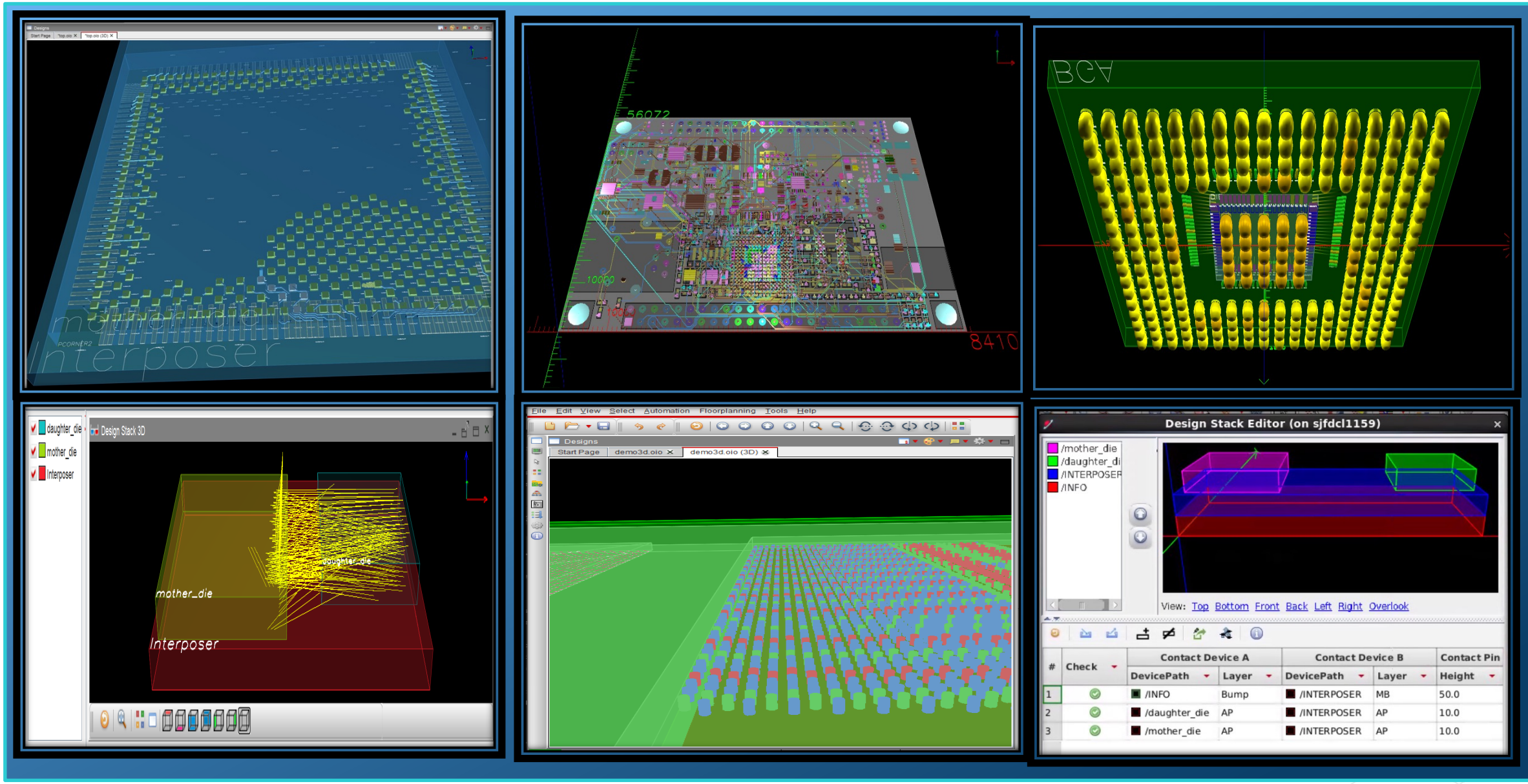
3D Viewing Capabilities for 3DHI



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Conclusion

- The age of Moore-than-Moore has arrived, and packaging is a huge beneficiary
- There are still many challenges to overcome to bring 3D heterogeneous integration to the mainstream
- The worlds of IC designers and package designers are converging
- IC/package co-design and analysis is imperative
- There are EDA solutions today that enable co-design/co-analysis

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