Enabling Co-Design of 3D Heterogeneous Packages

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Product Director
The Beginning of the “More Than Moore” Era

For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing… The economics of semiconductor logic scaling are gone…

Gordon Moore knew this day would come. He also predicted that “It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

Providing a possible alternative to advanced monolithic SoCs, multi-chiplet SiPs have become a very attractive option for cost-sensitive complex designs.

The generation of “More Than Moore” is here…
Simply Following Moore’s Law Alone is No Longer the Best Technical and Economical Path Forward

Cost & Yield & Size

- **28nm**
- **22nm**
- **16nm**
- **10nm**
- **7nm**
- **5nm**

Lower Memory Wall

Form-Factor & Modularization
SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures
The transition from system on a chip (SoC) to system in a package (SiP)

PCB

Board size/complexity reduction (SWaP)

Multi-Chip(let) Packaging
(Including stacking)

Disaggregated SoC

SoC/ASIC

MCM/SiP

Unpackaged die

Heterogeneous Integration

Chiplets

PCB to MCM/SiP Benefits
- Smaller footprint
- PCB simplification
- Higher bandwidth
- Lower power

SoC to HI Benefits
- Reduced NRE costs
- Shorter time to market
- Larger than reticle size designs
- More flexible IP use-model
Heterogenous Integration Leverages Multiple Packaging Technologies
The Needs of IC and Systems Designers are Converging

OSATs (SWaP)
Board design impact on packaging
1980-2010

IC
Foundries (PPA)
IC design impact on packaging
2011-Now

PCB Layout Flow
System-Level Analysis

PCB-like Flow
System-Level Analysis

IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis

IC Flow
IC signoff Methodology
3D Packaging Versus Silicon Stacking (3DHI)

**3D Packaging**
- Solder-based connections (>25um)
- Each die designed independently
  - Black-box abstracts used for layout
- I/O buffer to I/O buffer signaling

**Silicon Stacking**
- Solder-free connections (<10um)
- Single RTL partitioned at implementation
  - Full detail of IC required for layout
- DBI, hybrid-bond, cu-to-cu, direct connection
Times Have Changed…

• Yesterdays Advanced IC Packaging
  o *Necessary evil*
  o Avoid negative impact on chip
    – Electrical, Thermal
  o Protect chip from the outside world
  o Redistribute IO to pitch more suitable for the PCB layout

• Todays advanced IC packaging is about *adding value* to end products
  o Multi-chip(let) solutions leading the way for “More than Moore” vision
  o Companies leveraging packaging technologies to create value and differentiation from their competitors
  o TSV, WLP and 3D stacking technologies providing a tremendous number of packaging options for all form-factors and budgets
Multi-Chiplet 3D Diverse Ecosystem Challenges

Assembly Design Kits
- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
- Foundries need to provide the packaging engineer all the data he/she needs to produce manufacturing output of a design that can be assembled and tested
- Contents; tech files, libraries, assembly rules, substrate DFM, rule decks, and design templates
- Security and Test solutions

COTS Chiplets
- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
  - CHIPLET.US
- Progress with chiplet exchange formats
  - CDX, 3Dblox™
- Common communication interface
  - AIB, UCIe, BoW, …
- Too many packaging options to standardize on a single interface
Multi-Chiplet 3D Flow Challenges

Design Tools/Flows
- Explosion in the number of design tools and required expertise mean complex design flows
- **Co-design/co-analysis across die/chiplet/package is now mandatory**
- Capacity and performance impact on tools
- Support of existing and emerging 3D-IC standards
- Silicon stacking breaks abstract die representation use model
- Package designers pivoting to foundry-based design and sign-off requirements

Analysis and Sign-Off
- Early-stage and signoff-level thermal/power analysis
- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Stacked-die EMIR
- Stress and CMP planarity checks
- New 3D-IC test standards
- High-capacity EM/SI/PI to support very large structures (billions of instances)
- Compliance kits for new chiplet-to-chiplet communication standards
Over-the-Wall Approach Fails For Analog/RF 3D HI Packaging

- Separate logic/design capture means no system-level LVS (SystemLVS) and redundant schematic/libraries.
  - Many manual steps between domains

- IC designers use estimated package and PCB layout parasitics, leading to unexpected performance limitations

- Traditional design methodologies are breaking down
Why Can’t We Have One Layout Tool For Everything?

- Each platform has inherent advantages and disadvantages
- Capacity should be considered
- Two or more platforms often required to create optimal design
- Cross-platform solutions improve domain to domain data exchange/co-design

<table>
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<tr>
<th></th>
<th>Package/PCB</th>
<th>Analog/RF IC</th>
<th>Digital IC</th>
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<tbody>
<tr>
<td>Architecture</td>
<td>GUI-centric layout</td>
<td>Schematic capture, hierarchical layout</td>
<td>Language-driven flat design</td>
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<tr>
<td>Package Type</td>
<td>BGA/LGA, FOWLP, PoP, Si bridges</td>
<td>RF module, Photonics</td>
<td>2.5D-IC, 3D-IC</td>
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<tr>
<td>Die Model</td>
<td>Blackbox abstract</td>
<td>Transistor level</td>
<td>Standard Cell level</td>
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<tr>
<td>Routing Styles</td>
<td>Constraint-driven, push/shove 45-degree routing</td>
<td>PDK-driven, 90/45 degree/CurvyCore™ routing</td>
<td>Timing-driven routing, 45-degree RDL routing</td>
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<tr>
<td>Capacity/Perf</td>
<td>100,000s</td>
<td>1,000,000s</td>
<td>1,000,000,000s</td>
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<tr>
<td>Extraction/Analysis</td>
<td>3D-EM, SI and PI</td>
<td>RC Extraction + 3D-EM</td>
<td>RC Extraction</td>
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<tr>
<td>Manufacturing Outputs</td>
<td>Board/Substrate Foundry</td>
<td>Foundry</td>
<td>Foundry</td>
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<tr>
<td>Physical Verification</td>
<td>Only required in some applications</td>
<td></td>
<td>Sign-Off DRC and LVS</td>
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<td>OS</td>
<td>Windows, Linux</td>
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High-Level Co-Design Flow

3D-IC Design Platform

- System-Level Aggregation, Planning and Analysis
- Digital/Analog/RF Die/Chiplet Design
- Advanced 3D Packaging
- 3D-EM, Electrical and Thermal Sign-Off
- Common Database
Digital-Centric Top-Level Aggregation, Co-Design and Optimization

- Multi-design management with chip(let)-chip(let)-package-board signal-mapping
- Hierarchical Planning and Optimization of System-Level Design and Connectivity
- Early-Stage Thermal/Power Analysis
- Stack management (Supports 3Dblox™)
- System-level connectivity/stack alignment verification (SystemLVS)
- Advanced bump/TSV planning
- System-level co-optimization
Flexibility Importing Design Data Into Co-Design Platform

Industry Standard Formats

Assembly Design Kits (ADK)

ECO Flow With Layout Tools

Build On-The-Fly
Schematic Driven (Analog/RF) Co-Design/Analysis Flow

- Chip(let)/package (multi-PDK) co-design/analysis solution built on IC design platform
Analog/RF Co-Design and Co-Analysis Flow

- Schematic-driven layout flow for die, chiplet, package and module design
- Merged IC and package/module layout, to enable co-design across multiple PDKs
- Smart electromagnetic and parasitic analysis, integrating multiple solver technologies
  - Geometry and mesh viewing
  - Automatic stitching of EM models into golden schematic
- Functional circuit simulation with embedded on-die and off-die layout parasitics
- Physical verification and manufacturing outputs
Designer Perspective Views for IC/Package Co-Design

Package Designers View

Die Designers View
System-Level Layout Parasitic Back-Annotation and Simulation

- Coupled 3D-EM extraction between chip(let), package, and PCB layout databases
  - Multiple 3D-EM engines integrated through assistant
  - Support for partial/full nets, groupings, and device-level modeling
  - Direct pin mapping and eliminates double-counting of discrete devices
  - S-parameters (freq. domain) and RLGC (time domain) models
- Automatically create schematics (extracted views) that include the layout parasitics from the package and PCB
  - Must support multi-PDK, multi-die solutions (namespace collision avoidance)

**Simulate**

Setup testbench and model selection

Parasitics automatically stitched into schematic hierarchy

Automatic Mapping of S-Parameter Models to N-Port Cell Instances

S-Parameter Model
Specialized EM modeling

- 3D FEM
- Full package modeling
- MoM for III/V die
- MoM for silicon die
- Die-level RC extraction
3D Viewing Capabilities for 3DHI
Conclusion

The age of Moore-than-Moore has arrived, and packaging is a huge beneficiary

There are still many challenges to overcome to bring 3D heterogeneous integration to the mainstream

The worlds of IC designers and package designers are converging

IC/package co-design and analysis is imperative

There are EDA solutions today that enable co-design/co-analysis